DISSERTATION

EFFECTS OF CONTACT-BASED NON-UNIFORMITIES IN CDS/CDTE THIN-FILM SOLAR CELLS

Submitted by

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WE HEREBY RECOMMEND THAT THE DISSERTATION PREPARED UNDER OUR SUPERVISION BY ALAN R. DAVIES ENTITLED EFFECTS OF CONTACT-BASED NON-UNIFORMITIES IN CDS/CDTE THIN FILM SOLAR CELLS BE ACCEPTED AS FULFILLING IN PART REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY.

Graduate Committee

Advisor

Department Head

ABSTRACT OF DISSERTATION

EFFECTS OF CONTACT-BASED NON-UNIFORMITIES IN CDS/CDTE THIN FILM SOLAR CELLS

To strongly contribute to the near-term electricity supply, CdTe-based photovoltaic devices must continue to improve in performance under the constraint of simple and cost efficient fabrication methods. Uniform device behavior is a particular challenge for large area devices with minimal layer thicknesses. This thesis focuses on characterization and modeling of devices with non-uniform performance induced by the cell contacts. Devices were obtained from a commercially viable pilot-scale fabrication line at Colorado State University, from the National Renewable Energy Lab, and from the University of Toledo.

Current versus voltage (J-V), quantum efficiency (QE) and laser-beam-induced current (LBIC) techniques were used to characterize the devices in these studies. Numerical simulation and equivalent circuit modeling were also undertaken to contextualize and reproduce non-uniform device behavior.

The p-type CdTe semiconductor has a large work-function and thus tends to form a Schottky barrier when the back-electrode is formed. Cu can be included in the structure to mitigate the performance-limiting contact barrier. In otherwise identically processed devices, a Cu-containing contact was found to increase efficiency from the 6-7 % to the 11-12 % range over devices with no Cu. This coincided with a dramatic decrease in lateral variations in collection efficiency, and improved fill-factor (FF) from ~45 % to ~70 %. Low FF in Cu-free devices was caused by a temporary rollover effect in the fourth quadrant of the J-V plane. Barrier non-uniformities in devices with little or no Cu were identified with the LBIC measurement and modeled using PSpice software. The model developed for this work was sufficient to simulate a J-V curve with similar fourth-quadrant rollover to that observed in the experimental devices.

The Schottkey barrier is not the only source of non-uniformities from the back-contact. Devices with no distortion in the J-V curve, but fabricated with Au, Ag, Ni, or Al electrode

layers showed a strong dependence of uniformity on the metal choice. LBIC characterization showed that Au and Ni electrodes produced devices with a variation of 638-nm QE of about 1 %, centered around the 81 % level. For Ag, the QE variation increased to $\sim$ 12 %. The cell with an Al contact had extremely low current, reflected in the LBIC as a near null result except for small areas of high performance (QE $\sim$ 80 %). Again here, increased variations seen in LBIC data correlate strongly with reduced FF and, hence, efficiency.

CdTe cells generally employ front contacts made from transparent-conducting oxides (TCOs), F:SnO_2 in this work. When the n-CdS layer of the CdS/CdTe structure is thinned to facilitate greater current generation, non-uniformities of the solar cell junction arise from isolated CdTe contact with the TCO layer. Numerical simulations suggest that the SnO_2/CdTe junction is weaker than CdS/CdTe because of a large cliff-like conduction-band offset induced by the differing electron affinities in the heterojunction, such that device voltage is decreased by approximately the excess offset for values greater than 0.2 eV.

Experimental devices fabricated by evaporation and sputtering were measured had open-circuit voltage less than 400 mV for CdS $\sim$ 30 nm, while otherwise identical devices gave V_{oc} near 800 mV for CdS thicker than $\sim$ 100 nm. An empirical relationship between CdS thickness and the low-voltage area was developed and applied in the context of a model predicting device V_{oc} based on the mix of high- and low-voltage areas. For large (i.e. $\sim$ 400 mV) variations in the local V_{oc}, the total device response tends towards the low-voltage level with as little as 10 % weak-area fraction. LBIC-verified increasing non-uniformity in devices with thin CdS and whole-cell performance followed the trends predicted by simulations. The practical limit of CdS thickness was about 120 nm for evaporated CdS layers and near 80 nm for sputtered layers. The key parameters determining the thin-limit for CdS appear to be the SnO_2 surface roughness and the relative grain sizes of CdS and SnO_2.

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Chapter 1

The case for solar energy

This thesis is concerned with industrially relevant cadmium telluride (CdTe) based thin-film solar cells and modules. It will explore in some detail the consequences of measures taken to increase efficiency, while maintaining a minimum number and complexity of processing steps. The particular constraints placed on the fabrication methods studied here reflect the major goal of the thin-film photovoltaics community, namely to maximize the overall figure of merit for photovoltaic (PV) electricity generation—kWh/$. CdTe and other solar cell technologies continue to gain traction in the public attention because they represent an alternative method for generation of electricity to the traditional burning of fossil fuels to run steam driven turbines. A brief background of the modern energy situation is provided to establish a motivation for the pursuit of low-cost, high-efficiency photovoltaics.

1.1 The ghosts of energy: past and present

Mankind has an apparently insatiable appetite for energy. This appetite has steadily grown with increasing population and technological development. Integrating all of the energy 'produced' in a year and dividing by the number of seconds in a year, one arrives at an average rate of consumption of 14.5 TW, using 2006 numbers.[1] The lion's share of all of this energy is made available by burning oil, coal, and natural gas.

1.1.1 The modern energy mix

Fossil fuels dominate the energy supply mix with a modest contribution from nuclear and hydroelectric, and nearly insignificant representation of wind, renewable biomass and solar thermal and PV. In 2006, people converted 3090 megatonnes-oil-equivalent (MTOE) of coal, 3889 MT of oil and 2574 MTOE of natural gas to energy, for a net heat release of $4 * 10^{20}$ Joules. The other sources worth mentioning at these scales are nuclear and hydroelectric, accounting together for an equivalent of another 1323 MTOE [1] and bringing the total energy production of 2006 to $4.56 * 10^{20}$ J. Projections for 2006 suggest that about 15 billion kilowatt hours of electricity were consumed, which represents about 10% of that energy total, but the actual number of joules devoted to electricity production is quite a bit higher, when the $\sim$ 35% conversion efficiency of coal-fired power plants is taken into account. The lost energy is released to the environment as heat, and the CO_2 generated by the burning of the fossil fuel is (mostly) sent into the atmosphere.

Even at these scales of usage, the reserves of fossil fuels are abundant. At 2006 rates of consumption, the proven oil reserves will last for 40 years. Natural gas reserves will hold out for 65 years, and coal will last at least 200 years [1]. Fuel for nuclear reactors is not in short supply, although it can be expensive to prepare and socially sensitive to dispose of. As long as it continues to rain and snow in the mountains, the effectiveness and use of hydroelectric power are not expected to decline. It is natural to assume that the distribution of fuel consumption will shift under economic pressures as one type or the other becomes more scarce–naturally or in the supply chain, but it can be concluded that the presently dominant energy resources, especially fossil fuel supplies, are abundant enough to support the changing and growing world economy for some generations. If the emissions from fossil fuel burning were not implicated in recent worries about climate change, there would be no short-term reason to investigate alternative energy sources.

1.1.2 Consequences of fossil-fuel-based energy

With the details of the previous section in mind, it is reasonable to ask how well-founded concerns about the connection between energy consumption and climate change really are.

Let us consider, as an example, the combustion of gasoline. When gasoline—which for simplicity we'll assume is composed of 70% iso-octane (C_4H_{18}) and 30% heptane (C_7H_{16})—is burned, the reaction takes oxygen out of the environment and combines it with the hydrocarbons according to

$$C_8H_{18} + 25O_2 \rightarrow 8CO_2 + 9H_2O + heat, \tag{1.1}$$

and

$$C_7H_{16} + 22O_2 \rightarrow 7CO_2 + 16H_2O + heat, \tag{1.2}$$

assuming complete combustion for the octane and heptane, respectively. One US gallon of gasoline is about 2.7 kg, and according to the given proportion, is about 2.65 ℓ octane and 1.1 ℓ heptane, has on the product side of the two reactions a total of about 186 mol, or 8.2 kg of CO_2. It is apparent from this that by weight, more CO_2 gas is produced (by a factor of ~ 3) than the weight of the original hydrocarbon that was burned. If this factor is applied to the $\sim$ 10 gigatons of fossil fuels burned each year, CO_2 emissions to the atmosphere are in the ballpark of 30 Gt/yr. This is enough, it turns out, to measurably increase the atmospheric CO_2 content, which in turn increases the re-radiation of long-wave energy back to the earth. The greenhouse effect, which makes life on earth possible, has been shown [2] to have increased the incident power density at the earths surface by ~ 4 % on average, since the beginning of industrialization. Beginning in 1958, CO_2 has been directly monitored at Mauna Loa, HI and the results of those measurements are indicated in figure 1.1. Figure 1.2 shows simultaneous average temperature and atmospheric CO_2 concentration data which are extracted from polar ice core samples. Note that the present levels of CO_2 as measured at Mauna Loa (fig. 1.1), where it is assumed that adequate atmospheric mixing occurs such that the figures represent a reasonable average of worldwide conditions, are fully 50% greater than at any time in the last 400,000 years (fig. 1.2). While there are bound to be some error bars on both sets of data (not reported), the difference is much larger than the weakness of the data. Obviously, the last 400,000 years have included periods where the climate was distinctly unfriendly for human habitation, and if the correlation between

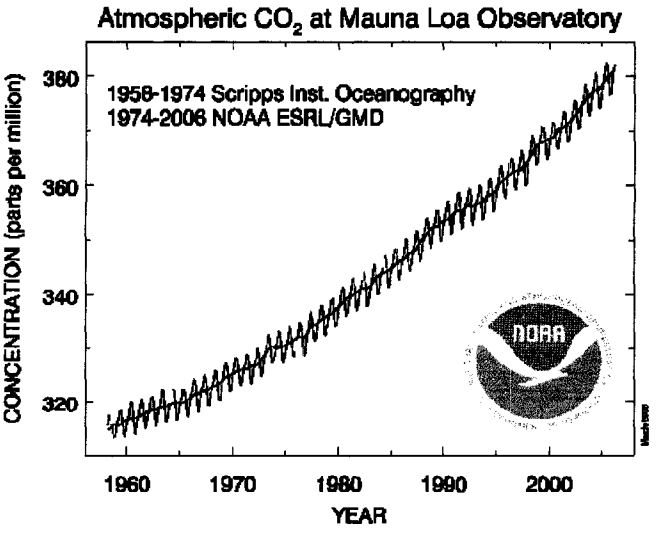

Figure 1.1: Atmospheric CO_2 observed at Mauna Loa, HI since 1958. Linear reverse extrapolation of the 1960-1970 data to the pre-industrial age (around 1850) places CO_2 concentration between 220-260 ppm.

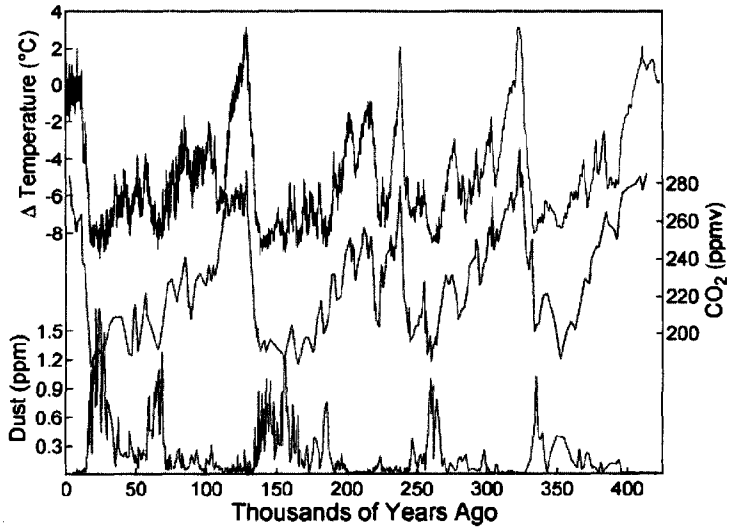

Figure 1.2: Temperature (blue) and CO_2 (green) concentration data inferred from the Vostok station ice-cores. Figure reproduced from [3].

atmospheric CO_2 levels and climate is truly as close as it appears from figure 1.2, then there is in fact cause for alarm about the environmental trends associated with emissions from fossil-fuel-based energy.

1.2 The ghost of energy: future

We have established that mankind, particularly through its relation to energy consumption, has had a pronounced effect on the compositional makeup of the atmosphere, and the newly CO_2 rich atmosphere has increased the radiative power density at the earths surface. This increased retention of heat is projected to have severe impacts on the climate. It is therefore incumbent upon present generation, armed with this knowledge, to find ways of reducing CO_2 emissions. Lowering the overall energy consumption does not appear realistic, as increasing energy usage appears to be prerequisite to social and economic development. Discovering and implementing alternatives to greenhouse-gas-emitting sources, then, may be the best route to meeting the simultaneous goals of economical energy provision and reduction of CO_2 emissions. Electricity obtained directly from the sun via the photovoltaic effect may prove to be one of the prime contributors to the 'new-energy' future.

1.2.1 Solar potential

At the mean radius of the Earth from the sun, about 93 million miles, the intensity of sunlight is approximately 135 mW/cm^2. After passing through, on average, 1.5 thicknesses of the atmosphere, the terrestrial intensity—termed 'air-mass 1.5', or simply 'AM1.5'—is 100 mW/cm^2. The earth's radius is nearly 6500 km, so it presents a cross section of about $1.3*10^{14}$ m^2 to the incoming sunlight. This means that the net power incident on the earth's surface is around $1.3*10^{17}$ W. About every three-thousand seconds, as much energy strikes the earths surface in sunlight as all of mankind used in 2006. A rough calculation shows that an area coverage of about $1.6*10^{11}$ m^2 would be necessary at an average conversion efficiency of 10% in order to meet the world energy demand. This about one-third of the land area of the state of Wyoming.

1.2.2 Challenges to the PV industry

As mentioned at the beginning, the key figure of merit for solar cells and modules is kWh/$. Practically, this is a difficult metric to obtain, as it would involve assumptions (or lengthy measurement) of a module's power output over its entire useful life. It is therefore more

common to judge a given fabrication method or technology in terms of $\$/W_p$ of the resulting modules, where W_p, or *watt peak*, describes the power conversion under peak terrestrial illumination conditions. Regardless of the metric used, PV generated electrical energy is, at the current state-of-the-art, more expensive than traditional electricity. The primary goal of the PV research community, then, is to minimize this figure of $\$/W_p$, and there are a plurality of approaches to do so, which are undertaken in parallel.

Mathematically, $\$/W_p$ is reduced when $\$$ is minimized or W_p is maximized, or both. Translated to PV technologies, the first part means reducing the cost of PV modules, which may be achieved by using less- and/or less-expensive material than the current state-of-the-art. Secondly, one can attempt to increase the W_p figure by improving the conversion efficiency of the PV devices constituent to the module, which reduces the number of cells/modules necessary for a given power output, or supplies more power for a constant area coverage.

The present day PV market is dominated by producers of modules based on mono- or multi-crystalline Si wafers. The cost of raw materials represents a significant fraction of the overall $\$/W_p$ for Si-based PV because of high requirements for material purity and perfection, and low material yield. Though the overall cost of Si-based PV has come down significantly in recent years, it remains substantially higher than fossil-fuel-based electricity. In the last twenty or so years, a new class of solar-cell technologies has emerged as a promising alternative to Si—thin-film solar cells based on polycrystalline $CuIn_{1-x}Ga_xSe_2$ (CIGS) or CdTe. The thin-film systems present numerous advantages over Si. Due to their band-structure properties, hundreds of times less material is required to absorb the same fraction of sunlight. Also, at equivalent conversion efficiency, thin-film cells can tolerate hundreds of times more impurities than their silicon counterparts. Though the record efficiencies of $CuIn_{1-x}Ga_xSe_2$ and CdTe lag those for mono- and multi-crystalline Si (table 1.1, η = efficiency), the economics of the thin-film technologies is already more attractive than Si, according to the $\$/W_p$ metric. A further advantage of the thin-film technologies is their immaturity, and they show great promise for cost reduction with production volume, as seen in figure 1.3. The research presented in this thesis is concerned exclusively with the thin-film CdTe system, its unique strengths and the particular challenges encountered with

Table 1.1: Record efficiency data tabulated from [4] show substantial room for growth of the thin-film module market if performance reaches a similar fraction of the theoretical maximum to Si. (*Figures for CIGS based on alloy ratio corresponding to current experimental record)

Technology	Crystalline Si	CIGS	CdTe
Max. Theoretical η	28%	24%*	28%
Record lab-scale η	24.7%	19.5%	16.5%
Record *module* η	22.7%	13.4%	10.7%
$\Delta\eta$ (Lab-production)	2%	6.1%	5.8%

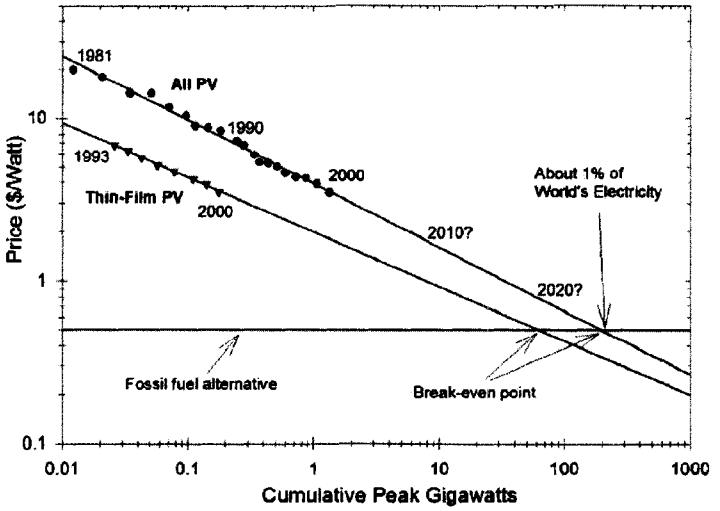

Figure 1.3: Price comparison for thin-film and Si photovoltaics. For equal production volume, thin-film PV delivers significant cost advantages. Figure reproduced from [5].

that technology. Let us now, therefore, turn the rest of this general discussion to CdTe.

1.2.3 CdTe thin-film solar cells

As with the larger PV industry, the key challenge facing the CdTe thin-film technology is the harmonization of techniques which, alone, could be employed to improve one or another of the factors determining the $\$/W_p$. Difficulties arise when desired strategies come into conflict with one another. Methods that increase the solar conversion efficiency may also require the expansion of the fabrication process to include additional cleaning and deposition steps, thereby simultaneously increasing the cost. The approach that is taken in the present research, is to constrain the deposition and subsequent processing to a minimum of steps, and attempt, by gaining an understanding of the physical processes which limit

the end performance, to optimize those limited processing steps for maximum efficiency and stability.

CdTe solar cells are most typically fabricated in a superstrate configuration, meaning that the light first travels through the glass and front, or n-side contact before being absorbed. The front contact is made with a transparent-conducting-oxide (TCO) layer, and n- and p-type semiconductors are the deposited to form the solar cell junction. Post deposition $CdCl_2$ and annealing treatments are undertaken to improve the electrical characteristics of the CdTe layer, and then application of a back-electrode layer completes the device. A schematic of the layer structure and energy band diagram is given in figure 1.4.

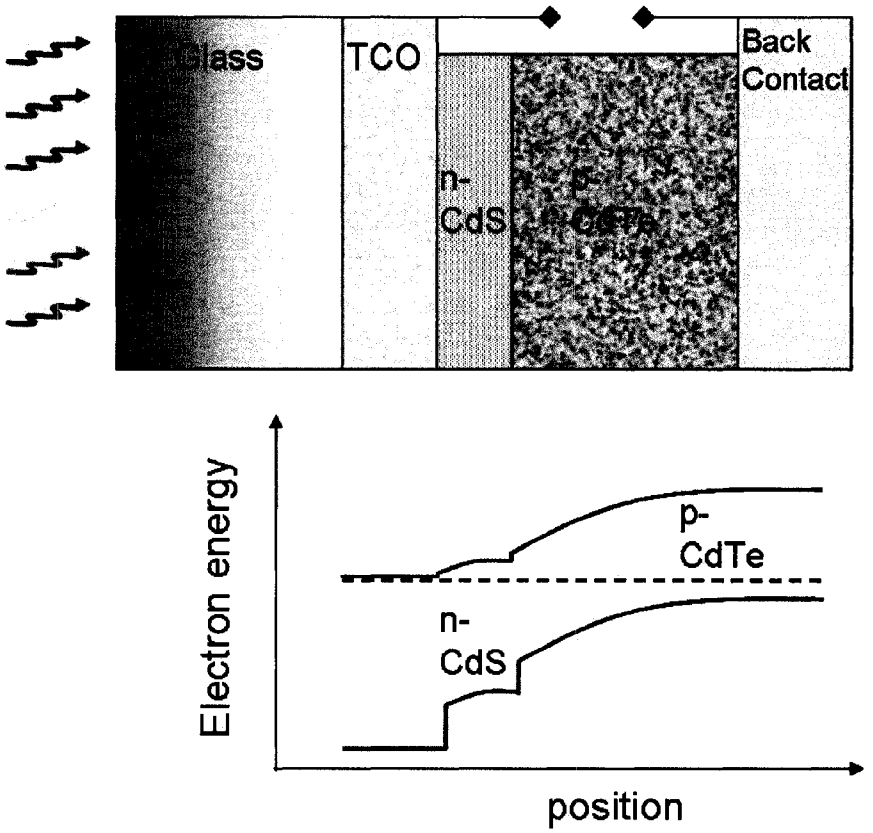

Figure 1.4: Ideally, the deposited layers of the solar cell form a large-area photosensitive diode. In practice, many non-idealities exist, including parasitic resistances and non-uniform physical and electrical properties. (layer thicknesses exaggerated)

Two areas where the choices made regarding cell processing substantially impact the final efficiency are at the front and back contacts. Optimization of the initial performance of

CdTe cells requires treading a fine balance of layer thicknesses, deposition temperatures and conditions, and post-deposition processes and there is also no guarantee that an initially high performance cell will prove robust when subjected to harsh environments.

Because of their polycrystalline nature, thin-film solar cells are susceptible to variations in the layer properties, which can affect larger areas than the variations themselves. In fact, many promising processing technologies, in terms of cost and scalability, produce cells which show substantial *non-uniformity.* The front- and back-contact-related originators of non-uniformities, which harm the performance of CdTe solar cells are the major theme of this thesis. They are investigated using the light-beam-induced-current, or LBIC, technique and device models are developed to account for their influence in whole-cell performance. We identify potential sources of such non-uniformities and relate them to aspects of the device fabrication, in order to be able to suggest ways to mitigate harmful effects of their presence.

Chapter 2 will describe (a) the basics of thin-film CdTe solar cell operation and (b) the various characterization methods and modeling tools used in this work and their common interpretations. Chapter 3 will present data and discussion showing how back-contacting to CdTe cells represents a major source of device non-uniformity, which is at least partly responsible for reduced and non-ideal cell performance. Some suggestions are offered for reducing non-uniformities of the back-contact in chapter 4. In chapters 5 and 6 the focus shifts to the front contact and window construction of the solar cell. Chapter 5 will present data showing the dependence of device uniformity and overall performance on the front-contact structure. The conflict between efficiency maximization and performance limiting effects of various window layer techniques is discussed and the connection to device uniformity is drawn. Strategies for front-contact non-uniformity mitigation are given in chapter 6.

Chapter 2

Thin-film solar cell physics and characterization

There are three key features of the CdS/CdTe thin-film material system that allows it to efficiently generate electricity from sunlight: (1) CdTe is a direct-gap semiconductor with a band-gap optimally matched to the terrestrial solar spectrum; (2) there is a sufficiently strong electric field built into the n-CdS/p-CdTe device to effectively separate electrons and holes and collect photocurrent; (3) the device can be contacted such that the separated charge carriers can be delivered to an external circuit. Thin-film CdTe solar cells have been fabricated by many methods, with greater or lesser success in the three areas [6–12].

Several characterization methods have been developed over time to investigate the physical factors that determine the degree to which a solar cell performs in each of these respects. The results presented in this document were obtained using current-density-versus-voltage (J-V) measurements to give high level information about whole cell performance parameters, and conversion efficiency. Spectral response, or quantum efficiency (QE), and capacitance measurements give the average response of the whole cell area to monochromatic illumination (QE), and response of the depletion layer to applied voltage bias (capacitance). Finally, laser-beam-induced-current (LBIC) measurement resolves the solar cell QE at one wavelength with high spatial resolution, allowing the user to identify local sources of reduced performance and to formulate strategies to prevent small defects from catastrophically af-

fecting whole-cell response. The first section of the present chapter will discuss the salient features of the semiconductor materials that permit conditions 1-3 above. The second section focuses on the method and interpretation of the characterization tools indicated.

2.1 Basics of solar cell operation

The physics of light absorption, carrier separation and collection, and cell contacts are briefly developed, with the aim of establishing a background for the concepts explored in this thesis.

2.1.1 Light absorption

A semiconductor's ability to absorb light is primarily determined by its energy band structure. The bands of allowed electron energies are, in turn, dictated by the crystal structure and constituent elements of the semiconductor. The periodic potential established by the lattice, and the electronic levels of the valence shells of the involved elements allow specific energy states for electrons in the material. In semiconductors, these states form quasi-continuous bands, separated by energies of about one-half to a few electron-volts (eV). The highest energy band, which at room temperature is mostly full is called the valence-band, and the mostly-empty band above that is the conduction-band. The energy difference between the minimum of the conduction band and the maximum of the valence band is called the band-gap. The band-gap for CdTe is 1.48 eV. This is the same as the energy content of a photon with wavelength of $\sim$ 840 nm.

For some materials, the conduction band minimum occurs at a different value of crystal momentum ($\vec{k}$) than the valence band maximum. These materials are denoted as "indirect-gap" semiconductors as opposed to "direct-gap" materials such as CdTe, in which the conduction band minimum occurs 'directly' above the valence band maximum in an E vs. $\vec{k}$ diagram.

When a photon with energy greater than the band gap is absorbed, it can induce a transition of an electron out of the valence-band into the conduction band. During such a process, the conservation laws for energy and momentum must be obeyed, and since photons

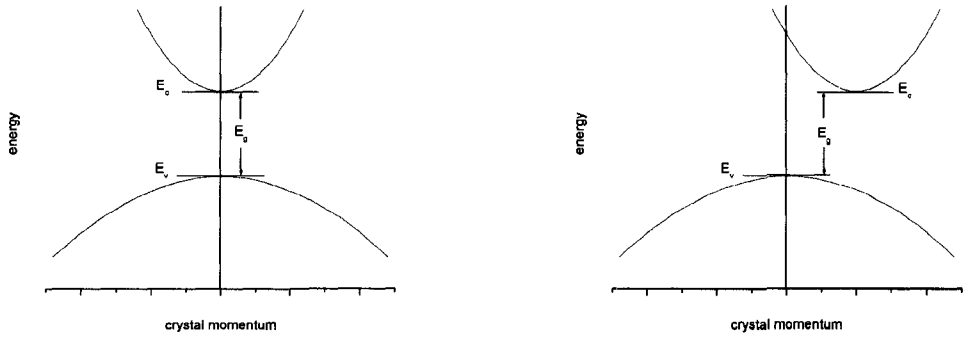

Figure 2.1: Schematic diagrams of allowed energy bands for direct (left) and indirect (right) semiconductors. The requirement for a simultaneous photon-electron-phonon interaction makes light absorption in indirect materials significantly less likely than in direct-gap semiconductors.

carry very little momentum, the minimum energy transition in an indirect-gap material requires the electron to simultaneously emit or absorb a phonon to gain the momentum shift necessary to access the available energy states at the bottom of the conduction band. The low probability of simultaneous photon and phonon interactions makes the absorption of a photon much less likely and results in a low absorption coefficient for indirect materials. The single interaction of photon and electron necessary to induce a direct transition is much more probable. For example, at the band-gap energy, the absorption coefficient for CdTe is $\sim 10^4$ cm^{-1}, whereas for Si, it is $\sim 10^2$ cm^{-1}. For solar cell fabrication, CdTe layer thicknesses are measured in units of microns, and Si wafers are measured in hundreds of microns.

The density of photons, or the intensity of the light, attenuates exponentially with depth in the material with the relation

$$I(z, \lambda) = I_0(\lambda) e^{(-\alpha(\lambda) z)}, \tag{2.1}$$

where I is the intensity of light with wavelength λ at depth z into a material with wavelength dependent absorption coefficient α. Since each absorbed photon results in one electron-hole pair, this equation also describes the generation profile for carriers.

The CdTe band-gap of 1.48 eV is considered an optimal match to the solar spectrum.

One might ask why the very minimum band-gap wouldn't be more desirable, since more photons could be converted to current, but it is the *power conversion*, not simply the current, which is of primary interest. The calculation must therefore also include the voltage at which the photocurrent can be delivered, and this depends on the band-gap as well. The curve of power-conversion versus band-gap for a single-junction device describes the trade-off between current and voltage based on ideal diode theory.

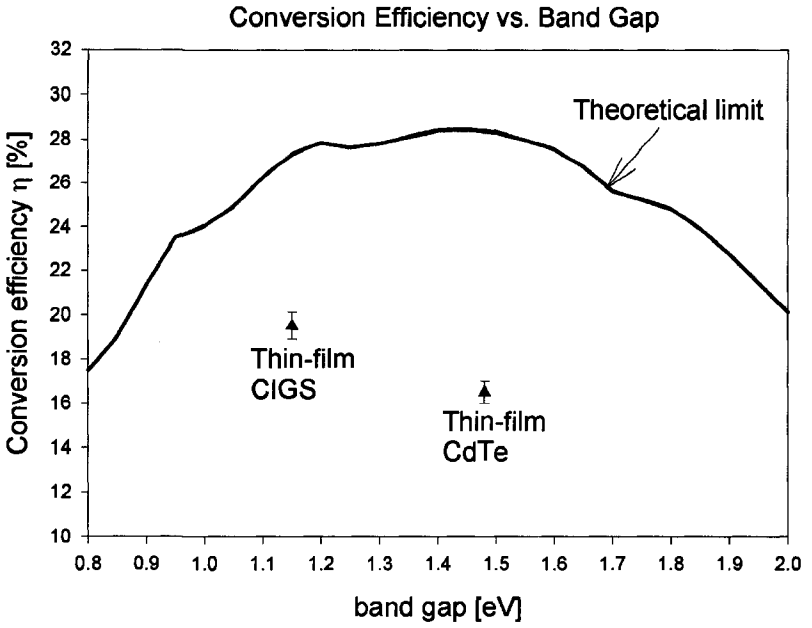

Figure 2.2: Ideal efficiency as a function of band-gap for a single junction device. The peak at around 29 % corresponds very nearly to the CdTe band-gap of 1.48 eV. The record efficiencies for thin-film CdTe and CIGS are also indicated.

2.1.2 Separation and transport of carriers

Absorbed photons generate electron-hole pairs in the semiconductor. Solar cells capitalize on a semiconductor junction to efficiently collect the photogenerated carriers and channel them into an electrical current.

Bulk semiconductor properties

The conductive properties of semiconductors at equilibrium can be manipulated by incorporating defects into the host material. These defects can be either physical as vacancies,

interstitial defects or grain faults, or they may be chemical in origin, when impurity elements are introduced either intentionally or by accident. The new energy states provided by defects often lie within the forbidden band-gap. States which are close enough to one of the band edges, that at room temperature they have a high probability of thermal ionization are referred to as shallow *dopants*. Sufficiently high concentrations of *donor* impurities can provide enough free electrons to the conduction band that the material becomes *n-type* owing to the abundance of free negative charge carriers, which control the conductivity. Conversely, defect states which sit a little above the valence band and *accept* electrons from that band due to thermal ionization make the material *p-type*, with the conductivity controlled by the positive majority carriers (holes). It should be noted here that impurities in CdS/CdTe and other thin-film solar cells is a topic of immense complexity and dedicated study. The reader is referred to [13] and its reference list for details on defect studies. Nevertheless, it is generally accepted that CdS deposits as n-type, with a majority carrier (electron) density in the 10^{16} to 10^{18} cm^{-3} range, and that CdTe deposits as p-type, with hole density in the high 10^{13} to 10^{14} cm^{-3} range.

p-n junction

When two semiconductors of opposite majority-carrier-type are brought or deposited together to form a metallurgical junction, the high concentration of oppositely charged free carriers induces diffusion across the metallurgical junction, with electrons from the n-type material recombining with holes from the p-type. The diffusion and annihilation of opposite charges across the junction leaves behind the ionized atomic sites which supplied them—negative on the p-side and positive on the n-side—and induces an electric field in the region of free charge depletion, opposing further diffusion. The static electric field in the p-n junction is central to solar cell operation. It provides a drift force for photogenerated carriers, encouraging the separation and collection of charges into macroscopic electric current. For CdS/CdTe devices, the vast discrepancy in carrier concentrations leads to a virtually one-sided junction, with the electric field extending 100 to 10000 times farther into the CdTe layer than the CdS. The spatial extent of the space-charge region into CdTe is

given by

$$x_p = \sqrt{\left(\frac{2\epsilon_s V_{bi}}{q}\left[\frac{N_d}{N_a}\right]\left[\frac{1}{N_a + N_d}\right]\right)} \tag{2.2}$$

and is related to the CdS depletion width by

$$x_n = \left[\frac{N_a}{N_d}\right] x_p \tag{2.3}$$

where $x_{(p,n)}$ denotes the extent of depletion into the p- and n-regions, respectively. N_a, N_d are the acceptor and donor densities on the p- and n-sides of the junction, V_{bi} is the potential barrier built into the junction and ϵ_s is the dielectric constant of the semiconductor. For the typical condition of $N_d \gg N_a$, equation 2.2 reduces to

$$x_p(V) = \sqrt{\frac{2\epsilon_s(V_{bi} - V_a)}{qN_a}} \tag{2.4}$$

where the change in depletion width in response to an applied voltage bias (V_a) is included.

The field points from the CdS layer, with a positive space charge 'skin' to the CdTe layer with a large negative space-charge volume. Thus, an electron excited into the conduction band of CdTe by an absorbed photon, at a location within this space-charge region, is pushed toward the junction by the drift field. For a given carrier generation rate, higher collection efficiency equates to higher conversion efficiency. The collection of carriers as a function of position in the absorber material is described by the *collection function*, which takes on a different form depending on the dominant current mechanism at a given point. To a reasonable approximation, the collection efficiency for carriers generated in the electric field region is close to unity. When carrier injection occurs outside this region, the collection is dependent on the electrons' ability to diffuse to the field region before recombining, as determined by the minority-carrier (electrons in p-type) diffusion coefficient and lifetime. The collection efficiency of carriers which must diffuse through the quasi-neutral bulk semiconductor material falls off (again to first order) exponentially from the depletion edge with a decay constant related to the minority carrier diffusion length. Advanced models of collection appear in [5]. Regardless of the exact form of the collection function, the general picture of good collection of carriers generated within the SCR and relatively poor collection

of deeply generated carriers is sufficient to keep in mind for developing a physical picture of device behavior. From this consideration alone, it would appear advantageous to engineer the device to maximize the depletion width (i.e. by lowering the carrier density), but this strategy will often result in lower output voltage due to a smaller junction potential barrier [14].

The charge, electric field, and electron potential of two semiconductor junctions are shown in figure 2.3. From 2.3(b) one can see that the charge depletion extends approx-

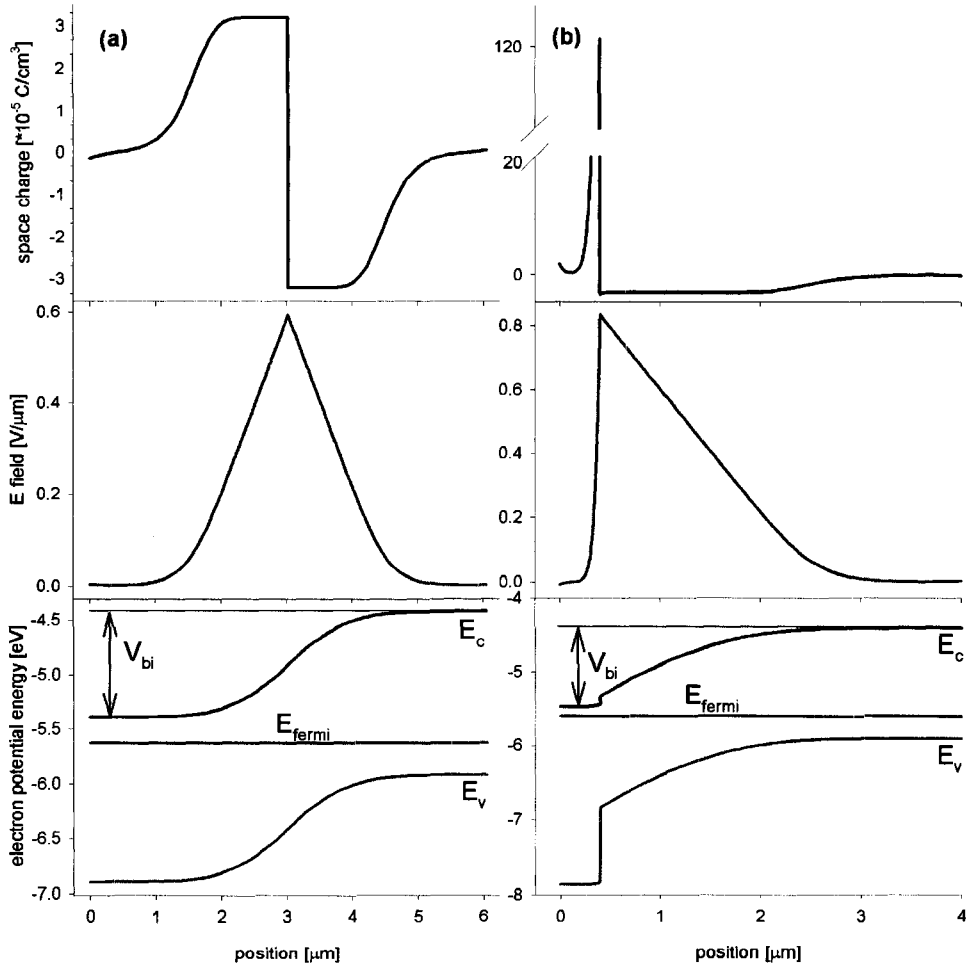

Figure 2.3: Charge, electric field, and energy bands of a (a) generic homojunction with equal n- and p-type doping and (b) a heterojunction with typical parameters for CdS (n-type, left side) and CdTe (p-type, right side)

imately 2.5 microns into the CdTe layer. If the thickness of the CdTe layer is restricted

to smaller values, then the layer is said to be 'fully depleted'. While collection in a fully depleted device is usually good due to the field strength at all positions, V_{bi}, and hence device voltage, tend to be reduced.

2.1.3 Contacts

The photovoltaic power generated in the cell is delivered to the circuit through the front and back contacts. Superstrate CdTe cells feature a transparent-conductive oxide (TCO) for the front contact, which allows a large fraction of incident light in the spectral band of interest to reach the CdTe absorbing layer. In choosing a front contact material, one attempts to simultaneously optimize the transmittance, conductivity, chemical and thermal stability, and cost of the layer. A common choice is SnO_2 because of its availability, reasonable transmittance (80-90 % in the visible spectrum), and functional sheet resistance (8-10 $\Omega/\square$)[15]. Most of the cells discussed here use SnO_2 TCO layers. Other TCO materials used in CdTe solar cells include In_2O_3, $CdSnO_4$ and $ZnSnO_4$[11, 16].

The TCO layer is not a metal in the strictest sense, although it fills the role of front contact. In analysis of the device band structure, it is typically treated as a very heavily n-doped semiconductor and could thus be a candidate for serving the double role of contact and n-type junction partner. However, extensive experimental results have shown that having the TCO in direct contact with CdTe is undesirable, as device performance suffers. The mechanisms of this effect are explored in chapters 5 and 6.

At any semiconductor hetero-interface, band offsets may exist in the conduction and valence bands due to the differing band-gaps and electron affinities of the materials involved. Conduction band offsets (CBO's) arise because the electron energy in free space must be a continuous function of position. This energy is referred to as the vacuum level. The requirement of a continuous vacuum level implies that at the abrupt junction of two materials, a discontinuity will exist in the conduction band, equal to the differences in electron affinities of the junction partners. It follows that there will also be an offset in the valence band, such that the sum of the band offsets will be equal to the difference in material band gaps. The band offset affects the potential barrier to current flow and, hence, the current-voltage characteristics and performance of the device.

Back contacts are simple enough in principle. Any metal can act as an electrode. Unfortunately most are not suitable for contacting p-CdTe without adversely affecting the device performance. Common electrode choices include Ni, Ag, Au, Al, Pd, and Pt. Cu is often included as an additive during preparation of the CdTe layer for contacting. Ideally the PV device should not incur performance losses due to the back contact, nor should there be any significant impact on the device band structure. However, the wide-gap of CdTe combined with high electron affinity, and low doping combine to allow the back-contact to play a large role in device performance, and it remains an area of intense study. The back contact is one area where the devil definitely is in the details.

Deposition of any of the above metals onto p-CdTe forms a Schottky diode, with a barrier height mostly dependant on the metal work function. The back-contact barrier, if it is large enough, can impede the injection of holes into the CdTe layer, limiting forward current. The situation becomes more complicated when a non-uniform back surface, or metallization results in spatial variation of the barrier height. The impacts of varying barrier height on device performance are featured in chapters 3 and 4.

2.2 Methods and interpretation of solar-cell characterization

The work presented in this thesis relies heavily on direct experimental measurement of whole-cell and localized performance parameters. The strategy taken is to use analysis of average performance parameters derived from whole-cell measurements to conceive of a band picture for a device fabricated with a given set of process conditions. This picture may be tested against calculations of band-structure and predicted performance using numerical simulation software. The spatially resolved LBIC measurement is applied where useful to establish the degree of variation present due to a specific fabrication parameter and to attempt to discern how the range of localized performance parameters contribute to the whole-cell average. It is the belief of this author that the results presented here need not be considered valid, unless sufficient evidence has been presented that the methods of measurement and data interpretation are sound. To this end, a survey of the experimental techniques, software tools, and data analysis pertinent to this work is presented in the next

sections.

2.2.1 Current density versus voltage (J-V)

Basic photovoltaic parameters are extracted from current-voltage measurements made with the cell in dark, or under illumination. From this measurement one may extract the device efficiency, and gain clues as to the mechanisms of efficiency loss. Parasitic resistances, and some diode parameters can be obtained using careful examination of J-V curves. In the following, the method for performing J-V measurements and general analysis techniques are reviewed.

Measurement technique

A cartoon of the J-V technique used at CSU and an equivalent circuit are given in fig. 2.4. The light source for J-V measurements is a Solar Light Co. A-M 1.5 simulator model

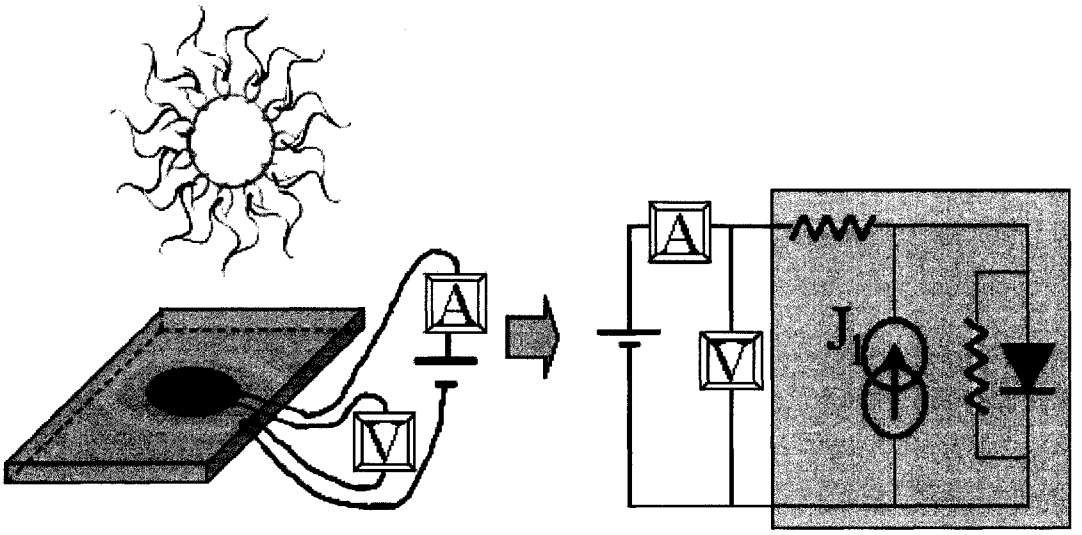

Figure 2.4: A light source of simulated solar spectrum and intensity illuminates the device in the test fixture. Independent circuits for voltage measurement and bias application/current sensing reduce inaccuracies. Analysis is aided by comparing solar cell behavior to an equivalent circuit with elements representing physical parts of the device.

16S-300VB. It uses a xenon arc light source with variable power input to control intensity. Warm-up time for the power supply is 20 minutes, and the intensity stability after this time is good. The lamp output is collimated by a parabolic focussing mirror and a collecting

lens. The slightly diverging beam is reflected through a path of approximately 50 cm to the solar cell mounting fixture. The beam diameter at the plane of the solar cell is 5 cm. An area of 4 cm^2 at the center of the beam has uniform intensity to within 3 %. The simulator spectrum matches approximately the terrestrial solar spectrum, as depicted in figure 2.5, the spectral data published by the system vendor [17].

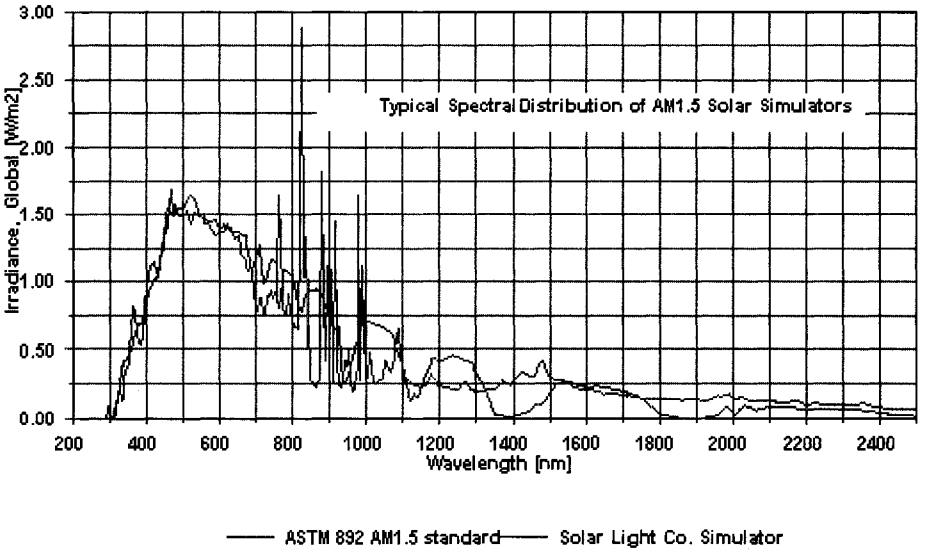

Figure 2.5: Spectrum of the solar simulator bulb compared to AM-1.5 terrestrial solar spectrum. The solar simulator gives a fairly faithful reproduction of outdoor illumination conditions, especially for $\lambda < 840$ nm, where CdTe solar cells respond to illumination.

A typical J-V measurement adheres to the following procedure: after the warm-up time has elapsed, an NREL-calibrated reference cell is mounted into the system at the center of the illumination area. The current supplied to the simulator lamp is adjusted until the photocurrent of the reference cell matches the calibrated value for one-sun illumination. The test cell is then mounted into the test fixture with connections as indicated in the schematic of fig. 2.4. An applied voltage bias (from a Keithley 230 programmable voltage source) is swept from a moderate negative value to an open-ended positive voltage. The maximum voltage is limited by a user-specified current threshold, after which, the voltage source is re-programmed to zero applied bias. Current and voltage are independently monitored by separate HP 34401A multi-meters, and all instrument settings and data acquisition are

computer controlled via GPIB connection and in-house programmed LabView® software. Standard temperature of 25 ±0.5°C is maintained during measurement using flowing boil-off gas from a liquid nitrogen dewar, and measured using a type-T thermocouple in direct contact with the device substrate. Sample dark and illuminated J-V data is given in fig. 2.6

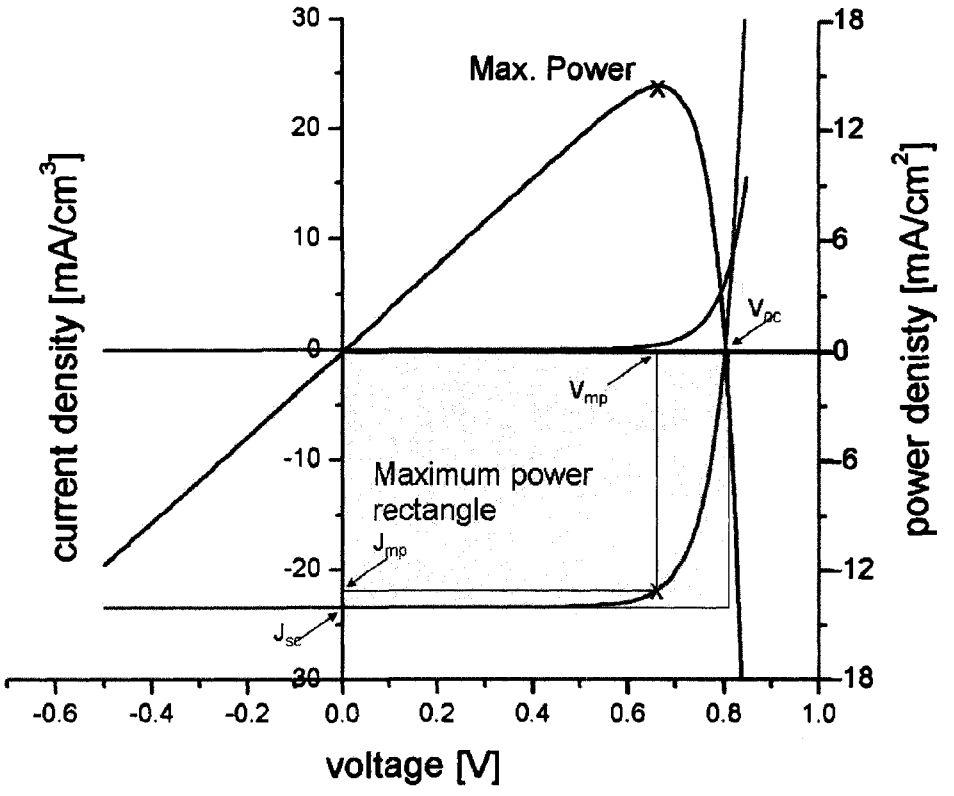

Figure 2.6: A typical J-V curve in dark (black) and light (red) for a CdTe thin-film solar cell. The power output (blue, right hand axis) is the figure of primary interest for solar cell efficiency.

Nonstandard methods of J-V measurement give further information about the device and materials, and include varying the light intensity or spectrum using optical filters, and J-V at T $\neq$ 25°C, usually by using increased N_2 flow to reduce the temperature.

Interpretation of measured data

The solar cell efficiency η is often represented in terms of other measurable parameters indicated in the figure. The short circuit current J_{sc} is the current that would flow if the illuminated cell were shorted with a wire. The open circuit voltage is the voltage drop that would occur if the illuminated solar cell were connected to an infinite load. For load resistances between zero (the wire) and infinity, the cell response traces out the red curve in the fourth quadrant. At some point, the product of current and voltage reaches a maximum. The blue curve in fig. 2.6 shows the output power as a function of voltage. The peak of the curve represents the maximum power output of the device and this value divided by the incident radiative power yields the device efficiency η. Mathematically,

$$\eta = \frac{Output\,power\,density}{Incedent\,power\,density} = \frac{J_{mp}V_{mp}}{100\,mW/cm^2} = \frac{J_{sc}V_{oc}FF}{100\,mW/cm^2} \tag{2.5}$$

where J_{mp} and V_{mp} are the maximum power current density and voltage, as indicated in the figure, J_{sc} and V_{oc} are the short circuit current density and open circuit voltage described by the axis intercepts, and FF is the *fill factor*, indicated in figure 2.6 as the ratio of the areas of the two rectangles shown.

The dark curve can be readily fit to the diode equation,

$$J(V) = J_o(e^{\frac{qV}{AkT}} - 1) \tag{2.6}$$

where J is the current density, J_o the diode saturation current, V the applied voltage, T the absolute temperature, q the elementary charge and k is Boltzmann's constant. A in this context is the *diode quality factor* which serves as an indicator of the mechanisms by which injected electrons recombine with holes.

When light is applied, photogeneration occurs mainly in the space-charge-region, and charges are swept apart by the built-in electric field. The light-generated current flows in the reverse direction from the diode polarity, in accordance with the potential gradient in fig. 2.3. In essence, the solar cell acts as a d-c current source. The ideal diode curve from

equation 2.6 becomes shifted by the amount of light-generated current J_l and the resulting behavior is described by

$$J(V) = J_o(e^{\frac{qV}{AkT}} - 1) - J_l \tag{2.7}$$

which was used to calculate the curve in figure 2.7(a). The current-voltage relationship for thin-film solar cells often differs from the ideal diode equation due to the presence of parasitic resistances and the influences of non-standard elements, such as variations in the main junction and back-contact barriers. All of the resistive elements present—bulk resistivity of the semiconductor, contact resistance, ohmic pathways between front and back contact, sheet resistance etc.—are lumped for convenience into two quantities, series and shunt resistances. The diode equation becomes:

$$J(V) = J_o(e^{\frac{q(V-JR_s)}{AkT}} - 1) - J_l + \frac{V - JR_s}{R_{shunt}} \tag{2.8}$$

where R_s is the lumped series resistance and R_{shunt} is the shunt resistance. The effects of series and shunt resistances are depicted in figure 2.7, curves (a) and (b). Back contact barriers are a major theme of chapter 3, and will be discussed there. With the effects shown in fig. 2.7 in mind, one can identify obvious problems in the device behavior on inspection of an illuminated J-V measurement.

For the work of this thesis, determination of J_o is of prime importance. It can be obtained from the J-V curve in a couple of ways. One may use a curve fitting routine (based on least squares, for example) to fit an experimental dataset to the full diode equation 2.8. More often, one rearranges the diode equation to obtain

$$ln\left(J + J_{sc} - \frac{V}{R_{shunt}}\right) = ln(J_o) + \frac{q(V - JR)}{AkT}. \tag{2.9}$$

If the left side is plotted against $(V - JR)$ for the range of values with $V > V_{mp}$ and a linear fit made, J_0 is the y-axis intercept of the graph, and the diode quality factor is obtained from the slope of the line [18], as in figure 2.8.

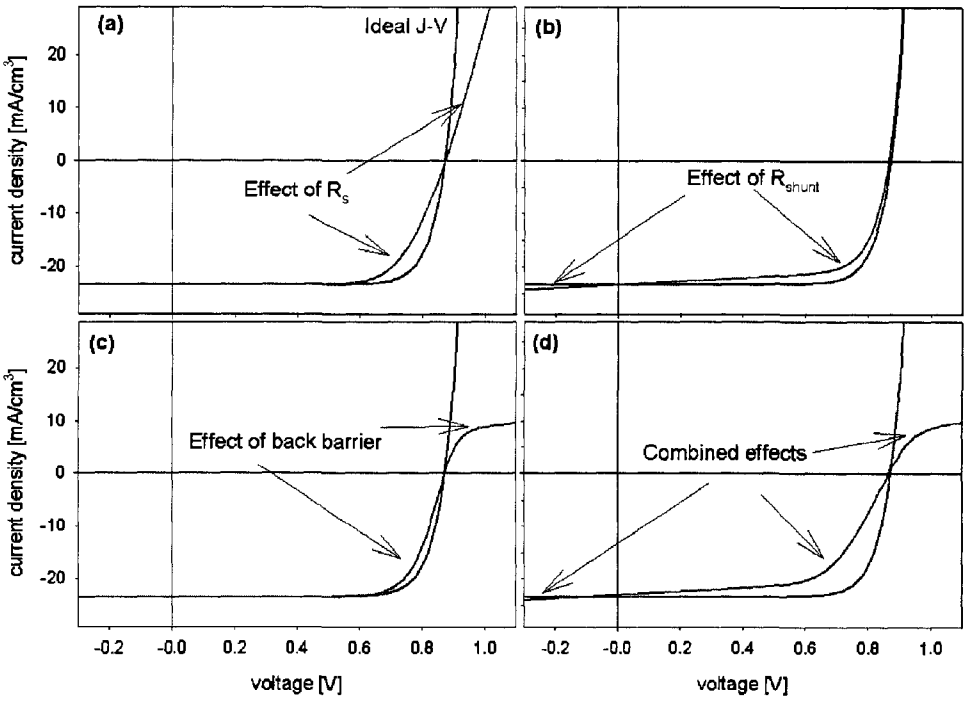

Figure 2.7: Simulation of an ideal illuminated solar cell J-V curve (black) develops linear slope components in the forward-current (a,d) and photocurrent (b,d) regimes due to series and shunt resistances. These tend to reduce the device fill-factor and efficiency, while not strongly affecting J_{sc} or V_{oc}. A back-contact Schottky barrier causes rollover in the first quadrant (c,d) and fill-factor loss.

2.2.2 Quantum Efficiency (QE)

Quantum efficiency measurements allow specific identification of photocurrent losses. The quantum efficiency is defined as the ratio of electron-hole pairs generated to photons available. As opposed to basic photocurrent measurement, QE is photocurrent resolved as a function of illumination wavelength.

$$QE(\lambda) = \frac{current\ out}{photon\ flux(\lambda)} \tag{2.10}$$

In-depth analysis of QE data can yield estimates of layer thicknesses [19], and some information about minority carrier diffusion lengths [14] can be inferred. Also, one can get information about the form of the collection function from study of the changes in QE under various test conditions of voltage and light bias. [5]

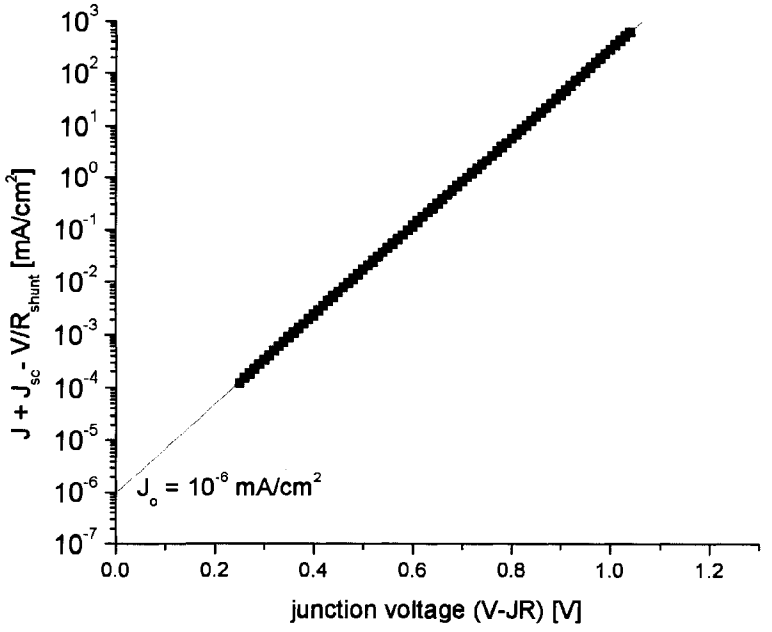

Figure 2.8: Linear extrapolation of the semi-log plot yields the diode saturation current, while the slope indicates the dominant forward current mechanism.

Measurement procedure

The light source used to obtain the monochromatic excitation is a 240-W tungsten halogen bulb, as is common in overhead projectors. Light from this source is directed through the entrance slit of an Acton Research model SP-150 monochromator. The monochromator grating with 1200 g/mm and exit slit dimension are selected to achieve a monochromatic beam with linewidth ~2 nm over the spectral range of interest, $380 < \lambda < 900$ nm. A pause is allowed during wavelength scanning to allow for insertion of an optical cut-off filter, which prevents distortion of the excitation beam from second-order fringes of half-wavelength. The monochromatic beam is then mechanically chopped at a frequency of 151 Hz, collimated by a 100-mm focal length lens, and then focused onto the solar cell with a second lens. The cell is illuminated with a dc broad spectrum light source at an intensity of $\sim 1/4$ terrestrial solar power density. The ac current produced by the monochromatic beam is detected by an SR570 current-to-voltage preamplifier. The preamplifier converts the ac current signal from the cell to an ac voltage signal. The SR570 is also employed to apply dc voltage bias, and

compensate (or filter) dc response from the cell. An SR810 model lock-in amplifier, locked to the frequency provided by the mechanical chopper, detects the voltage signal from the preamplifier. As with the J-V measurement, all instrumentation control and data handling are computer-automated.

Two quantities must be precisely known to generate an accurate ratio for eq. 2.10. The first is the photon flux. The spectrum of the source bulb is weakly dependent upon the supply power when it is operated near the 240-W prescribed level. Nevertheless, sufficient inaccuracies are introduced resulting from variations in the way the user sets the power supply, and the age and operating temperature of the bulb, that a reliable spectrum cannot be assumed from one session to the next. It is thus necessary to calibrate the illumination spectrum prior to using the system. A stable and encapsulated monocrystalline Si device was calibrated at NREL to be used as a QE standard. Scanning the desired wavelength range with this reference device of known QE(λ) in the test fixture establishes the photon flux at each wavelength. This flux is then assumed during investigation of the test device. Calibration protocol requires that this step be performed twice, with a time interval on the order of the measurement, and a stability of response $< 1\%$ to ensure that the light source is stable for the subsequent experiment.

The second quantity of interest is the measured current. However, the conditioning and sensing electronics are of a sufficient sensitivity that electronics inaccuracies are insignificant compared to the calibration procedure for the photon flux, and they will not be discussed here.

Non-standard QE measurements, which yield useful information include especially QE with an applied dc voltage bias, as this can give information about changes in the collection efficiency, as a function of both voltage and wavelength.

Interpretation of QE data

The astute reader will have noticed that the quantities involved in the ratio described in eq. 2.10 are not necessarily those obtained using the procedure outlined above. In particular, the photon flux inferred from the calibration step, while it may indeed be a reasonable representation of the spectrally resolved intensity of the source bulb, only accurately repre-

sents the photons available to the cell insofar as none of those photons are lost to reflection, incomplete absorption in the base layer or absorption in any overlayers not participant in the solar cell operation (i.e. glass). We distinguish between *internal* and *external* quantum efficiency to account for these losses. The current measured by the instruments most correctly corresponds to the external QE. Measurement of reflection and application of models for extraneous absorption, transmission and incomplete collection of photogenerated carriers allows one to back-calculate to the internal QE. Practically speaking, a measurement of the transmission through a comparable glass/TCO layer to that used for the cell deposition allows one to infer the internal QE when plotted simultaneously to the external QE data. A graphical presentation of a typical QE measurement is shown in figure 2.9.

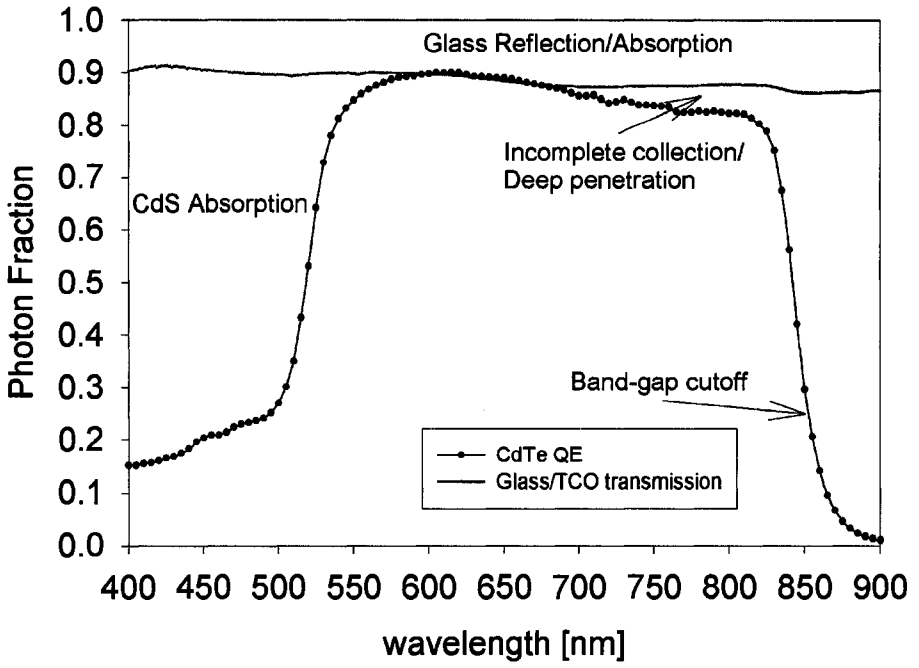

Figure 2.9: Analysis of QE data allows specific identification of current losses, and gives hints as to the mechanisms of the loss.

In addition to the reflection and glass/TCO absorption loss, substantial useful information is available in an accurate QE curve. Moving from right to left across the graph, the first feature to note is the null result for long wavelengths. This is a direct manifestation of the light absorption characteristics mentioned above. Photons with energy much less

than E_g cannot excite an electron hole pair and thus no photocurrent is generated from illumination in this portion of the spectrum. The steep rise corresponds to the average absorber band gap. The absorption coefficient is wavelength dependant, such that lower energy photons will have a longer penetration length before the probability of absorption is high. CdTe cells typically exhibit a discrepancy between the EQE and the transmission curve for the glass/TCO at longer wavelengths, and this is a result of the combined deep or even incomplete absorption of those photons and the collection characteristics of the solar cell.

As mentioned previously, photogenerated carriers in the CdS window layer tend to be poorly collected, which is obvious from observation of the short ($\lambda < 500$ nm) wavelength region. To improve the device current, the CdS layer is made fairly thin, such that even despite the large absorption coefficient, as much light as possible passes through to the CdTe where the generation and collection of carriers is very efficient. If one assumes no response from absorption in the CdS layer, the thickness of the layer can be deduced from the QE in this region. The average CdS thickness is calculated from

$$QE(\lambda) = QE_{D_{CdS=0}} e^{-\alpha(\lambda)z} \tag{2.11}$$

where α is the wavelength dependant absorption coefficient of polycrystalline CdS, z is the thickness of CdS, and $\mathrm{QE}_{D_{CdS=0}}(\lambda)$ is the hypothetical QE if there were no CdS absorption. Note in fig. 2.9 that for wavelengths just longer than those absorbed by CdS, the glass/TCO transmission and device QE add to unity. It is assumed that the CdTe IQE is unity over all wavelengths smaller than the onset of the deep penetration loss, so in practice $\mathrm{QE}_{D_{CdS=0}}(\lambda)$ is the same as the transmission curve in the $380 < \lambda < 500$ nm range.

2.2.3 Capacitance

As discussed earlier, the internal electric field in the solar cell is developed because of diffusion and annihilation of free charge carriers between the n- and p-type sides of the device. The resultant depleted volume can be approximated as a parallel plate capacitor,

with the edges of the depletion region as the plates. Its capacitance is given by

$$C = \frac{\epsilon_s A}{d} \tag{2.12}$$

where ϵ_s is the dielectric constant of the semiconductor, A the area and d the separation between the plates.

Careful measurement of solar cell capacitance and some physical interpretation of the results yields information about the carrier density in the absorber material, the built-in potential, and the depletion layer of the cell. Sometimes this information also alludes to the thickness of the absorber layer.

Capacitance measurement

Solar cell capacitance is obtained using an HP4192A LF impedance analyzer. For the measurement, the cell is held at a user-defined dc bias level by a Kiethley 230 power supply and cell voltage is monitored by an HP33401A digital multimeter, as well as the impedance analyzer. When a parallel dc current flows either through an ohmic shunt in reverse bias, or through a shunt or because of the diode current in forward bias, independent monitoring of the bias level is necessary, as the analyzer voltage can differ substantially from the actual cell bias. The dc bias level is varied over a user specified range, typically -2 V to $+0.2$ V. At each dc level, the current response to an ac voltage perturbation of 20 mV is measured. The out of phase component of the current response is related to the cell capacitance.

Prior to the capacitance-voltage (C-V) measurement, the response of capacitance is measured at a few dc bias levels as a function of the frequency of the ac signal. For well-behaved devices, there is typically a range of frequency where the capacitance is independent of frequency, and the phase angle of the response is large, or at least 20°, meeting the requirement for accurate data acquisition established by Mauk *et al.* in [20]. The frequency sweep range for the capacitance-frequency measurement and the voltage range for the C-V are pre-programmed so that the measurement is completely automated and the data is gathered to the computer, as with J-V and QE, by LabView® software.

Information obtained from capacitance measurement

In a CdS/CdTe solar cell, the CdS is much more heavily doped, so virtually all of the depletion width is in the lightly p-type CdTe layer as indicated in figure 2.3, and the entire depletion width may be approximated by equation 2.4. The plate separation, d from equation 2.12 is interpreted as the depletion width in the CdTe layer, which responds to applied voltage according to

$$W = \sqrt{\frac{2\epsilon_s(V_{bi} - V)}{qN_a}} \tag{2.13}$$

Combining equations 2.12 and 2.13 results in an expression allowing interpretation of capacitance data:

$$\frac{A^2}{C^2} = 2\frac{(V_{bi} - V)}{q\epsilon N_a} \tag{2.14}$$

with the voltage intercept equal to the built-in potential. Furthermore, it is evident from 2.13, that the depletion width varies with voltage, such that the carrier concentration (N_a) can be calculated as a function of position of the depletion edge, from the slope along the curve of A^2/C^2. Two plots, then, can be generated from a C-V measurement, as shown in fig. 2.10. When describing a solar cell model, or calculating the band-diagram, it is common to treat the absorber carrier density as a constant in the position. The carrier density plots of figures 2.10 and 2.11 clearly indicate that this is not the case. Most often there exist higher densities of compensating defects near the front and rear interfaces, so that the carrier density rises somewhat in the middle of the absorber. Changes in carrier density on the order of 2-8 % alone do not strongly affect the band structure and idealized operation of the cell, but the implied defect densities can be responsible for reduced performance through higher recombination.

For thin CdTe absorbers ($\sim$ 2.5 μm), the free-carrier density multiplied by the layer volume is often too small a total charge for the diffusion process of the p-n junction formation to go to completion. Fully-depleted devices will show very little variation of capacitance with voltage, since the only parameter of eq. 2.12 that changes with voltage should be d, and the depletion width—already extending to the metal contact—cannot expand into the absorber with reverse biasing. This effect is manifest in the C-V and p vs. position curves

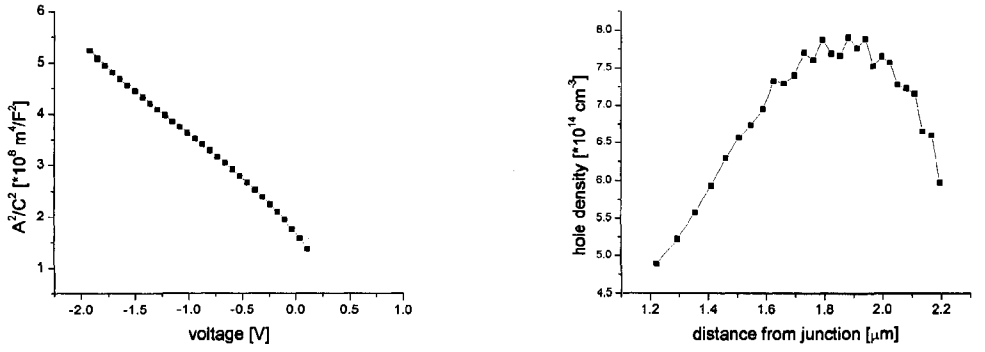

Figure 2.10: A^2/C^2 for a well-behaved device decreases with increasing voltage because the depletion width reduces with bias. The carrier density is obtained from the slope of the A^2/C^2 graph.

as shown in figure 2.11.

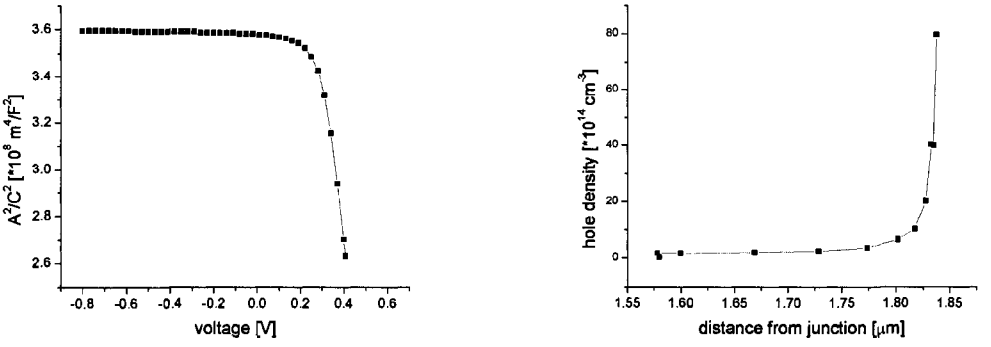

Figure 2.11: A thin absorber might be fully depleted, so that the depletion width cannot respond to voltage bias. Apparent carrier densities are often skewed in this situation.

The steep increase in apparent carrier concentration observed in figure 2.11 is usually interpreted as arising from the back surface layer of the CdTe absorber or perhaps the metal contact. Such a measurement is difficult to interpret in terms of the bulk carrier density, since the variation is so great, but it allows an estimation of the device thickness and acts as an existence proof for the full-depletion condition.

2.2.4 Light-Beam-Induced Current (LBIC)

The characterization tools described to this point share the common feature that they provide information about the average performance of a solar-cell. However, a hallmark of

the fabrication methods used for thin-film solar cells is that there is almost always some variation in the layer parameters—thickness, defect density, grain size, material intermixing etc.—over the deposition area. The LBIC measurement enables detection and characterization of some of these non-uniformities so that steps may be taken to minimize them.

The LBIC apparatus at CSU consists of four interdependent systems: a mechanical system, an optical system, an electrical system, and a computer interface. The measurement consists of scanning a focussed laser beam over the device area and measuring the photocurrent at each position. Local changes in photocurrent represent differences in quantum efficiency at the laser wavelength. These changes can often be traced to specific kinds of defects and translated to variations in the energy band structure.

LBIC system

Five separate diode lasers with lasing wavelengths of 638, 685, 788, 823, and 825-857 nm (tuneable with temperature), form the heart of the optical system for the LBIC measurement. They are powered by a ThorLabs LDC500 diode controller, which supplies a baseline dc power level, with a small amplitude ac component for lock-in detection. Each laser has a specific combination of control settings for use and the reader is directed to [21] for details on this and other aspects of the LBIC system. Each laser diode is pigtailed into a single-mode fiber, which, when selected, is routed into an OZ Optics DD-100 fiber based attenuator. The attenuator can control the intensity throughput reliably over four decades, so that the spot size can be varied while a constant illumination power density is maintained. The output from the attenuator is then collimated and polarized, sampled by a monitor photodiode, and steered to the experiment. At the experiment, the beam is focussed to the desired spot size using an Olympus 1-UB367 SL C Plan Fluoride 40x/0.55 N.A. objective. This unit includes a correction collar for reducing abberations that arise when multiple refractive indices are present between the objective and the desired focus point, as when focussing through a glass superstrate onto a solar cell.

The electrical response of the test sample is monitored with the same electrical setup as the whole-cell QE measurement. The photocurrent is amplified and converted to voltage by the SR570 preamplifier, which also provides a dc voltage bias when it is desired and sinks

away the dc current response from the cell. The ac component is then sent to the SR810 lock-in amplifier. The QE of each individual photocurrent measurement is established by comparing the cell lock-in response to that of the calibrated monitor photodiode, whose response is tracked in real-time with the measurement by a second lock-in amplifier on an IOTech DAQ2000 board. The computer software uses the two measured responses, the monitor diode calibrated QE at the laser wavelength and the known beam-splitting ratio of the sampler to calculate the device QE at each position, so that a 2-D map of photocurrent response is generated. The system also features a second photodiode mounted in the opposite optical path as the monitor photodiode, which picks up the reflection signal from the cell surface.

The mechanical system consists of three Newport stepper motors, which feature sub-micron precision and repeatability. Two stages are combined in an orthogonal piggy-back configuration to form an x-y plane. Devices are characterized by probing in a custom mount affixed to the x-y plane and translation under a constant radius focussed laser beam. Since the plane of the solar cell is rarely orthogonal to the axis of the laser beam, the focussing objective is mounted on the third stepper stage such that the objective axis is collinear with the beam axis. Prior to measurement, the plane of the cell is established and programmed to the stage control. In this way, a constant focused spot size is maintained during the measurement. The mechanical stages can be individually controlled from the computer interface, enabling line-scans, and various system calibration processes.

A full description of the LabView® software, which was programmed to run the LBIC experiment is available in [21]. Various augmentations have been made by subsequent users to enhance the data-processing scheme, attenuator and translation-stage control. The main interface of the program includes control of the three translation stages, the light attenuation, and access to interfaces for controlling the preamplifier and lock-in settings. Sub-routines, opened from the main interface, allow the user to calibrate the attenuator controls, the calculation of the incident power density from the monitor diode response, the cell plane, and various properties of the beam alignment and angle. A final sub-program allows the user to set up and run default or custom geometry 2-D scans. In the course of this work the LabView routines for stepping of position during scanning and for beam

alignment were to some extent re-written in order to maintain accuracy of the system in response to effects of wear and tear after five years of use.

LBIC technique

The procedure used for the LBIC measurements presented in this thesis was developed to ensure reproducible and accurate data, and as described here is specialized for measurement of CdTe solar cells, though some aspects would generalize well for use with CIGS cells.

The cell is contacted in the cell-mount with two front-contact probes and two for the back-contact. A small disk of indium metal is typically inserted between the back-contact probes and the solar cell to prevent damage to the back-contact. The superstrate structure of the CdTe devices allows for complete contacting on the 'back' surface of the glass, and eliminates shadowing due to contact probes. One set of probes is connected to an HP34401A digital multimeter to monitor dc bias on the cell, so that it can be compensated with the preamplifier. The other connection is routed to a switchbox, which selects between the cell response and the reflection photodiode for the preamplifier input.

With the cell response selected, the edges of the cell are determined, and the experimental coordinate frame is established by scanning in the x and y directions to the edges of the cell, locating the center of the device, and declaring the coordinate middle of the intended scan area. Next, the cell plane is established using the reflection from the glass surface. A last preparation step is locating the objective position corresponding to the minimum spot size, by repeatedly resolving a feature of the solar cell response at the diffraction-limited highest resolution (~ 1 μm).

Once the cell dimensions and plane, laser-spot size and attenuation are determined, the acquisition scan may be initiated. The measurement proceeds automatically with a command loop in three steps. (1) a step of 1/2 the size of the spot radius is made, and the objective position is adjusted according to the cell plane to keep the spot size constant at the cell. (2) the translation stage reports its position and this number is checked against the desired final position. If the stage has not achieved the desired position, the loop begins again with step (1). (3) the measurement of cell response is made.

Scans are made at three 'standard' resolutions—defined by the spot radius—of 100 μm,

10 μm, and 1 μm. Typical scan sizes are 5 mm x 5 mm for the low resolution, 500 μm x 500 μm for middle resolution and 50 μm x 50 μm for high resolution. For any of these standard configurations, the result of an LBIC measurement is 10201 independent measurements of the device photocurrent, each ascribed to a specific position.

2.2.5 Interpretation of LBIC data

Two complimentary methods of representation for LBIC data have been developed to extract as much useful information as possible from the experimental results. 2-D photomaps show whether the device area contains micro-defects, where they are, and to a degree, what may cause them. Histograms lose the spatial information, but give an unambiguously quantitative basis for comparing device uniformity.

'Reading' LBIC photomaps

The photocurrent at each position can be converted to the QE, and organized into a 2-D map of device QE as in figure 2.12. The black, zero-response area is outside the cell perimeter, and the cell edge shows a rise from zero response to a plateau at the cell QE over the space of approximately twice the spot size. By local convention the range of QE is distributed over a scale of eight colors and the range of QE for each color is selected so that the dominant color shown is the central green. As with the scanning protocol, a set of standard contrast levels has been developed to represent the data for different levels of device uniformity. Standard contrast uses a 2 % color scale, which makes moderate non-uniformities apparent. Local defects on devices with good uniformity are made more visible using a 1 % color scale, denoted 'high-contrast'. Devices with pathological defects will often show large variation in local QE. Under 'low-contrast', a 5 % color scale is chosen so that in all but the most severe cases, the full range of QE values may be displayed in the range of colors. It is frequently helpful to view the same data set under multiple contrast levels, because a single cell may contain defects of varying severity. A sample of data at the different resolutions and contrast levels is shown in figure 2.13.

Specific determination of the electrical nature of a feature seen on an LBIC photomap is often possible using multiple scans of the same area under varying conditions. Isolation

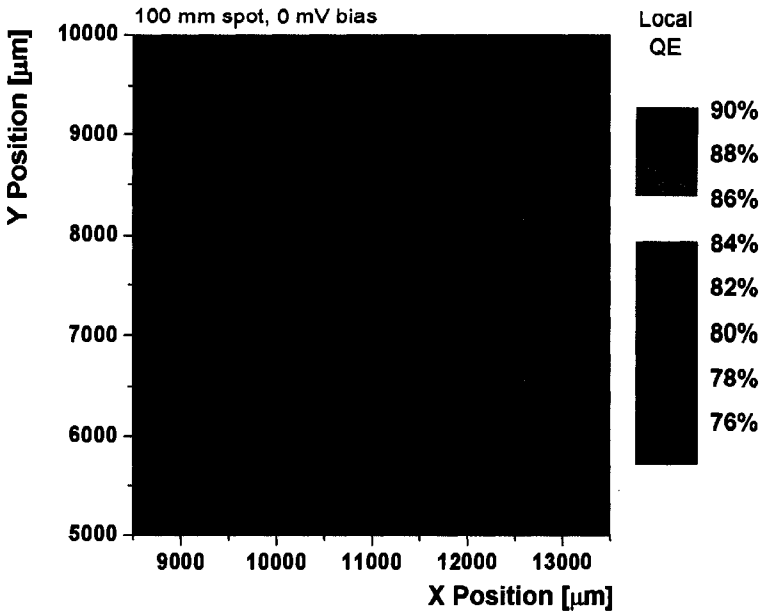

Figure 2.12: 5mm x 5mm LBIC scan field of a CdTe solar cell. The 2-D photomap representation emphasizes defective areas of the solar cell, such as the lower right triangular section of this device.

of optical features such as spatial variation in surface reflection is also possible. These interpretations of photmaps will be demonstrated in the later chapters.

'Reading' LBIC histograms

The calculated QE of each of the 10,000+ measurements of a typical scan can be binned according to value, usually within $0.1, 0.2$, or 0.5 % increments to generate a statistical distribution of the scan results. A sample of the resulting curve, for the scan of figure 2.12 is given in fig. 2.14.

The X-axis in the figure 2.14 corresponds to the calculated QE for each measurement. The Y-axis is the percentage of datapoints where the QE fell within the bin-width chosen for the distribution. A few points of particular interest are identified in the histogram. First, the distribution is usually a somewhat peaked function of QE. The location of the peak is the mode QE for the device, and in most cases corresponds fairly closely to the value one obtains with a full-cell QE measurement. The second quantity of interest is the

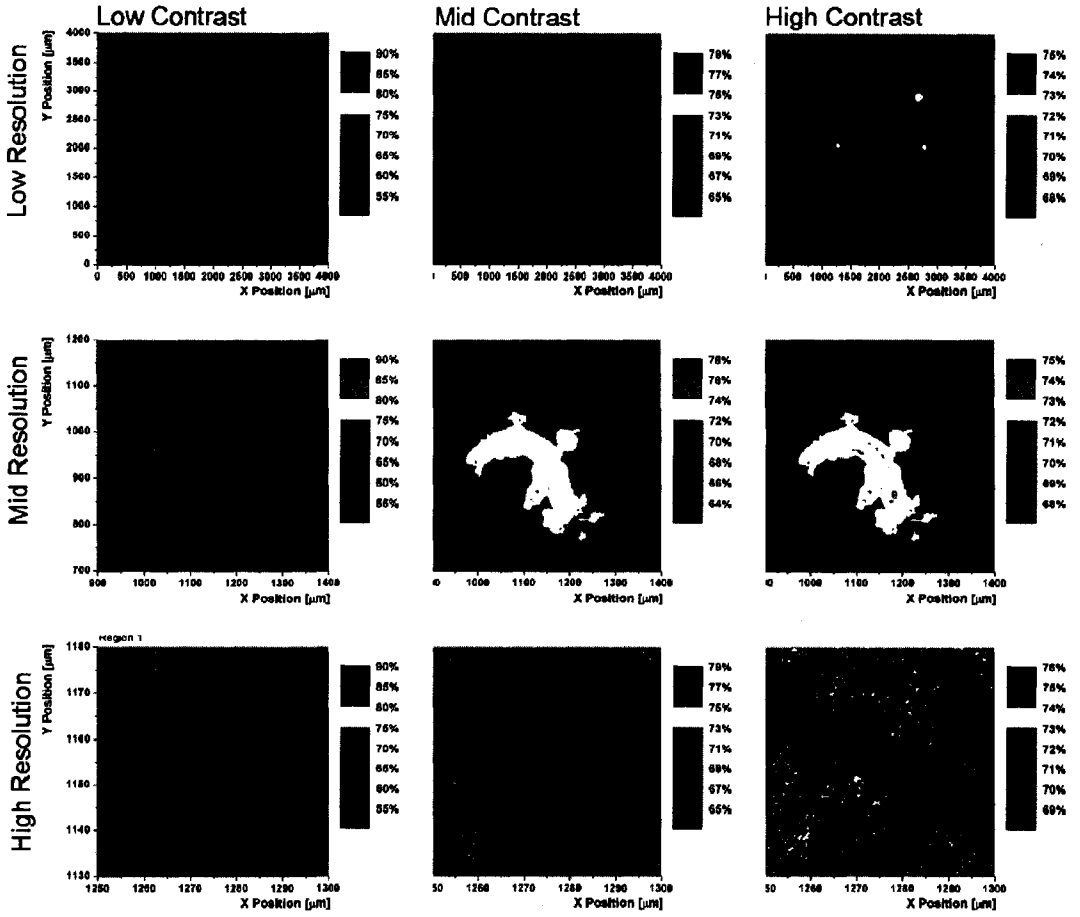

Figure 2.13: LBIC measurement results on CdTe at low, mid and high resolutions, presented with various color contrasts. The high-contrast figure emphasizes the size/shape of defects, while the low-contrast singles out the most severe areas.

width of the distribution at half the peak value. The full-width at half-maximum (FWHM) of histogram distribution is the quantity typically taken to make quantitative comparison of the uniformity of devices. As will be shown in chapter 5, one occasionally finds a device which has poor collection (a low mode-QE), but good uniformity (small FWHM, or narrow peak), although the more common combinations are low-mode QE/large FWHM and high-mode QE/small FWHM. Finally, there are occasions when the histogram is somewhat double-peaked, and because of the area ratios of the two average responses, one peak will not contribute to the FWHM. In these cases it is important to consider the total range of QE values measured.

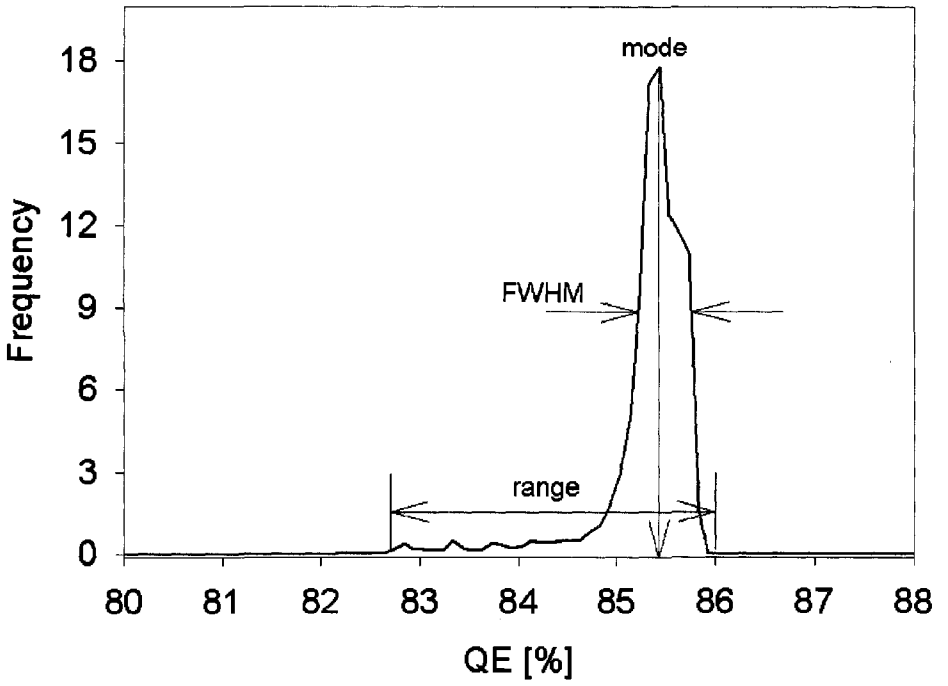

Figure 2.14: The mode, FWHM and range of the histogram distribution allow relative classification of device uniformity.

The reader will also notice that the distribution in fig. 2.14 is not symmetric. The shape arises because most of the non-uniformities one observes cause reductions in the photocurrent collection, and the high end of the distribution is physically limited by the EQE of the material in question. A perfectly uniform device would give a δ-distribution at the device QE for the chosen excitation wavelength. Non-uniformities typically only reduce the response, so as a device becomes less-uniform, a tail develops on the low side of the peak QE.

Each point within the scan area is sampled an average of twelve times, except for points on the edges, so that in the photomap, as well as in the histogram, there is a smooth transition between the QE plateau and the non-uniform spot. To develop a sense for interpretation of histogram distributions, let us consider a device with distinct regions of two QE values: a high QE (QE-1) and some lower value (QE-2). There are three possibilities for each individual measurement: (1) the laser spot is completely contained within a region

of QE-1, (2) the laser spot is completely contained within a region of QE-2, and (3), the spot partially overlaps both regions. If the characteristic defects for a given device are smaller than the laser spot, then only possibilities (1) and (3) remain. It can be shown that a random distribution of low-response spots smaller than or equal to the beam size and totalling ~ 8 % of the scan area will cause virtually every datapoint to have some influence away from the ideal QE value, since part of the beam area will contain some or all of one such spot. The distribution will tend towards a gaussian shape, with the peak shifted down in QE from the uniform case. The more common result, which bridges delta- and gaussian-function regimes can be described by a peaked function with an exponential decay tail towards lower QE values. The sharp peak arises from those areas not affected by non-uniformities, and the shape of the tail comes from the larger number of measurements affected by only part of the defect area, than those containing the entire spot. If the defects are larger than the beam size, one may observe two peaks, with inside-tails. Often the separation of QE's in a cell with multiple modes is fairly minor, such that there is significant overlap of the distributions corresponding to QE-1 and QE-2. Of course, this is an idealized approach to histogram interpretation, and real devices tend to have more than two possible QE values, and a variety of sizes of defects, but this approach has been somewhat successful in guiding interpretation of histogram distributions.

One can apply a fit to many histogram distributions of real devices using an empirical function of the form

$$y = \frac{A}{w\sqrt{\pi/2}} e^{\frac{-2(x-x_g)^2}{w^2}} + \frac{B}{1+e^{R(x-x_d)}} e^{\frac{x-x_d}{t}}. \tag{2.15}$$

The first term in the equation corresponds to the gaussian distribution influence, while the second term identifies the sharp peak and exponential tail. The parameters of eq. 2.15 do not uniquely indicate one physical phenomenon or another, but they can be interpreted to help understand the severity of variations in photocurrent response. From the exponential decay part, the location of the step x_d corresponds to the maximum QE the device can provide, while the decay constant t gives an indication of the frequency with which the beam is only partially over a defective spot. The factor R describes how steep the cut-

off step is. R is usually large, indicating an abrupt decrease to zero in the number of measurements with QE larger than x_d, but not always. The prefactors A and B normalize and indicate the relative contributions of the exponential decay and the gaussian parts and can loosely be thought of as indicating the fraction of "good" and "bad" areas at least the order of the beam size. The center x_g of the gaussian part of the fit can be used to obtain an average QE. That is; once one has estimated the defective area, i.e. from the photomap, and using x_d for the maximum QE, the average defect QE value is the missing quantity necessary to calculate the observed gaussian center. The width w of the gaussian can be interpreted as an indicator of the shape of the 'walls' of the defect areas. It should be noted that several of the parameters here are bound to one another. For example, the center of the gaussian and the peak of the decay should not differ by more than the combined widths of the two distributions. However, pathological cases do exist in which the solar cell has multiple distinct regimes of performance coexistent on the surface area. For this reason, it is important to use both representations of LBIC data complimentarily. One could puzzle for a long time over a histogram that doesn't conform to the fitting and interpretation presented here, where inspection of the photomap would immediately give visual clues to an unusual non-uniformity behavior.

Putting it together

As with the photomaps, new information comes out of the histograms when one performs multiple scans of the same area under different conditions.

Consider the device from figure 2.12, with expanded analysis plotted in figure 2.15. The photomap on the left is the same as figure 2.12. The histogram of that scan, ignoring the dark regions outside the cell perimeter has been included. The second image and histogram are for the same cell and scan area, but with a 600-mV dc-voltage bias applied. From the photomaps is apparent, that there are essentially two areas of independently uniform response, and that the transition from one area to the other is fairly sharp. This is reflected in the histogram. The FWHM of the peak representing the dominant area of the cell changes little between zero bias, and approximately the maximum-power voltage. The implication is that the junction is quite uniform and that the collection—although it does

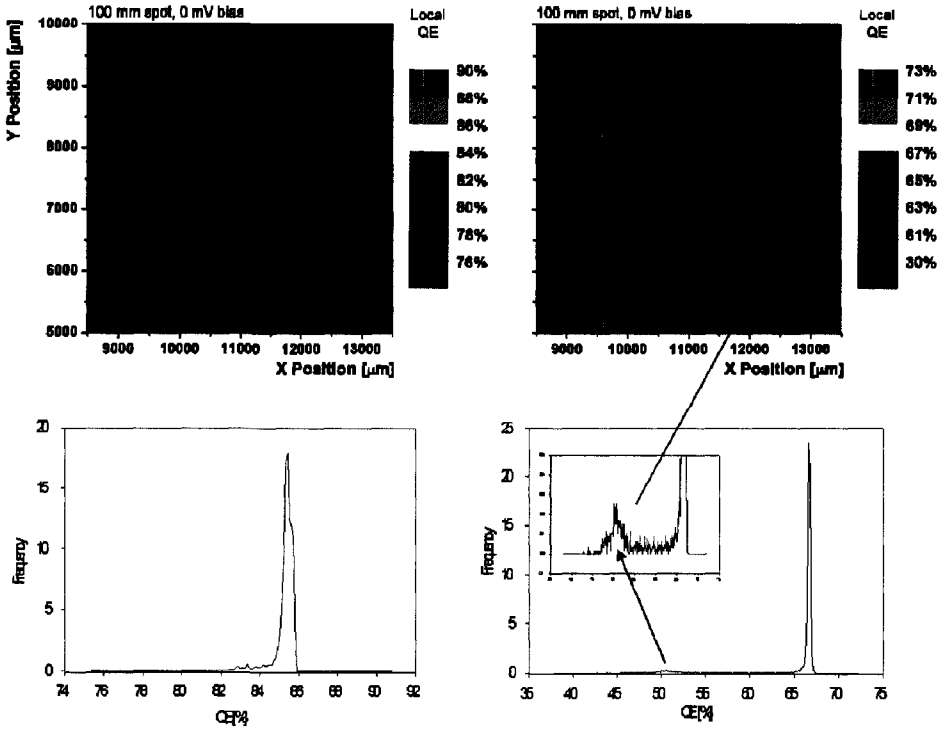

Figure 2.15: The FWHM of the main cell area is about 2 % at zero bias and in forward bias. The low response area also maintains its FWHM—about 3 %—but it shifts dramatically from the shoulder of the main peak (zero bias) to a second individual peak (forward bias, inset) indicating that this area has a much stronger voltage dependance for the collection efficiency than the rest of the cell.

decrease somewhat—does so uniformly. The lower right region of poor collection decreases in photocurrent more significantly at the increased voltage bias, but still uniformly. The small secondary peak in the histogram indicates that this area exhibits a high degree of internal uniformity. From the data shown, one could conclude that the band-bending in CdTe is less in the 'bad' region, because for the same voltage bias, the collection has decreased more in this region than the main cell area.

2.2.6 Device modeling and equivalent circuit software: AMPS-1D and PSpice

The whole-cell measurements described above can lead to a model for the device behavior, which may then be assumed to vary when LBIC data indicates lateral non-uniformities are present. Numerical calculations of band structure and predicted device performance can be

useful to verify the consistency of the suspected model with measurement, and to further develop the context for LBIC interpretation.

AMPS-1D

Analysis for **M**icroelectronic and **P**hotonic **S**tructures in 1-**D**imension (AMPS-1D) was developed by Professor Steve Fonash and colleagues at Penn St. University to do numeric calculation of the basic semiconductor equations. It allows the user to develop a band-diagram and simulate J-V and QE curves for a given set of parameters. A full description of the features available is given in the AMPS manual [22]. The program takes a user-defined grid of positions throughout the generated device and at each one solves the basic semiconductor equations in one dimension: Poisson's equation,

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho}{\epsilon_s}, \tag{2.16}$$

and the continuity equations for electrons and holes:

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\frac{\partial J_p}{\partial x} \tag{2.17}$$

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\frac{\partial J_n}{\partial x}. \tag{2.18}$$

The electrostatic potential (φ) at each point yields the energy-band diagram as a function of position in the device. In steady state, at a number of selected non-equilibrium conditions, the numeric solution of this system of coupled equations determines the current flow for holes and electrons J_p, J_n based on the generation and recombination rates G_p, G_n, U_p, and U_n.

Orcad PSpice Student

PSpice calculates the response of a circuit containing a variety of linear and non-linear elements to a given stimulation. For application in this work, the solar cell junction is replaced with a diode in parallel with a dc-current source. A basic solar cell equivalent circuit was given in figure 2.4 above. The user specifies the diode parameters of saturation

current, internal series resistance, quality factor, and reverse characteristics. Where PSpice is used in this work, diode parameters obtained from measurements and AMPS simulations are used as input parameters, and then scaled guided by results from LBIC measurement.

Chapter 3

Effects of non-uniform back contacts

Using the tools and techniques discussed in chapter 2, several investigations of back-contact behavior have been made. In the present chapter, we attempt to address the following questions: (1) How do non-uniformities of the back contact arise? (2) When present, what characteristics do they present that differentiate the non-uniform case from the uniform case? (3) How does LBIC give us clues as to the nature and severity of back-contact non-uniformities? And finally (4) can we propose a simple equivalent circuit model to account for non-uniform behavior?

The devices for which results are presented here have back-contacts prepared by multiple processes, each of which can introduce non-uniformities by different mechanisms. The first sections will describe the back-contacting processes used for the devices in question and potential sources of non-uniform electrical behavior are identified. Next, experimental evidence of back-contact based non-uniformities is presented and discussed. Finally, a simple, yet flexible model is introduced for averaging the contribution of back-barriers with varying severity to predict full device response.

3.1 Issues relating to back-contacts for CdTe solar cells

As mentioned previously, the back-contact to p-CdTe based thin-film solar cells is one of the most complicated and delicate parts of the solar cell fabrication process. In the context of this document, the 'back-contact' includes all processing subsequent to the $CdCl_2$ annealing. The models for solar cell function considered here share the assumption that current in the absorber layer flows only normal to the device plane, i.e. light generated electrons flow from back to front of the device, and forward electrons flow from front to back. One could think of current flowing only parallel to the axis of columnar grains of absorber material. Only in the contact layers does current flow laterally and condense into whatever wire or lead is contacted to the cell.

3.1.1 Back Contact Formation Processes

The schematic picture of Fig. 1.4 glosses over the complexity of the various methods, which have been developed for contacting the absorber layer of CdTe solar cells. Two contacting methods are of particular interest for this chapter. 'NREL' devices are typically completed using a three-step back-contact-formation process. A wet chemical etch is used (either nitric-phosphoric acid in water or dilute bromine in methanol) to strip the CdTe surface of contaminants and residue from the $CdCl_2$ process, and to create a smooth, Te-rich surface layer. This layer is already more p-type than the bulk, as the Cd-vacancy acts as a shallow acceptor, but the second step enhances the p-type conductivity by the formation of and interfacial layer, usually involving Cu and Hg, and sometimes including Sb. This interfacial layer serves to narrow the depletion due to the Schottky barrier formed by metallization on CdTe, reducing its height and influence. Finally, a metal contact is applied, either by metal evaporation or in the form of a paste containing metal particles in a carbon and polymer binder. Details of a typical NREL back contact process appear, for example, in [23]. This process, however, was amended for the devices studied here. The addition of Cu to the surface was achieved by evaporation of a 5 nm thick layer, followed by an anneal in flowing He. The electrode was formed by evaporation of a metal layer, and several elements were surveyed. Details follow in section 3.2.2.

The second technique applied in this research was the one employed at the Mechanical Engineering Lab (MEL) at Colorado State University, and since most of the devices studied in this work were fabricated there, a full review of the technology is appropriate.

The CSU fabrication process

The concept of the process is to fabricate ready-to-ship photovoltaic modules in as compact and automated of a process as possible. The viability of this process is proven by the recent incorporation of an industrial effort, producing modules based on the technique developed in the MEL. As opposed to sputtering, PVD, electrodeposition, and other techniques, the modified-CSS technique applied at CSU uses a single vacuum chamber at $\sim 30-40$ mTorr pressure and constant residual atmospheric composition for all of the deposition and annealing steps. The system uses a patented air-to-vacuum seal as an entrance to the deposition chamber, and a mirrored exit-seal.

Substrates are loaded onto a continuous belt, which is translated at two-minute intervals by a fixed distance. The translation time between positions is less than seconds. Within the chamber, a different processing station awaits the substrate at each of the standing positions. The first station is a substrate heater, which brings the glass to ~ 600 °C in two minutes. CdS and CdTe depositions occur at the next two stations, followed by a $CdCl_2$ deposition and then anneal. 'CSU' devices feature a very different back-contacting process from the NREL devices. At the next position within the chamber, re-sublimation of the $CdCl_2$ is induced by reversal of the thermal gradient which drives the evaporative transport of material to or from the substrate. A Cu-containing compound is then evaporated onto the film stack, and annealed for two minutes at 200 °C. After the completed device exits the deposition chamber, any residual chloride haze is rinsed off in methanol, and a graphite layer ($\sim 2\mu$m) is spray-deposited onto the film-stack, followed by an electrodag contact layer ($\sim 100\mu$m), which contains Ni as the electrode metal. A schematic of the deposition process is given in fig. 3.1.

Variations in processing are implemented either by changing the deposition time, the thermal conditions of one or another station, or by changing one of the sources. For example, the Cu deposition can be eliminated by setting an empty crucible at that station, or could

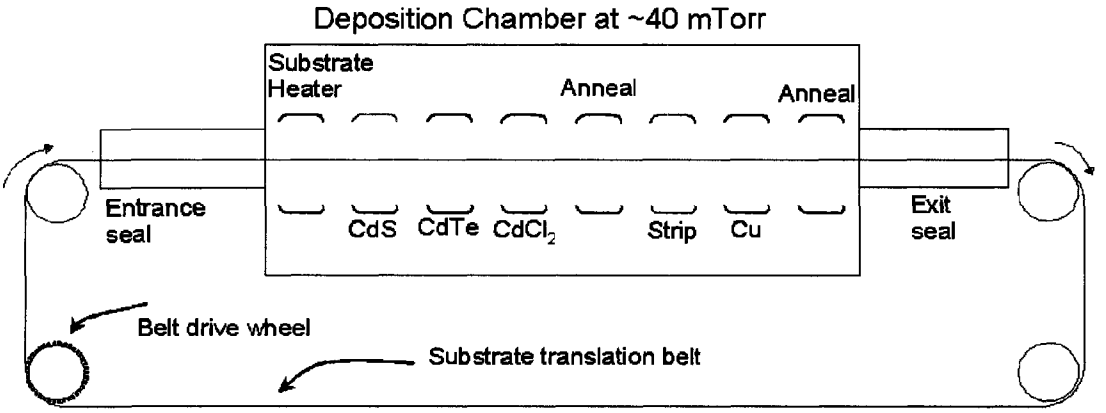

Figure 3.1: The all-in-one deposition process conceived at Colorado State enables fabrication of high-efficiency PV devices using a minimum of materials, processing complication, and space.

be enhanced by leaving the substrate at that station for two deposition periods simply by pausing the belt advancement for one step. Another option would be increasing the source temperature under the crucible, or reducing the temperatures in the previous station, so that the substrate comes in colder, giving a higher sticking coefficient.

3.1.2 Determination of back-contact-barrier height

The solar cell equivalent circuit of figure 2.4 implies that the front and back contacts to the solar cell are ohmic. These assumptions are not always true, especially as regards the back-contact. Because of the rather large band-gap and electron affinity of CdTe, there are no pure metals with work function great enough to make ohmic contact [24]. Consequently, contacting a CdTe solar cell generates a Schottky barrier at the back of the device. A new equivalent circuit to represent this behavior was proposed by Stollwerk and Sites [25], and is indicated in fig. 3.2

The 'height' of this secondary barrier is measured from the fermi-level in the semiconductor bulk to the valence band maximum at the material interface, and is given by:

$$\varphi_b = (\chi_s + \frac{E_g}{q}) - \phi_m \tag{3.1}$$

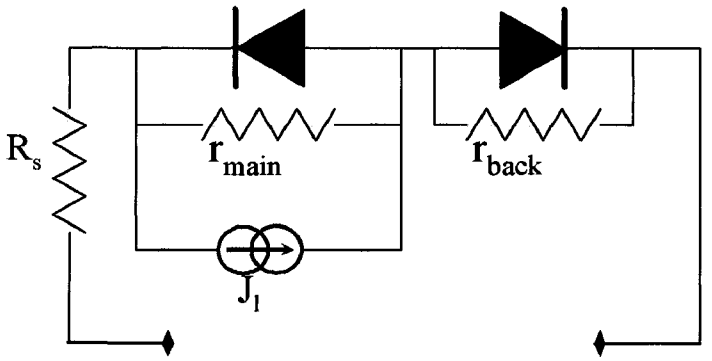

Figure 3.2: The two diode model proposed in [25] describes the behavior of a Schottky back contact as a leaky, reverse-polarity diode connected in series with the main junction diode.

where φ_b is the back-contact barrier, χ_s and E_g are the semiconductor electron affinity and band-gap, and ϕ_m is the work function of the metal.

The Schottky barrier may be lowered for holes attempting to exit the semiconductor by the image-forcing effect, and the change barrier height $\Delta\varphi_b$ is given by

$$\Delta\varphi_b = \sqrt{\frac{qE_{max}}{4\pi\epsilon_s}} \tag{3.2}$$

where E_{max} is the electric field strength at the interface, which depends on the semiconductor carrier concentration and the barrier height. For CdTe at a doping level of 10^{14} cm^{-3} the barrier lowering effect amounts to about 0.01 eV reduction in the barrier, so it is a small effect, unless steps are taken to increase the doping in CdTe. Increasing the p-type carrier concentration to 10^{18} cm^{-3} or higher increases the barrier reduction to 0.1 or more eV, which can become significant for device performance.

The effect of this barrier on the current voltage characteristic of the device is to block the forward current by impeding majority carrier (hole) injection from the back contact at a level equivalent to the saturation current of the secondary diode. The saturation current for a Schottky diode (metal-semiconductor) is given by

$$J_{ob} = A^* T^2 \left(e^{\frac{-q\varphi_b}{kT}}\right) \tag{3.3}$$

where A^* is the Richardson constant and only depends on the semiconductor parameters, T

is the absolute temperature, φ_b the back barrier from equation 3.1, q the elementary charge and k is Boltzmann's constant. It is apparent from equation 3.3 that a small barrier results in a large back contact saturation current. Conversely, for high barriers, the back contact current, and thus the whole device current becomes limited. The result is a flattening or "roll-over" of the current in the first quadrant of the I-V curve, accompanied by a FF reduction in the 4^{th} quadrant of the illuminated curve. One estimates the back barrier from experimental data by identifying the current density at the onset of rollover and equating it to J_{ob}. The barrier effect on a J-V curve is shown in fig. 3.3(a).

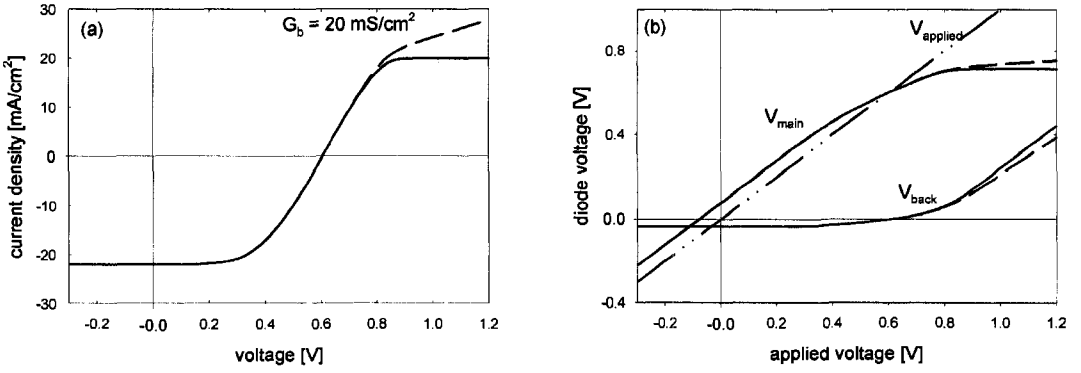

Figure 3.3: Simulated current-voltage curves (a) and voltage distribution (b) for the equivalent circuit of figure 3.2 with back-contact leakage conductance of 0 (solid lines) and 20 (dashed lines) mS/cm^2. The back diode has a saturation current of 20 mA/cm^2, corresponding to a barrier height of 0.436 eV.

In terms of the equivalent circuit from fig. 3.2, the rollover feature of the J-V curve is manifest as a voltage division between the front and back diodes. This can be calculated from the requirement of current continuity, as was proposed in [26], and the front- and back-voltages are plotted in figure 3.3(b). While the main junction is in forward bias, and would allow current to flow, injection of holes from the back contact is blocked by the reverse-biased Schottky barrier.

The applied voltage is the sum of the voltage drops across the front diode and the back barrier (minus the drop across the series resistance). From figure 3.3(b) one can see that the effective voltage on the main junction is increased in the power quadrant by the voltage developed across the back-diode needed to allow the photocurrent to flow. The increased effective voltage on the main junction contributes to reduced fill factor, while V_{oc} and J_{sc}

are unaffected.

3.1.3 Back contact barriers: the role of Cu

We have seen how a high hole-barrier at the back contact can inhibit forward current injection, and why such a barrier is a common feature of CdTe solar cells. A barrier height of ~ 0.8 eV, as one can calculate from CdTe and Ni work functions, would induce a major rollover in the first quadrant, limiting essentially all forward current flow. The barrier lowering effect may reduce this value a little, but the barrier is still high enough to reduce the power conversion. A widely used strategy to mitigate the back barrier effect is to include Cu by some means at the back surface of the device. The method Cu inclusion for two fabrication methods was described above.

So what does copper do? The jury is still out, but a number of behaviors which may improve the cell behavior have been identified. When a Cu atom sits on a Cd vacancy in the CdTe lattice, it acts as a shallow acceptor, so one effect is to increase the doping of the back surface. Increased doping increases the barrier lowering effect as discussed previously. Higher carrier concentration also reduces the depletion width due to the Schottky barrier. Alternatively, one may consider a modification to the band structure by the creation of a Cu_xTe layer, which has a different band-gap and electron affinity from CdTe.

Although Cu has been shown to be helpful in reducing back-barrier effects, it has also been implicated in instability of CdTe solar cells. In a polycrystalline film, Cu can migrate quickly, especially along grain boundaries, so the Cu which is introduced at the back contact may not stay there. Just as Cu_{Cd} is an acceptor, the copper interstitial gives a donor state in CdTe, so Cu which moves away from the back contact is likely to be two-fold harmful, since the barrier could re-emerge, and the minority carrier lifetime in the absorber is reduced by the higher density of recombination centers.

Up to this point the discussion of back barriers and the strategy for reducing their effects has been applicable in one-dimension. To conclude this introduction to the experimental work, a generalization of the discussion to include the effects of non-uniformities is necessary.

3.1.4 Back-contact sources of non-uniformity

The back contacting processes described above, when performed on a rough, polycrystalline, as-deposited CdTe layer, can induce non-uniform electrical behavior in numerous ways. SEM studies have indicated, for example, that the Br:methaol and nitric-phosphoric (NP) etches strip the CdTe surface differently.[27] The NP etch results in a smooth and planar surface, but also widens the grain boundary void regions. The Br:methanol etch does not strongly expand the grain boundary regions, but the surface texture remains rough after etching. For cases like the 'CSU' process, with no wet etch, but a thermal re-sublimation of material off of the substrate, thermal uniformity is of paramount importance, since the sublimation rate principally depends on the temperature. In practice, the re-sublimation is not uniform on the cm-scale, and devices from a single substrate may show differing behavior as a result, even though on the μm scale, only a weak gradient in response might be observed.

When it comes to applying the Cu interface layer, the degree of alloying that takes place, and the uniformity of coverage will depend strongly on the surface condition, so a rough surface may experience non-conformal coverage, and a porous surface could be susceptible to enhanced grain-boundary diffusion of metal impurities. It is also to be expected that during formation of the interfacial compound, be it Cu_xTe with $1 < x \leq 2$, or p+ CdTe, any non-uniform etch depth or geometry will be reflected in the thickness or doping level of the barrier-reducing layer. For the CSU process, the Cu deposition and anneal is non-uniformly modified by the presence of residual $CdCl_2$ so that even the chemical condition of the back surface will vary with position.

A paste- or spray-based electrode layer is many times the combined thickness of all the other layers and is composed of a well-mixed suspension of metallic particles in a binder material, so it is expected to behave as a layer of essentially infinite thickness and uniform composition relative to the semiconductor surface. However, the potential Schottky barrier created when applying the metal layer to CdTe is bound to reflect the non-uniformities generated in the previous steps. Also, although the electrode is not likely to become depleted of metal atoms, it may act as a source of defect impurities, if diffusion of metal out of the

contact and into the semiconductor layers is energetically favorable at any point. Lastly, the electrode itself *can* be a source of non-uniformities if mechanical or environmental stresses cause it to de-laminate from the thin-film stack. This is of particular concern for laboratory-scale devices, which are typically not protected by an encapsulant material and have a much larger edge-length to surface-area ratio than would a commercial-scale module.

3.2 Back-contact experiments

Several experiments have been conducted, in which the effects of variations in the back-contacting process were scrutinized. In the interest of industrial relevancy, most investigations involved devices fabricated in the in-line system at Colorado State University. Experiments involving a greater range of device processing parameters were carried out in cooperation with NREL to broaden the knowledge base of the performance of various back-contact candidates.

3.2.1 CSU devices: the influence of Cu and $CdCl_2$ treatments on device uniformity and performance

In this study, devices were chosen from two deposition runs. The processing for the two runs was nominally identical, with the lone change being the parameters of the $CdCl_2$ treatment. $CdCl_2$ treatments (1) and (2) were initially defined by the resulting performances of the devices, and it was subsequently determined that the key parameter of the $CdCl_2$ treatment was the O_2 content in the chamber. For each run, one set of devices was made which included Cu in the back-contact process, and one set was made without intentional Cu. With the exception of the Cu variable, all devices were completed using the process described earlier. Small-area devices were formed by masking the cell area and removing all the deposition layers down to the SnO_2 TCO by a sand-blasting process. An electrode to the front contact is applied using indium solder. At least four devices from each parameter-pair were included and thus a total of nineteen devices in four categories were studied, as depicted in table 3.1. All devices were characterized using current-voltage, quantum efficiency and LBIC measurements.

Table 3.1: Four or five devices from each of four categories were tested for performance and uniformity as a function of the paired influence of the O_2 content in the ambient during $CdCl_2$ processing, and in- or exclusion of Cu in the back-contact formation process.

Process Parameter	$CdCl_2$ with insufficient O_2	$CdCl_2$ with optimized O_2
No Cu	5 devices (group a)	4 devices (group b)
With Cu	5 devices (group c)	5 devices (group d)

The J-V results for nineteen devices are summarized in table 3.2. Certain trends are

Table 3.2: J-V results for the nineteen devices described above. Cu has a more dramatic effect on device performance than the changes in the chloride process, although an empirically optimized process (group b) offers substantial gains even without Cu.

Device ID		η [%]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]
No Cu	a1	5.3	685	19.0	40.5
Insufficient O_2	a2	5.7	700	19.0	43.0
	a3	2.5	610	11.5	36.0
	a4	2.7	610	12.0	36.0
	a5	3.5	635	14.5	38.0
No Cu	b1	6.8	725	20.0	47.5
Optimized O_2	b2	7.0	755	20.0	47.0
	b3	6.6	770	20.5	42.0
	b4	6.2	770	20.0	41.0
Cu	c1	9.5	740	18.5	69.0
Insufficient O_2	c2	9.3	740	18.5	68.5
	c3	9.5	735	19.0	69.0
	c4	9.6	735	19.0	69.0
	c5	9.7	740	19.0	68.5
Cu	d1	11.0	770	20.0	71.0
Optimized O_2	d2	11.8	785	20.5	73.0
	d3	11.8	775	21.5	70.0
	d4	12.0	790	21.5	71.0
	d5	11.4	780	21.0	70.0

evident from the parameters extracted from J-V measurement. Firstly, devices with Cu present at the back-contact clearly out-perform devices without. The dominant manifestation of the improvement is in the fill factor. Modest gains in V_{oc} are also achieved with the addition of Cu. Furthermore, the higher-oxygen chloride process (process 2) exhibits higher

V_{oc}, and marginally better J_{sc} and fill-factor than process 1, regardless of Cu inclusion. Beyond the parameters, additional information is available by examining the shapes of the various experimental J-V curves.

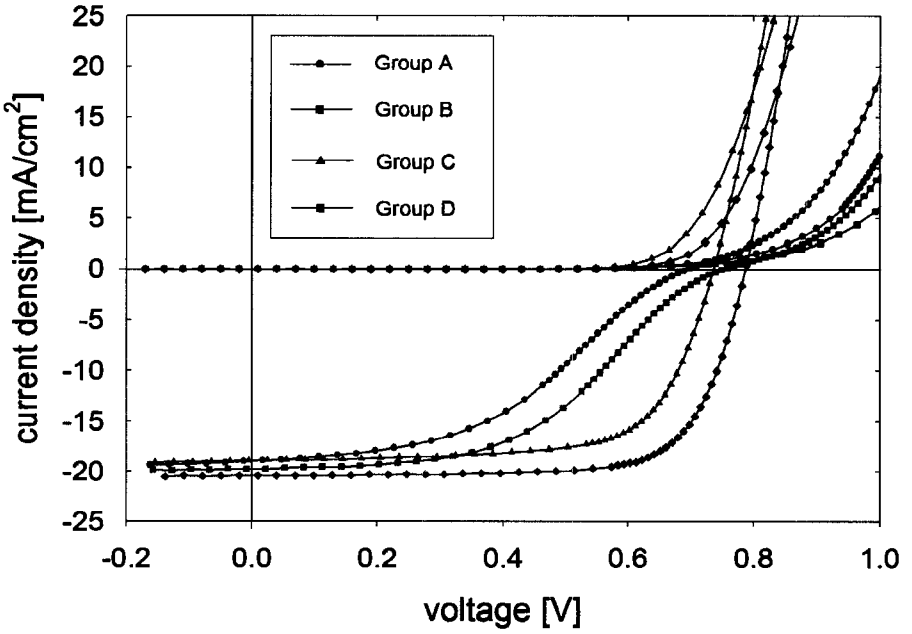

Figure 3.4: J-V curves for representative devices from each group. Adding Cu to the back contact cures the rollover behavior in an otherwise identically processed cell.

The fill factor gain mentioned before can be seen in fig. 3.4 to be achieved through the elimination of the non-ideal behavior apparent in the illuminated J-V curves for the group 'a' and 'b' devices. Since the difference between 'a' and 'c' devices, as well as 'b' and 'd', is only the Cu, a fair conclusion is that the back contact is at the root of the deviant J-V curves and that the addition of Cu removes the cause of that behavior. This non-ideal shape of the curves for 'a' and 'b' devices recalls some of the general features of barrier-induced rollover, but observe that the curves do *not* look the same as the simulated curves from the equivalent circuit example of before. In particular, the downward concavity of the curve reaches a maximum in the fourth quadrant, and there is a secondary turn-up in forward current, which are not permitted by the theory of the two-diode model. Nevertheless, the addition of Cu minimizes the behavior, so it is reasonable to attribute this modified rollover to the back contact. A similar behavior was simulated by Pan [28]

with a combination of minority carrier lifetime and back-barrier height parameters placing the model at the transition between a full-rollover (like the two-diode model) regime where hole impedance limits the total current, and a regime where enhanced electron current dominates the forward current behavior, causing a reduction in device voltage. This 1-D model predicts the delayed turn up of forward current, but rollover current still occurs in the first quadrant. One possibility for the difference is that the fourth-quadrant rollover is a result of non-uniformity, making it impossible to model in one dimension. The LBIC technique allows us to verify the uniformity assumption experimentally. Presented in figure 3.5 are the LBIC photomaps for the devices with the J-V curves shown above. The devices with Cu show a very uniform response over the full device area, even at high contrast. The device without Cu, but with the optimized chloride process is also uniform under short-circuit conditions. The group 'a' device has significant variations on $\sim$ 100 μm and mm scales.

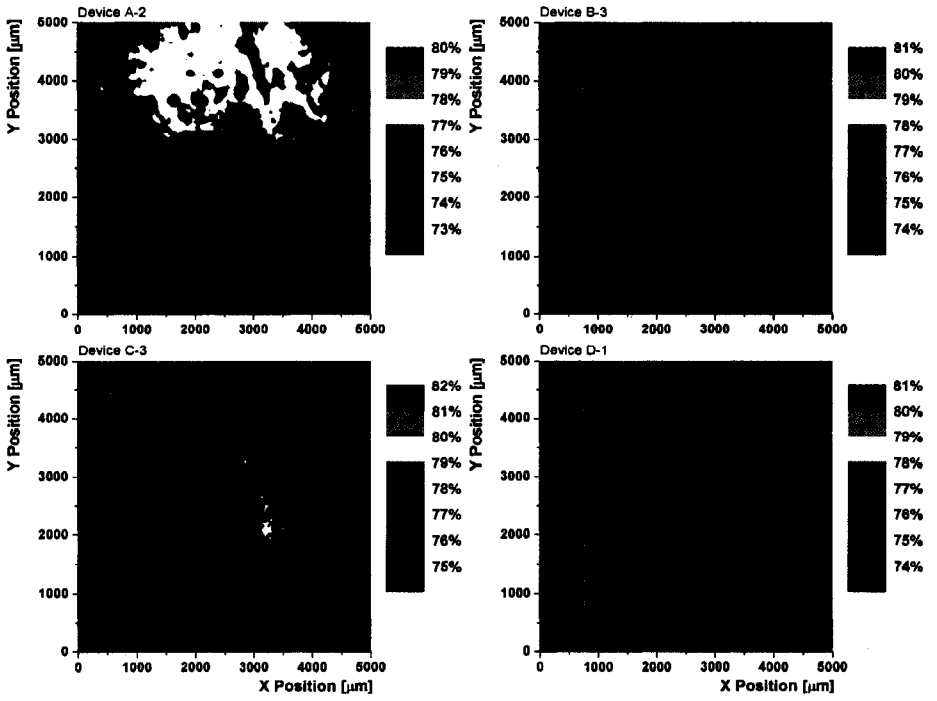

Figure 3.5: Regardless of $CdCl_2$ treatment conditions, the addition of Cu at the back contact improves the uniformity of photocurrent collection. All scans at zero voltage bias.

With what we know from the J-V and LBIC data, we can identify trends in the device

behavior, and propose a model for the physical situation of each combination of process parameters. The addition of Cu improves the fill factor. The addition of Cu improves the device uniformity. Perhaps the phenomenon which contributes non-uniformities to the LBIC measurement is the same one that causes the fourth-quadrant rollover.

Even more telling than the LBIC data of fig. 3.5, is the evolution of the device uniformity with forward voltage bias. Performing the LBIC scan on each cell a second time, at a voltage approximately V_{mp} - 50 mV, yields the data shown in figure 3.6

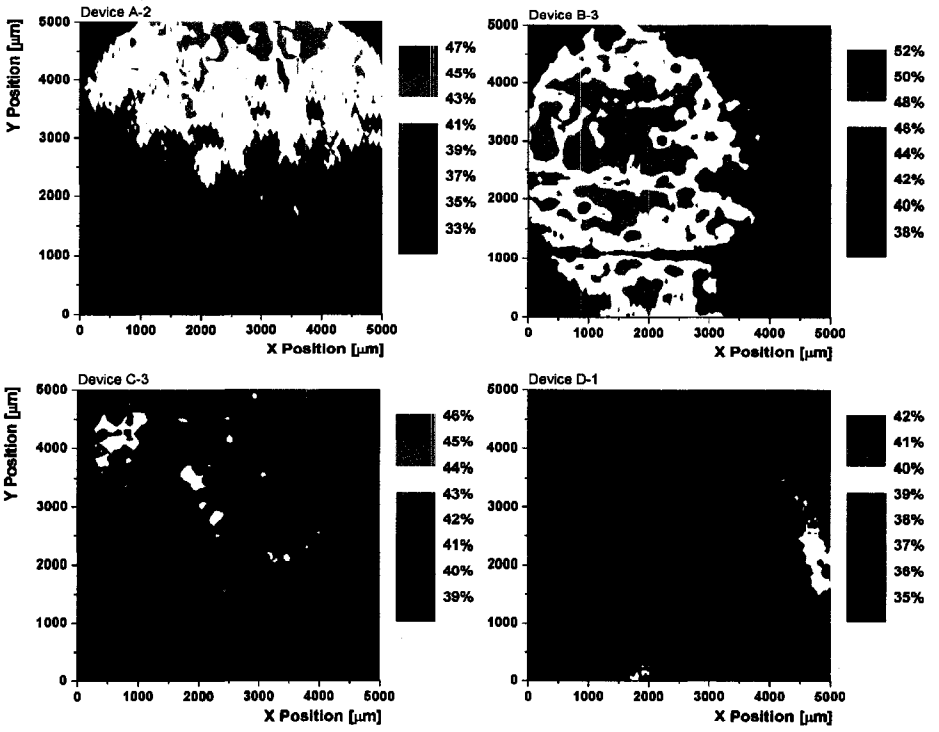

Figure 3.6: The development of non-uniform photocurrent collection with increasing voltage shows that much greater spatial variations exist in the collection of cells without Cu-containing contacts, than in those with Cu. Variable back-contact barrier influence is the most logical culprit, given the expected influence of the Cu. Bias levels were chosen so that $QE_{bias} \sim QE_{sc}/2$

Even changing the contrast level for the cells without Cu, they clearly appear less uniform on the $\sim$ 100 μm and mm scales, whereas for the cells with Cu, collection reduces with voltage bias uniformly over the whole device area. The reader is reminded that the change of collection efficiency with voltage is directly related to the change in depletion width, as spelled-out in equation 2.4. As far as carriers generated by the 638 nm illumination

are concerned, the band profiles for devices with Cu are uniform and respond uniformly to voltage bias. Cells without Cu at the back contact exhibit changes in the collection function of up to 10 % over the cell area, implying variations in the band profile within the device.

3.2.2 NREL devices: the consequences of the choice of back-electrode metal on device uniformity

As previously discussed, the presence of Cu in the back-contact reduces the influence of the Schottky barrier. A study performed on devices using an evaporated Cu layer after a wet chemical etch showed that 5 nm of Cu was sufficient to mitigate the back-barrier effects for one electrode composition, while not introducing so much Cu that recombination or compensation were enhanced [24]. Based on this result, a second study was designed to examine the uniformity and performance consequences of the back contact electrode.

Starting from nominally identically prepared CdS/CdTe/$CdCl_2$/anneal/surface etch devices, back-contact formation was completed by evaporating 5 nm Cu followed by an anneal to incorporate Cu into a Cu_xTe layer, then various metals—Ni, Ag, Au, or Al—were evaporated 300-500 nm thick to form a back electrode. J-V and LBIC characterization showed that device performance and uniformity were strongly correlated, and varied with the electrode metal chosen. LBIC data are shown in figure 3.7. For each electrode metal tested, there are areas of good and poor collection. We can speculate as to the driving mechanism for the poor regions in each of the photomaps shown. In all cases, the weakest areas originate from the cell edges so the cell definition process may be responsible for adhesion loss there. Still, gold and nickel contacts produce nominally uniform devices using the process described here. The device with a silver contact shows moderate variation on the micro-scale, with features on the order of 100-200 μm in size varying by up to 3 or 4 % in collection. These variations are overlayed on a gradient of average response from left to right of the scan area of about 12 %. The aluminum contacted device shows only small areas where photocurrent collection occurs at all, but these islands have fairly high collection, in the $\sim$80 % range, implying that the Al contact could perform well, but is very prone to catastrophic failure. The susceptibility of the contacts to adhesion loss of differing severity should not overshadow the differing tendencies towards formation of micro-nonuniformities,

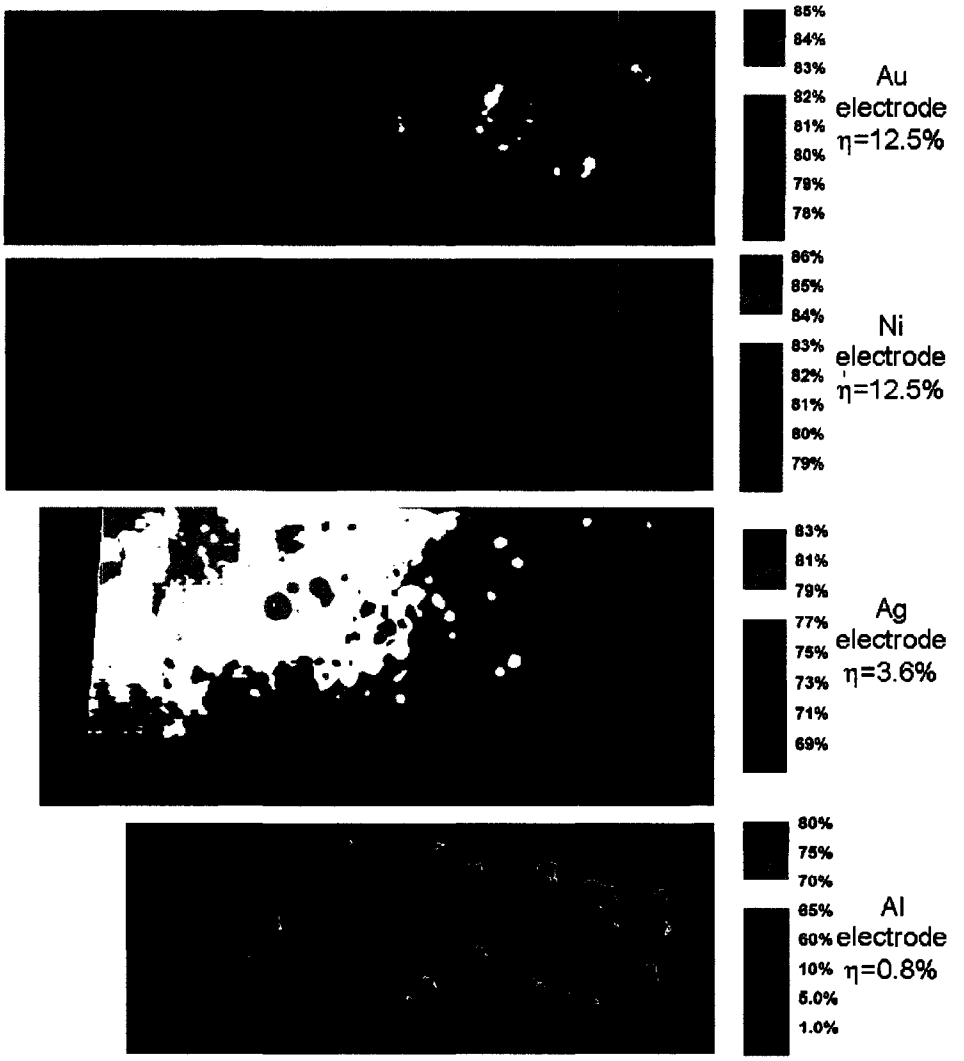

Figure 3.7: Even with equivalent $CdCl_2$ and Cu processing, CdTe devices can show a strong dependence of uniformity on back electrode metal. Using high-contrast display, Au, and Ni contacted devices show superior uniformity to Ag and Al, even when the latter are plotted with a larger color interval.

which are much more prevalent in Ag and Al cells than those with Au or Ni contacts. The poor performance of Al and Ag back-electrode materials in this study was related to the energies of formation of telluride compounds. [24] Those metals (Al and Ag in particular) that have a low heat of formation for metal-telluride phases are more likely to alloy with the absorber layer. Inclusion of electrode-based impurities can have deleterious effects in two ways: it can contaminate the Cu_xTe layer, freeing Cu atoms to move into the absorber; the high mobility of certain impurity atoms in CdTe also suggests that defect states corresponding to Ag, or Al impurities could arise in greater concentrations than other metals. The J-V performance of these devices correlates with the LBIC measured uniformity, with Ni giving the highest efficiency and Al the lowest, and while LBIC is performed at only one wavelength, it hints at the large differences in J_{sc} and V_{oc}. First and second-level J-V parameters are summarized in table 3.3.

Table 3.3: The Al contacted cell shows only small islands of photocurrent collection in LBIC, and the corresponding J_{sc} is very low. Those devices with better LBIC uniformity also have higher current and fill-factor from J-V measurements.

Electrode Metal	η [%]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]
Au	12.5	780	23.5	68
Ni	12.5	790	23.4	68
Ag	3.6	642	11.1	50.5
Al	0.8	751	3.7	27.5

3.3 Failure of the two-diode model

We have shown that the presence of a significant back-contact barrier tends to correlate with non-uniform photocurrent collection, so that the implicit assumption of uniformity in the two-diode model does not hold. LBIC data on CSU devices with no intentional Cu in the back contact gave example of this. The change caused by addition of Cu—that is, the narrowing of the Schottky depletion region—improves uniformity and performance, restoring the J-V characteristic to a more well-behaved form. Also, a highly doped surface layer should reduce the volume of the absorber which is affected by the back-barrier, and

make it less susceptible to voltage bias effects. The Schottky barrier lowering effect of a heavily doped back-contact may also be significant, if the p-type carrier concentration is increased by two or three decades due to the copper. Without Cu, two key effects arise from variations in the back contact: (1) variations in the barrier height are reflected in non-uniform depletion width near the back-contact; and (2) when the absorber layer is thin, front junction and back-contact depletions may overlap, reducing the built-in potential. Thus the two-diode model must be amended for the situations were (1) the properties (notably the saturation current which depends on barrier height) of the back-diode are not uniform and (2) the elements cannot be considered discreet in an equivalent circuit model.

It was also shown that even when the back-contact barrier is mitigated with a Cu layer, the electrode metal chosen can exert a strong influence on device uniformity and performance. The assumption that photocurrent generation and collection is uniform needs amendment to account for situations like the NREL device with Al electrode, which showed that the back-contact properties, most likely the contact resistance when adhesion is an issue can induce non-uniformities in this respect as well.

3.3.1 Modeling of non-uniform back-contacts

Based on the discussion above, a generalized equivalent circuit model is necessary to include the possibility of influence from all the effects observed. Distributed diode networks have been used by others to model nonuniformities of the main-junction [29–31], and we make use of this technique to simulate non-uniformities of the back-contact as well.

The four diode model: barrier variation only

The simplest case is non-uniform barrier height, which does not affect the primary junction, or the generation of photocurrent. Such a case can be modeled with an equivalent circuit with two branches. The diode representing the main junction is identical in both branches, but in the first branch the barrier is low, representing the device area where the optimized back-contacting process has functioned as intended. The second branch has a high barrier, which is variable depending on the expected physical situation of the solar cell. For example, a cell with an insufficient Cu treatment, or which has degraded due to exposure to high

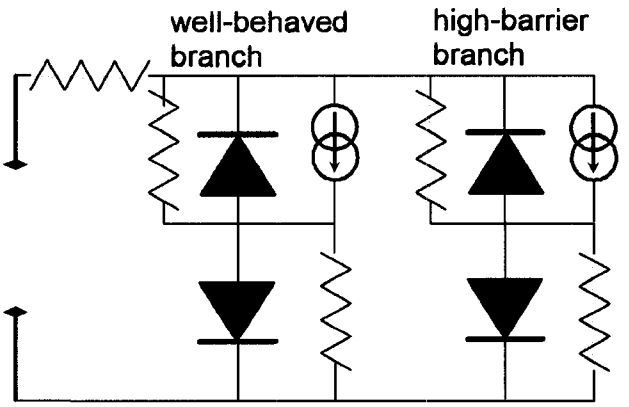

Figure 3.8: In the generalized equivalent circuit for a device with non-uniformities, the contributions from non-ideal components (back-contact barriers and main-junction variations) are averaged into a single set of parameters for the 'weak branch'. The strong branch behaves much like the circuit from 3.2 with a very low barrier.

temperature/humidity will wind up with some areas of low barrier, thanks to locations of conformal Cu_xTe coverage of the interface between CdTe and the electrode, and areas where CdTe abuts the electrode or a metal/telluride phase generates a high-resistance contact. The relative areas of the high- and low-barrier branches are selected by modifying the saturation current parameters of the circuit elements, and re-distributing the magnitudes of each branch's current source. The PSpice software takes these parameters as current, so we assume a typical current density for CdS/CdTe and multiply by the area fraction for each region. The J-V curve generated by this model does not deviate qualitatively from the uniform low-barrier case. The slight increase in V_{oc} is explained in terms of the voltage distribution shown in figure 3.3(b). As the saturation current of the barrier diode is approached, the voltage of the 'weak branch' is transferred to the back barrier diode, while the parallel branch continues to develop greater forward current due to the voltage on the main junction. Since only one branch of the circuit contributes to the forward current, it develops slower, causing a slight increase in V_{oc}. The current blocking of the weak branch contributes to a small reduction in the device fill factor. However, unless one returns to the 'uniform' case, but with the entire area exhibiting a substantial barrier, the rollover effect is not observed.

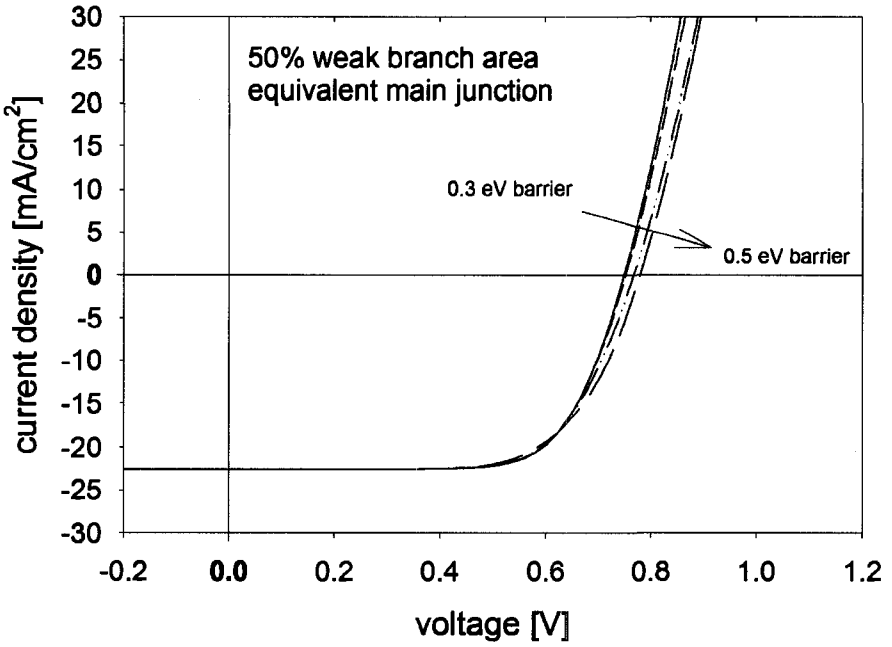

Figure 3.9: The five curves which nearly overlap are the result of the equivalent circuit of figure 3.8. The barrier heights simulated are 0.3, 0.35, 0.4, 0.45 and 0.5 eV. For the highest barriers, there are small deviations in FF and V_{oc}.

The four diode model: barrier and junction variations

Next, consider an extension of the model to include situations where degradation or variations of the back contact not only cause a variation in barrier height, but also change the performance of the main diode junction. Two important physical scenarios make a model which includes variation in *both* front and back-diode elements relevant.

Defect contamination

Firstly, the scenario of a degraded back contact, as hinted at before, should induce some variations in the back contact performance, but evidence suggests that this degradation also supplies recombination centers for the main junction. One possible description of the physical situation is that the metal atoms which leave the back contact and enter the absorber diffuse perpendicular to the junction plane (probably along grain boundaries, but also in the bulk) to the space-charge-region or even the absorber/window interface, where the enhanced recombination reduces the local junction voltage. Equivalently, the recombination current is increased by the presence of these impurities. The modification to

the model, then, is fairly straightforward: the branch which contains the high-barrier back diode should also have a main-junction diode with lower voltage, or higher I_0.

Depletion overlap

A similar model can be used to describe a very different phenomenon which has been labeled the "reach-through" effect by others [29]. The driving mechanism of this feature is the doping in the CdTe layer. The extent of carrier depletion in the absorber layer is calculated as in Chapter 2. If the absorber layer is thin, and the CdTe doping is low, the full depletion regime is entered, and this can be verified with capacitance measurement. C-V on CSU devices virtually always shows no change in capacitance with varying reverse dc bias, indicating that the depletion width cannot expand past the back-contact. Now, a back contact prepared without Cu or another treatment to increase the p-type doping near the CdTe surface will develop a significantly wide depletion of its own, determined by the barrier height and the CdTe carrier concentration. When the depletion due to the Schottky barrier and the depletion of the p-n junction overlap, then the minimum difference between the fermi-level and the valence-band maximum increases, lowering the electron barrier V_{bi}. There is a direct effect on V_{oc}, since it is limited by V_{bi}. This situation can arise when variations in absorber layer thickness, barrier height, or doping cause the extent of front and back space-charge region overlap to change with position. Heavy doping at the back surface, or minimization of the Schottky barrier by Cu addition or contact material choice can eliminate the overlap of front and back depletion regions, or at least make the extent of the overlap less sensitive to variations, since it would occur in the nearly-flat-band region of the absorber layer and the back-depletion width would be less buffered from expansion with voltage by the high carrier density. The same model of varying back-barrier height and varying front junction voltage can describe the reach-through case since the built-in potential of the solar cell may vary between the extremes of the neutral bulk case and the case where the valence-band to fermi-level difference equals the barrier height.

The four diode model in PSpice

The PSpice software calculates the current response to an applied voltage at a chosen point in the circuit. For the diode elements, the critical parameters that determine the J-V curve are the saturation current, the internal resistance and the ideality factor. To

establish a modeling baseline, parameters were chosen that yielded a curve typical of a 'CSU' CdTe device. These are: $J_o = 10^{-5}$ mA/cm^2, A$\sim$ 2 and $R_s = 0.5$ Ωcm^2. For this work, the basic cell was then divided into two branches with areas calculated as described above. The barrier height for the weak branch is assumed, and the back-diode saturation current calculated from eq. 3.3. J-V curves were generated for several values of the barrier height. A third dimension was added, assuming varying severity of degradation of the main-junction in the weak branch of the circuit, achieved by increasing the I_o of the weak-branch main-junction. The conditions of the simulations performed are summarized in table 3.4.

The strong-branch main-junction was left alone. The PSpice simulations performed for this section use only a lumped series resistance, with no resistance separating the branches of the circuit. From basic circuit theory, it is therefor understood that the only effect of reducing the strong-junction performance will be to shift the final forward-current turn-on regime to lower voltages.

Table 3.4: The 'weak branch' conditions simulated using PSpice circuit modeling software. All combinations of barrier height, degraded-junction saturation current, and weak area were calculated.

Barrier height eV	'weak branch' voltage mV	'weak branch' area:total area %
0.3	760	10
0.35	680	30
0.4	650	50
0.45	580	70
0.5	440	90

A selection of the results is presented in figure 3.10. The modeling results corroborate the supposition that it is necessary to have areas of high and low V_{oc}, and high and low back contact barrier in order for the non-standard rollover behavior to appear in the J-V. In other words, the rollover observed experimentally in cells with insufficient barrier mitigation, or somewhat degraded cells is directly linked with non-uniformities. It is therefore advisable to take care in the fabrication of CdTe devices so that chance for formation of back-contact related non-uniformities may be minimized.

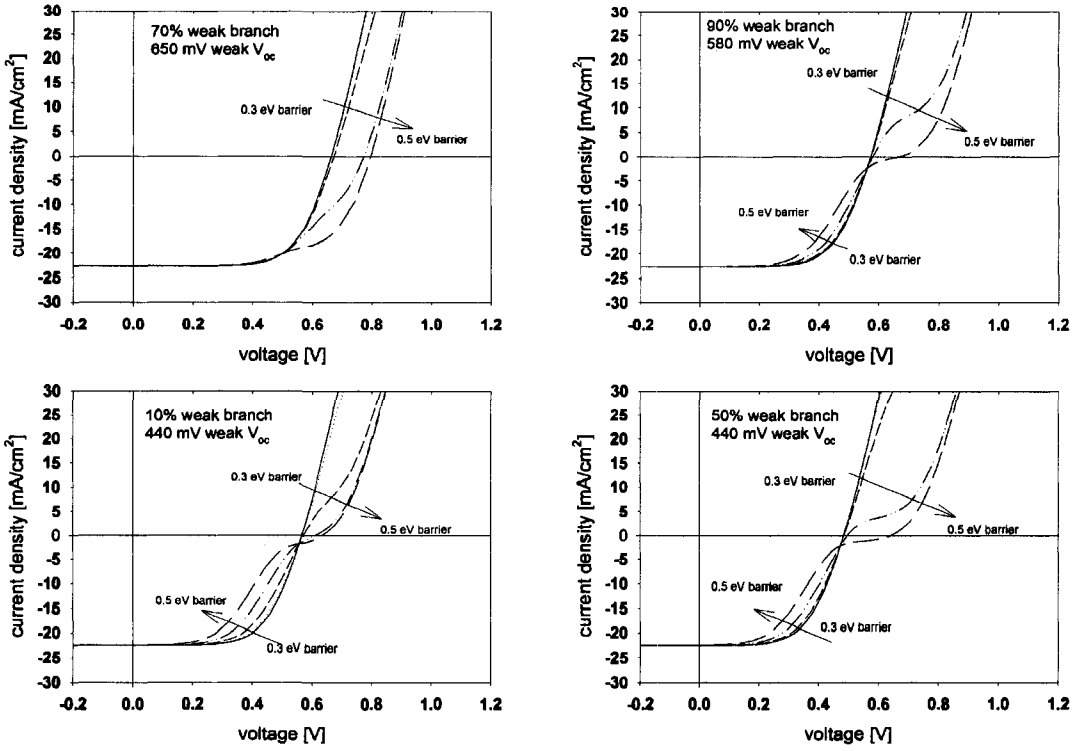

Figure 3.10: Simulation J-V with influence from back-contact based non-uniformities when they also induce reductions in main-junction performance. This combination of effects can result in rollover in the power quadrant, as observed in some experimental data.

Putting the four-diode model into practice

The ultimate test of this (or any) model of solar cell behavior is whether or not it has fairly general application. We'll test it on another set of experimental data. Let us consider the device with J-V curve shown in figure 3.11.

This is another 'CSU' device (from a much later deposition run than the ones discussed before) with no Cu in the source during deposition, but all other fabrication parameters fairly well optimized. The J-V shows the same non-standard (i.e. fourth-quadrant) rollover with subsequent turn-up as was attributed to non-uniform blocking of forward current by the back contact in earlier experiments. LBIC scans were performed on this device at the bias levels indicated by the cut lines on the J-V graph, as well as short circuit. The photomaps for two of the scans are given in figure 3.12

From inspection of the photomap of the forward bias scan, one can estimate an area

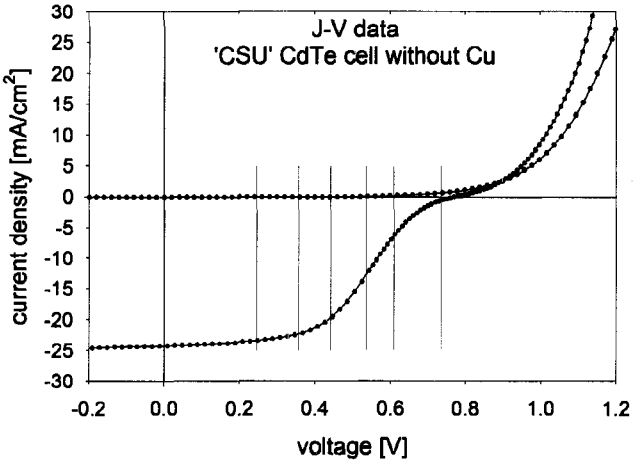

Figure 3.11: Experimental J-V curves for a 'CSU' device without Cu in the back contact. Voltage bias levels for LBIC measurements are also indicated.

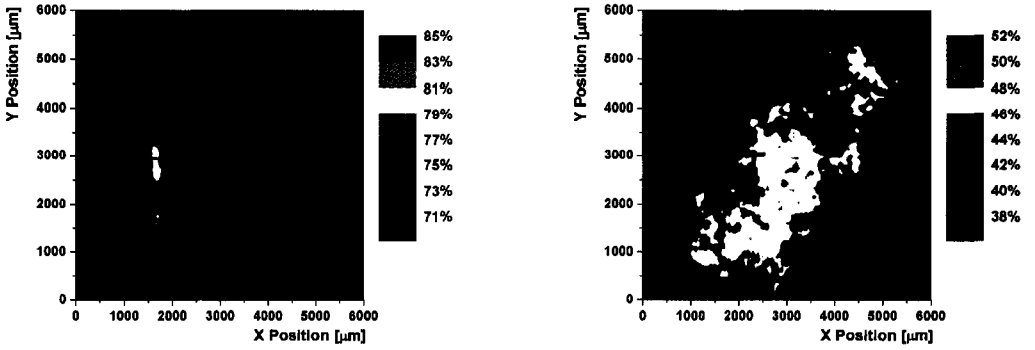

Figure 3.12: LBIC photomaps at short-circuit conditions (left) and 535 mV forward bias (right). The severe loss of uniformity in forward bias correlates to the presence of multiple diode turn-on regimes.

division for the two branches of the equivalent circuit model. Approximately 60 %, (corresponding to green and yellow color areas) of the area might belong to the well-behaved branch, and 40 % (cyan $\rightarrow$ dark blue) to the weak branch. This may be corroborated by examining the histograms of these scans.

To see if the four-diode model can closely reproduce the observed J-V behavior, series and shunt resistances of 3.5 and 600 Ωcm^2, respectively, are estimated from the J-V curve. Back-contact shunt resistances are not included. The simulated photocurrent is distributed 60% in the first branch and 40% in the second. J_o is carried over from the 'baseline'

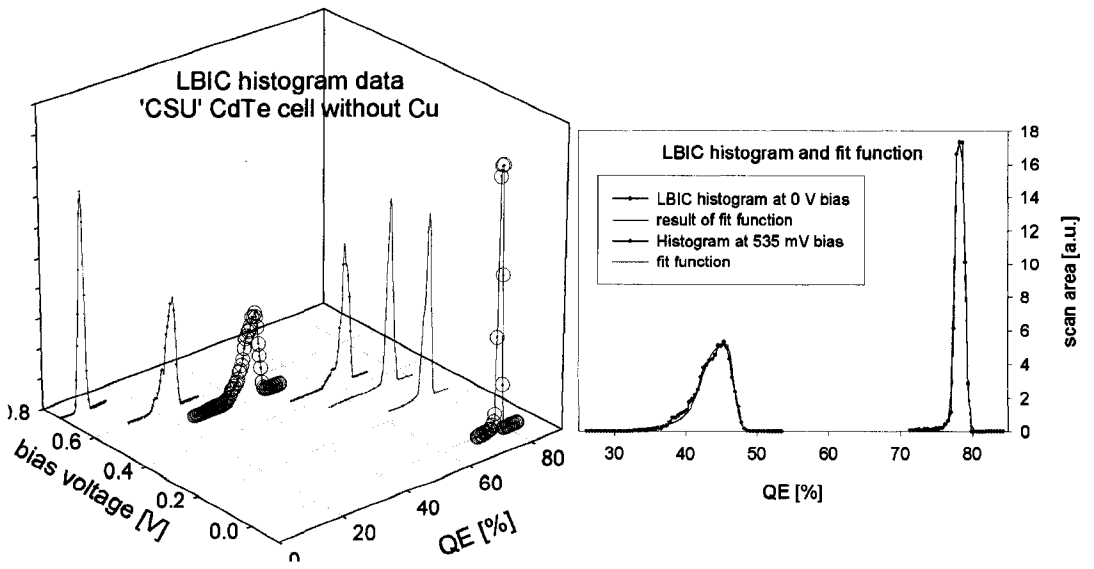

Figure 3.13: Histograms from a series of LBIC scans at various voltage biases (left) show the increasing and then decreasing spatial variations in photocurrent response. Near V_{oc} the device appears uniform, since collection in the good areas is low due to the flat-band condition, and forward current in the weak areas is blocked by the back barrier. The histograms corresponding to the photomaps above are plotted on the right, and fit using equation 2.15. The parameters in the fitting equation corroborate the $\sim$ 60/40 area distribution suggested by the photomaps.

simulation from before, and scaled to the area of the strong branch. Three parameters remain to be determined for the model: the barrier height, the weak-branch saturation current, and the diode quality factor. Analysis of the experimental J-V curve near the maximum power point suggest a diode factor of 2.2 and J_o between 10^{-4} and 10^{-5} mA/cm^2. We obtain a good fit using $A = 2.1$ and $J_o = 5.7 * 10^{-4}$ mA/cm^2. The barrier height cannot be calculated by the traditional method, so we allow the barrier height to vary within the range 0.4-0.5 eV. With a barrier height of 0.425 eV, and the other parameters of the model as described, the following fit is obtained:

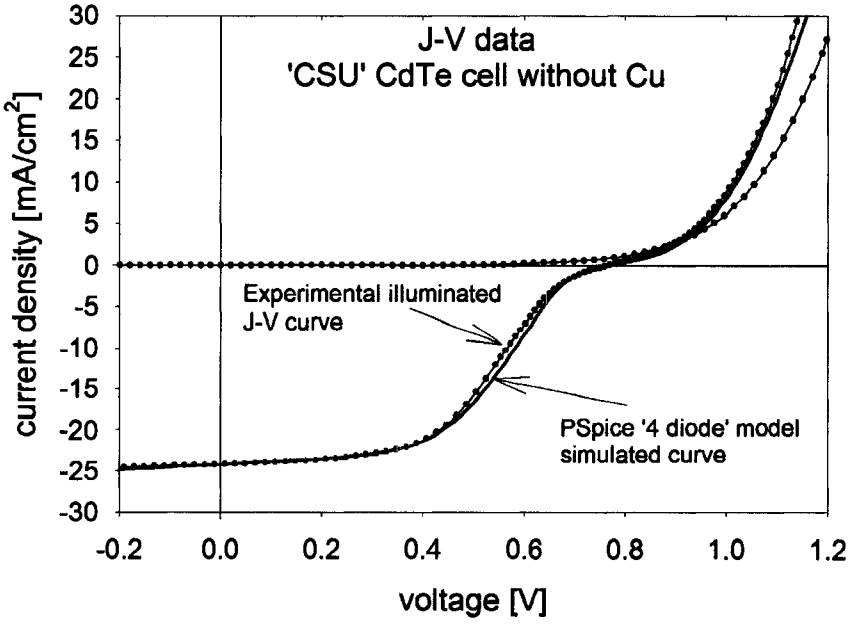

Figure 3.14: Nonstandard J-V behavior which is not explained by the two-diode model of back-barrier induced rollover, can be closely fit (green curve) by assuming non-uniformity of the device performance and modeling with parallel circuit branches representing well-behaved, and rollover-type areas coexistent on the same device.

Table 3.5: Tabulated parameters for the four-diode-model fit to the experimental data in figure 3.14.

Input parameter	area [cm^2]	J_0 [mA/cm^2]	A	φ_b [eV]
Strong Branch	0.6	10^{-5}	2.7	0.2
Weak Branch	0.4	$5.7 * 10^{-4}$	2.1	0.425

Chapter 4

Recommendations for mitigation of back-contact non-uniformities

A non-uniform back-contact Schottky barrier height can induce unwanted behavior in the current-voltage characteristic of a device, as discussed in the previous chapter. If the barrier goes above a certain height, the device will suffer a loss in fill factor, accompanied by some limitation to the forward current. The model discussed before showed that it is not even necessary for the high barrier to exist over half of the device area for there to be a detrimental effect.

In the present chapter we discuss possibilities for improving the back-contact characteristic, under the constraint of processing limitations imposed by a technique such as the CSU fabrication scheme outlined above.

4.1 Absorber thickness

Devices with thick absorbers (i.e. *thickness* $> 2x_p$), when they show rollover, tend to do so only in the first quadrant of the J-V plane, and the effect on fill factor is less than when rollover occurs near or below V_{oc}. The possible benefits of a thicker absorber include: (1) elimination of overlap of front- and back-depletion regions; (2) greater absorber volume, and longer diffusion distance for impurities to create recombination centers in the junction

region; and (3) slight improvement in conversion of photons with near band-gap energies. Drawbacks include: (1) neutral bulk region which may allow greater recombination (if, for example *thickness* $> 2L_d$). (2) higher production cost due to material usage, and (3) longer processing time (unless deposition rates are adjusted). The 'pro'-arguments are discussed in the following.

4.1.1 Separation of front and back depletion

We discussed in Chapter 3, how a thin absorber could experience a detrimental overlap of depletion regions originating with the main junction at the front and the Schottky junction at the back. For a CdS/CdTe junction with 10^{17} and 10^{14} cm^{-3} doping for the respective layers, the depletion width in CdTe is about 2.6 μm, using the approximations discussed in the capacitance section. The depletion width due to the Schottky back-contact barrier scales according to the square root of the energy barrier. Barrier heights in devices with rollover-limited performance (which fit in the two-diode regime) fall in the 0.35 - 0.5 eV range, and the corresponding depletion width in p $= 2 * 10^{14}$ cm^{-3} CdTe is between 0.6 and 1.1 μm. These depletion width calculations are for thermodynamic equilibrium conditions. One could therefore prevent interaction of the front and back-depletion regions in most cases by making the absorber layer at least 3.5 μm thick. This would allow the absorber built-in potential to reach the maximum values suggested by the carrier density, which should also delay the onset of forward current flow, resulting in more uniform V_{oc}.

Alternatively, increasing the absorber layer doping reduces the depletion width. Increasing the bulk CdTe doping to $8 * 10^{14}$ cm^{-3} would reduce the depletion width to 1.3 μm by the same calculations as before. While the depth of electric field would not completely cover the absorption/generation profile, the larger built-in potential increases the collection within the space-charge region and raises the device V_{oc} marginally. For the same doping, the Schottky depletion is reduced to 0.6 μm, so the total absorber thickness could be limited to $\sim 2\mu$m. The depletion widths calculated from equation 2.13 for the CdS/CdTe junction, and the back-contact with select barrier heights are plotted as a function of absorber carrier concentration in figure 4.1.

One recommendation, then, would be either to increase the CdTe thickness to between

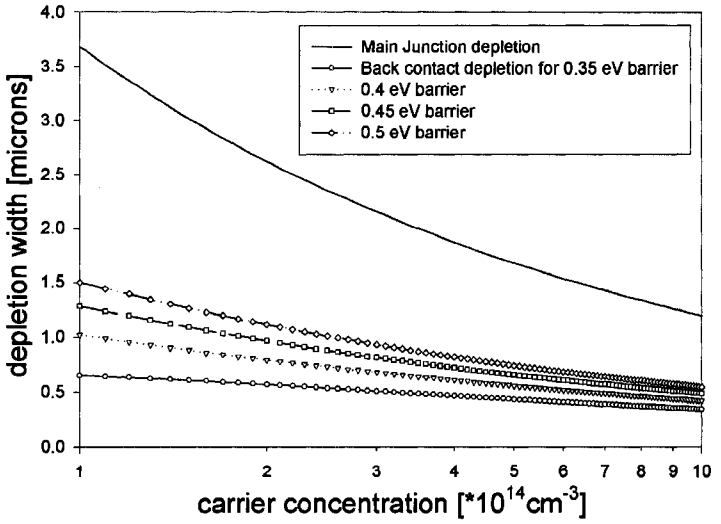

Figure 4.1: An absorber layer with thickness greater than the combined depletion widths from the front and back regions should be less susceptible to influence from non-uniformities in the back-contact

2.5 - 3 μm, or the carrier concentration to the high 10^{14} cm^{-3} range, assuming that this could be achieved with minimal re-optimization of other process parameters to ensure consistent film quality. The first option seems more accessible since final carrier concentrations are largely uncontrolled.

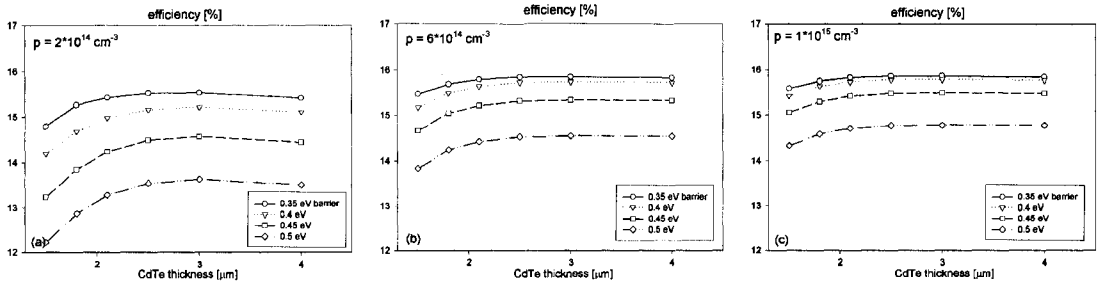

Figure 4.2: The efficiency as a function of absorber thickness for three carrier densities and multiple values of the back-contact barrier height. Efficiency is highest when the absorber is thick enough to separate the front and back depletion regions, but can be reduced if the CdTe is thick enough that collection suffers.

4.1.2 Lower impurity concentration

If the number of impurities introduced by diffusion from the back contact remains constant, and the CdTe absorber layer thickness is increased, there should be a greater absorber

volume to impurity number ratio, and hence a lower density of defects. This may be particularly important in the case of Cu usage, where as Zhou *et al.* showed [32], a compositional ratio with more than 1.4 Cu atoms per Te atom leads to instability of the Cu_xTe phase and promotes formation of harmful Cu-related defects. Greater absorber volume may help to dilute Cu_i defects, so that the compensation and electron lifetime reduction due to these is reduced.

Another often suggested mechanism for the contamination of the absorber and window layers is diffusion of impurity elements (usually metals) from the back-contact along grain boundaries[33], as in the NREL devices of chapter 3. A thicker absorber would result in longer diffusion paths for back-contact related impurities before they could reach the junction region, and may result in less accumulation of defects at the CdS/CdTe interface. The reduction of grain-boundary diffusion is expected to be small, since contact annealing has been shown to induce a rapid diffusion of contact materials into the absorber layer, regardless of thickness [34].

4.2 Electron reflector

It has been proposed [35] that an electron reflector in the conduction band at the back of the absorber layer could improve cell voltage by reducing back-contact related recombination, so long as recombination at the CdTe/reflector interface is small. This effect is expected to be particularly powerful for fully depleted devices. A candidate material for generating such a reflector is ZnTe, which should—according to ideal calculations—also help to reduce back barrier effects due to improved band alignment at the back contact. In this section, we will discuss the properties of ZnTe as they relate to the uniformity of the back contact.

4.2.1 Band alignment

ZnTe is typically a p-type semiconductor. It has a band gap of 2.2-2.3 eV [36–38] and electron affinity of 3.4 eV from studies of single crystal material. Measured carrier concentrations for ZnTe films on SnO_2 and stainless steel substrates are in the 10^{16} cm^{-3} range. If one calculates from the vacuum level downwards, there is approximately a 1 eV conduction

band offset at the CdTe/ZnTe interface and about 0.3 eV valence band offset. A Ni contact to ZnTe creates only a small barrier ($\sim$ 0.2 eV), which does not measurably affect the J-V characteristic at operating temperatures. A calculation of the CdTe solar cell energy bands with and without a ZnTe back surface layer are shown in figure 4.3.

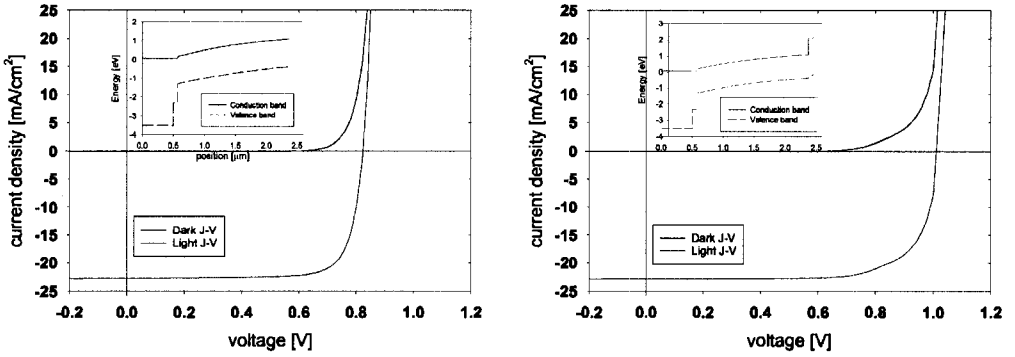

Figure 4.3: Simulated J-V curves and band-diagrams (insets) for CdTe devices with absorber thickness of 1.8 μm, $p = 2 * 10^{14}$ cm^{-3} (a and b) and a thin (100 nm) ZnTe layer (b only). The relatively low electron affinity of ZnTe establishes a positive conduction-band offset at the back of the device, reducing the number of electrons available to carry forward current. V_{oc} can be substantially increased as a result.

A reduction in back-barrier height and addition of electron reflector could significantly improve cell voltage and efficiency, provided surface recombination at the CdTe/ZnTe interface is not high. On the other hand, the conduction-band offset between CdTe and ZnTe may be too large for moderate lifetime electrons to survive long enough that the voltage benefit of the electron reflector is realized.

4.2.2 Complications of ZnTe layer

ZnTe layers have been applied in the back-contacting process to CdTe solar cells before [39], but without great success. ZnTe appears to have many of the desirable properties for filling the role of electron reflector and transfer layer between CdTe and the back-contact, but clearly the inclusion of ZnTe is not as straightforward as has been outlined here. The recombination situation at the CdTe/ZnTe interface and within the ZnTe layer itself will be of great importance, so care must be taken in the fabrication to minimize interface recombination centers. Simply transferring the position of recombination from the

CdTe/metal interface to the CdTe/ZnTe is likely to negate the effect of the electron reflector. This could be avoided using only a partial alloying of ZnTe at the back surface. The similar lattice constants of CdTe and ZnTe should facilitate a low-defect-density interface. A passivation step (such as $CdCl_2$) may be helpful following ZnTe deposition. One must also take care to provide a strong enough electric field in the CdTe to force carriers away from the back of the device, once they are reflected by the ZnTe layer. When using ZnTe a fully depleted absorber layer will be necessary.

Another possible problem is the tendency for the fermi-level to pin at mid-gap energy states on the ZnTe surface or ZnTe/metal interface [37]. In such a situation, the voltage of the solar cell is strongly reduced by added curvature in the band and a reduction in V_{bi}, resulting from an increase in the contact barrier height, superseding the band alignment calculation of eq. 3.1. The reduction in voltage, coupled with strong blocking of both forward and photocurrents could nullify the expected gains resulting from the electron reflector.

4.3 Back contact effects summary

The essence of chapters 3 and 4 is that back contacts to CdTe are a serious challenge because of the χ of CdTe and the fact that it is p-type. Furthermore, the Schottky barrier that forms between CdTe and a metal electrode is likely to be spatially non-uniform for a number of reasons: non-uniform barrier height due to stoichiometry variations, variable depletion depth from the back contact into the absorber caused by the barrier height variations, variable overlap of back- and front-depletion regions for thin absorbers, and possibly others. The result is a mixed influence of partially blocked forward current, often in combination with a locally low V_{oc}, and a well-behaved J-V characteristic. Consequently, rollover is shifted into the 4^{th} quadrant or near V_{oc}, and ff suffers dramatically. This can be modeled by a parallel combination of two (or more) spatial regions, each consisting of two opposite polarity diodes in series, and resistors for shunt/series and contact.

I would recommend making the absorber somewhat thicker—in the range of 3.5 μm—so that the front and back depletions are clearly separated. Non-uniformities resulting from back-contact diffusion should be reduced in this case, and the changes to existing industrial

fabrication processes would be minimal. A more aggressive $CdCl_2$ treatment step may be required so that the full absorber volume experiences the 'activation' attributed to that step.

With further study, it may become advantageous to add another step to the fabrication process–a deposition of ZnTe at the back of a thin/depleted CdTe layer, forming an n-i-p structure. A ZnTe contact layer may be a way to improve the device performance by providing an electron reflector *and* improving the valence-band-alignment at the back contact.

Chapter 5

Effects of non-uniform front contacts

The same basic non-uniformity issues apply to the front-contact region of the solar cell as those related to the back-contact: (1) what aspects of the materials and processes are likely to cause non-uniformities of the front contact, (2) how can we model the effects of non-uniform front contacts on the device performance and behavior, and (3) how do our characterization tools allow identification of front-contact-based problems?

In chapter 2 we mentioned that the key properties of the window layers are (1) low sheet resistance in order to minimize resistive losses, and (2) high optical transparency, so that the energy available for conversion in the CdTe layer is maximized. A common strategy in several research labs has been to reduce the thickness of the n-CdS layer to increase blue-photon response, and enhance the efficiency through higher photocurrent. On research scale cells, however, this approach has sometimes proved treacherous, since devices with too-thin CdS often exhibit lower voltage and fill factor. The uniformity implications associated with thin CdS layers are the subject of this chapter. We will begin by introducing the relevant properties the window layers used in the experimental work and employ numerical simulations to establish a framework for the performance variations one might expect with non-uniform front contacts. Next we describe experiments focussing on the role of the CdS layer, and how the device processing, and the TCO may influence device performance and

uniformity. The physical model explaining variations in localized performance stemming from the front contact is tested against the experimental data, making use of some simulated results, and literature parameters for the materials involved.

5.1 Front-contact processes/materials

Both the CdS and CdTe layers of the devices studied here were fabricated either by the close-spaced sublimation (CSS) method (the CSU process), or by sputtering. Cells were fabricated on commercially available SnO_2:F coated glass superstrates. The cell structure, unless otherwise indicated, is Glass/SnO_2:F/CdS/CdTe/back contact. The SnO_2 layer is the first to be deposited on the glass, so uniformity of this layer is a key foundation for a uniform, high-performance device. The thin CdS n-type window can reflect non-uniformities of the SnO_2 layer, or introduce problems of its own. In this chapter, the TCO and CdS layers are referred to collectively as the 'front-contact'.

5.1.1 Sources of non-uniform SnO_2

In this section we review the physical and electrical properties of fluorine-doped SnO_2 that may contribute to non-uniformities in the SnO_2/CdS/CdTe device.

Morphology and surface roughness

SnO_2 films are commonly deposited by chemical-vapor-deposition or spray-pyrolysis techniques. They exhibit small crystallite grains varying in size from a few hundred to approximately one-thousand angstroms. Surface texture may vary as well, with rms roughness between 15 and 60 nm and peak-to-valley ranges from $\sim$ 100 to $\sim$ 300 nm, as measured by SEM. [40–42] Typical layer thicknesses used in solar cells are about 500 nm, so the surface roughness can represent an appreciable fraction of the layer thickness. The CdS layer nucleates and grows on top of the SnO_2 surface, so the CdS grain size and orientation, as well as the degree to which the CdS layer covers the TCO, are expected to depend on the condition of the SnO_2 layer.

Variations in optical and electrical properties

TCO sheet resistance for SnO_2 has been shown to decrease with fluorine doping, while the optical transmittance increases [43, 44]. Sheet resistance also decreases with increasing layer thickness, but transmittance decreases. In practice, neither of these effects are of great concern, since the as-received substrates have acceptable macroscopic sheet resistances, and there are so few photons in the SnO_2-sensitive part of the spectrum, that the implications for current generation are minor. In deposition methods where the TCO material is carried by a transport gas it is important to properly ventilate the spent carrier gas, as failure to do so results in clouding of the film [45]. Since typical SnO_2 grain sizes are somewhat less than the illumination wavelength for the LBIC measurement, variations in electrical properties from grain to grain are not picked up by that technique, and our other measurements average electrical behavior over the whole cell. Hence, the most important considerations for device uniformity relating to the SnO_2 layer arise from the impact of the surface roughness on subsequent CdS growth, and possible macroscopic variations in transparency and resistivity.

5.1.2 Sources of non-uniform CdS

CdS layers, commonly deposited by chemical-bath deposition (CBD), sputtering, or CSS, are employed as the n-type partner in the n-p heterojunction for CdTe based PV. In this section we consider sources of non-uniform physical and optical properties of the CdS layer, which may contribute to variations in the electrical response of the solar cell.

Physical properties of CdS layers

CdS has stable forms in both the wurtzite and zincblende structures. The lattice constants are $a = 4.16$ and $c = 6.756$ Å in the hexagonal structure, and $a = 5.832$ for zincblende. CSS-grown CdS layers tend to have the hexagonal crystal structure, grain size the order of 100-200 nm, random orientation, or slight preference for the (0,0,2) direction [46], and rms surface roughness from tens to hundreds of nm, though this depends strongly on the growth condition. Because CSS-CdS grains are usually larger than the underlying SnO_2 grains, conformal coverage of the SnO_2 layer is often an issue [46–48]. CdS films are also

susceptible to the formation of pin-holes and discontinuities, possibly resulting from surface contamination of the SnO_2 TCO layer [49]. It was shown that for thin CdS layers ($\sim$ 10 nm) grown by CBD, discontinuities (voids in the CdS layer) up to 20 μm in dimension may exist, exposing the underlying SnO_2, along with μm-sized (or smaller) pin-holes. These layer defects decreased as the thickness increased towards 100 nm.

All of these effects can induce non-uniformities in CdS/CdTe junction performance. Variable lattice mismatch between randomly oriented CdS grains and CdTe with zincblende structure and $a = 6.5$ Å implies a distribution of recombination velocities at the CdS/CdTe interface, and pin-holes or discontinuities may result in local shunting or formation of SnO_2/CdTe junctions, with different properties from CdS/CdTe. Individual CdS grains are again smaller than the resolution of LBIC, but the effects of CdS-based non-uniformities are often evident over larger distances, particularly when the density of pin-holes or discontinuities is locally high.

Optical properties of CdS

CdS thin films generally exhibit an optical band-gap of about 2.4 eV, making them highly absorbing for wavelengths less than 520 nm. A plot of the absorption coefficient vs. photon wavelength is shown in figure 5.1

The optical absorption data allows prediction of the shape of the QE curve in the low-wavelength region of the spectrum for a given thickness, which is a useful comparison for the thickness determination method described in chapter two. Optical properties of CdS may change during cell processing. For example, Lee *et al.* [51] showed that the optical transmittance of sputter deposited CdS films changed after annealing with $CdCl_2$. Non-uniformity in the layer thickness or transmittance can cause non-uniform current generation in the solar cell, though these effects are probably minor over small lateral distances (microns to millimeters) if the deposition process is well controlled.

5.1.3 Effects of non-uniformities on solar cell junction properties

From the discussion above, a range of possibilities for the n-p junction exist. The contact could be CdS to CdTe, with a range and distribution of interface defect densities based

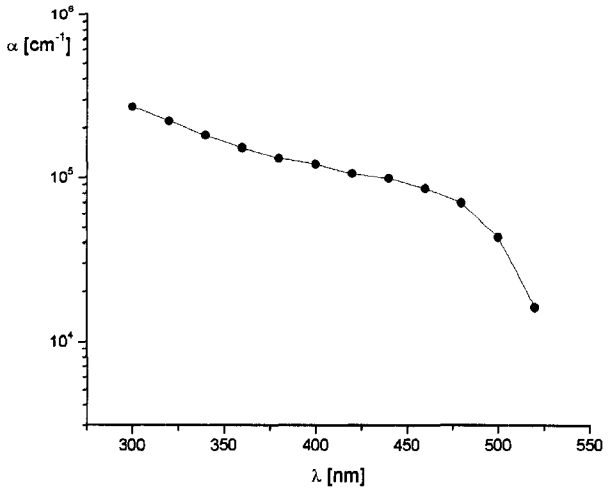

Figure 5.1: Absorption data for thin-film CdS [50]. The absorption coefficient in the range 2.4 - 3.0 eV allows a good estimate of the CdS layer thickness based on the QE data in the 400-500 nm range.

on lattice mismatch, though interdiffusion of CdS and CdTe in subsequent processing may reduce grain-scale variations in the optical and junction properties. Layer discontinuities or pinholes may lead to abrupt lateral transitions between CdS/CdTe and TCO/CdTe junctions, with strongly differing properties. Gradients in CdS thickness may be responsible for changing densities of pin-hole defects on mm or even cm scales, and are typically the result of grosser aspects of the processing, such as thermal gradients which may exist across the substrate and source, and spatial distribution of the source material within the crucible.

When thin CdS is employed to encourage greater current generation, the potential for such variations increases. For this reason we'll consider briefly the properties of the range of n-p junction conditions that may be formed.

CdS/CdTe junction

The target CdS/CdTe junction is that of the present record device, with V_{oc} = 850 mV, J_o = 10^{-9} mA/cm^2, A = 1.9. Devices in the present work which use thick CdS layers typically have $V_{oc} \sim$ 800 mV, $J_o \sim 10^{-5}$ mA/cm^2, and A $\sim$ 2. Where numerical modeling is used, the parameters for the CdS and CdTe layers are assumed to be similar to those given in

[50], with the exception of the thickness, as this model reasonably faithfully reproduces the J-V curve of the record device to-date.

SnO_2/CdTe junction

SnO_2 is usually strongly n-type because of intentional oxygen deficiency, and the conductivity is enhanced by doping with fluorine. The band-gap is 3.6 eV corresponding to illumination at $\lambda = 345$ nm. Electron affinities χ_{SnO_2} are reported in literature in the range 4.4-4.9 eV [52, 53]. One often encounters the terms electron affinity and work function used interchangeably, since the doping levels ($N_d > 10^{20}$ cm^{-3}) make the semiconductor degenerate, with the fermi-level and conduction-band-minimum at very nearly the same energy. The degenerate doping level also smears the measured electron affinity due to high population of the lower states in the conduction band. Uncertainty in the work function for SnO_2 confuses the description of the junction that may be formed with CdTe, since the conduction band offset, the maximum field strength and the subsequent depletion width in CdTe will depend on the difference between the SnO_2 and the CdTe electron affinities.

To establish the context for variability of SnO_2/CdTe junctions, we will consider the extremes of junction properties based on the cited values for the SnO_2 electron affinity. Assuming a CdTe electron affinity of 4.4 eV [50], and SnO_2 is at the low end of the reported range, then there will be minimal CBO at the interface. For an absorber carrier concentration of $p = 2 * 10^{14}$ cm^{-3}, the bulk fermi-level should reside about 0.3 eV above the valence band in bulk CdTe, so that the band bending in CdTe will account for a further 1.2 eV energy barrier to forward electrons. In the case of $\chi_{SnO_2} = 4.9$ eV, the cliff-like conduction band offset is 0.5 eV, and the band bending in CdTe is reduced to 0.7 eV for the carrier concentration as before. This is illustrated in the simulated band diagrams and J-V curves of figure 5.2.

The primary effect of the large cliff offset is to reduce the voltage in the J-V curve. Because of the reduced band-bending in CdTe with the 0.5 eV offset, relative to the 0.1 eV case, the flat-band condition and corresponding onset of forward current flow is reached at much lower values of applied voltage. Moreover, the field-aided collection of photocurrent is marginally reduced because of the weaker field strength, and shallower depletion width in

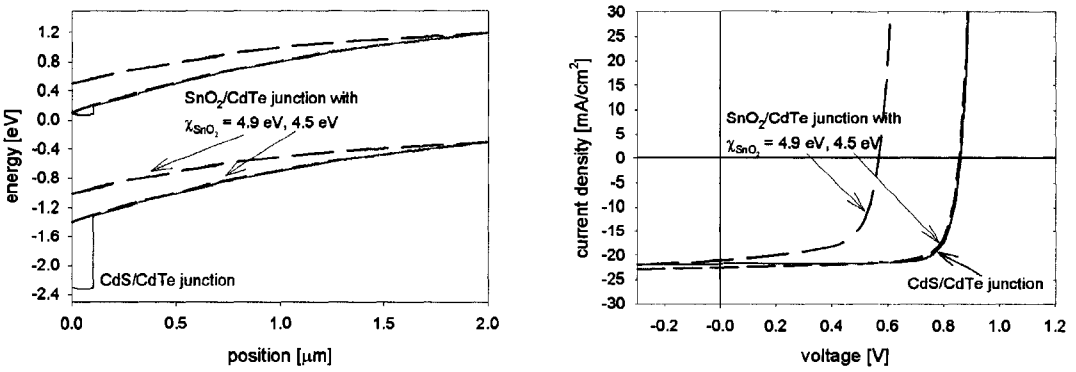

Figure 5.2: Simulated band diagrams and J-V curves for two SnO_2/CdTe junctions and CdS/CdTe. When CdS is present (red J-V and band diagram curves), the electron affinity of the SnO_2 layer does not strongly impact the cell behavior, because the band profile of CdTe, where most of the light absorption and current transport takes place, is determined by the CdS/CdTe junction. Without CdS, the cell voltage depends strongly on the (uncertain) electron affinity of SnO_2.

the high-barrier case. Photocurrent is weakly reduced as a result. With a CdS layer present, the CdTe layer is not allowed to 'talk' to the SnO_2, and the J-V behavior is controlled by the CdS/CdTe junction, with very little effect from the CdS/SnO_2 interface, even though some bending of the CdS bands may occur at the front surface.

The quality of the SnO_2/CdTe junction is also influenced by the interface recombination velocity. As shown in figure 5.3, the voltage depends mostly on the electron affinity, but the efficiency responds to the recombination velocity because of gains realized in both J_{sc} and fill factor. The lower recombination velocity effectively produces a longer lifetime, so that collection is improved at all voltage biases. It should be noted though, that this one dimensional simulation discounts other factors which could set a lower bound on the recombination velocity. Grain-boundary effects are not included, and the potential for enhanced bulk recombination in CdTe due to contamination by defects from the SnO_2 is also ignored. From comparison with experiment, unintentional SnO_2/CdTe interfaces produced by industrially relevant processes probably fall in the range of fairly high $\chi_{SnO_2} = 4.8 - 4.9$ eV, with interface recombination speeds in the $10^6 - 10^7$ cm/s range, approaching thermal velocities.

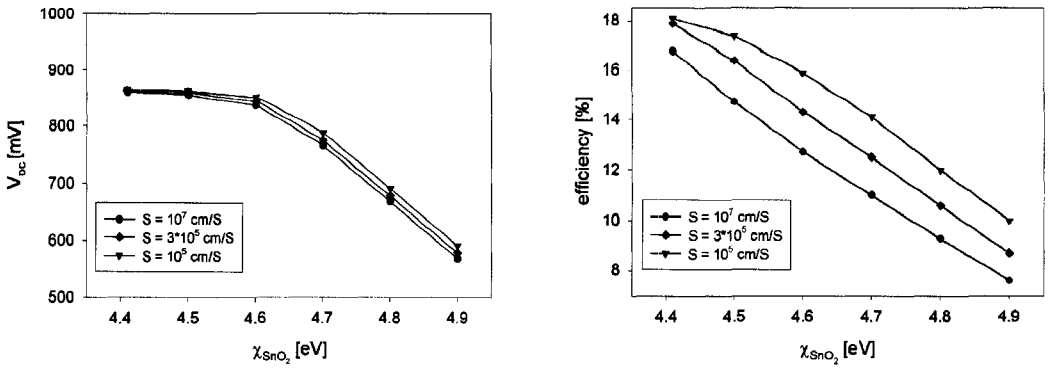

Figure 5.3: Simulation results for V_{oc} and η as a function of SnO_2 electron affinity and various values of the interface recombination velocity. V_{oc} depends strongly on the SnO_2 electron affinity for SnO_2/CdTe junctions. Efficiency benefits from improved FF and current collection due to low recombination velocity, even at small offset values.

5.2 Front-contact experiments

Two experiments were undertaken to investigate the effects of non-uniformities in the front-contact region of the solar cell. In both cases the variable of interest is the thickness of the CdS layer, and we show how too-thin layers cause performance loss consistent with influence from the parallel SnO_2/CdTe junction.

5.2.1 CSU devices: effects CdS thickness variation on CSS CdS/CdTe solar cells

Description of experiment

Thin-film CdS/CdTe solar cells were fabricated using the in-line CSS pilot deposition line in the MEL at Colorado State University, as described earlier in this thesis. All deposition parameters were held constant with the exception of the CdS source temperature, which was varied to control layer thickness. The 'base' process has been optimized for $\sim$ 140 nm CdS deposition. A hotter source translates to a thicker deposition, while a cooler one yields devices with thin CdS. Some variation of CdS layer thickness across the 3" x 3" substrate is to be expected for the non-standard process and the results presented here are not to be understood as indicative of typical process tolerances. Each deposition can yield up to 15 individual devices, and four were extracted from two substrates for a total sample set of 8

devices; 4 with nominally 'thick' CdS and 4 with nominally 'thin' CdS.

Characterization results

The spectral response for all eight devices shows the variation in CdS thickness among the sampled cells. It is important to note that the four devices with 'thick' CdS come from a single glass substrate and deposition. The same is true for the four 'thin' CdS devices. From the QE data in the 400-500 nm range, we estimate optical CdS thicknesses from about 10 to 100 nm for the 'thin' deposition, and 150-240 nm for the 'thick' run. From these data, on can conclude that the average CdS thickness may vary strongly over a length scale of centimeters. While it is not the focus of this work, modeling of module-scale performance based on this level of non-uniformity is an important topic for future study, as industry strives to improve commercial-sized products. Also evident from the spectral response curves is the modest decrease in collection of photogenerated carriers in thin-CdS cells for wavelengths near the band-gap. We attribute this to a shorter electron lifetime for thin-CdS devices, or to a larger J_o. Increasing J_o with decreasing CdS thickness is consistent with measured J-V parameters, as discussed below. The device with thinnest CdS has a slightly steeper band-gap cutoff at long wavelengths. This may relate to insufficient CdS for saturation of the CdTe layer with band-gap-reducing sulfur [54, 55]. Other than slight variations in the photocurrent, cells

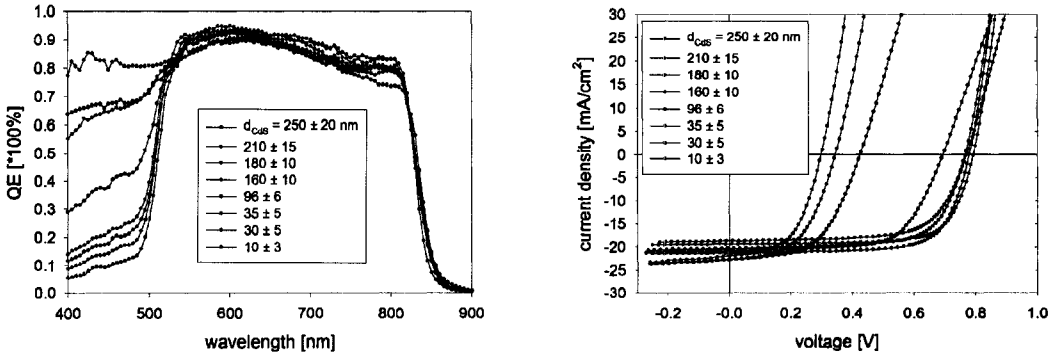

Figure 5.4: CdS layer thickness is inferred from QE data in the $400 < \lambda < 500$ nm range. When the CdS layer is thinner, photocurrent increases slightly. However, below about 100-nm layer thickness, V_{oc} and FF suffer more dramatically, reducing overall device performance. The likely culprit of reduced performance is transition to performance dominated by the weaker SnO_2/CdTe junction.

with thicker CdS show little difference in performance, so CdS thickness greater than about 150 nm may be considered infinite for practical purposes. The same absolute differences in CdS layer from one cell to the next have a much greater impact when the average thickness is less. J-V measurements on all devices are summarized in figure 5.4

A transition region from relatively constant voltage and efficiency at high CdS thicknesses to another (broader) grouping at low thicknesses is apparent in the 40-100 nm range. Apparently there are two regimes of device behavior, dependant on the CdS thickness, and the layer properties, and hence the quality of the solar cell junction change significantly between 35 and 100 nm. The agreement with calculations from section 5.1.3 suggest that the higher efficiency regime is controlled by a CdS/CdTe junction, while the lower performance corresponds to the SnO_2/CdTe junction. However, the behavior of the 'real' cell with thin CdS cannot be modeled simply by one or the other type of junction, since *some* CdS is obviously present. The logical supposition is that there is a shared influence of both types of junction, so investigation of device uniformity is necessary.

The losses in V_{oc} and fill factor that accompany reduction in CdS thickness correlate with increases in lateral variations of photocurrent response at 100-μm resolution. LBIC data of devices from the 'thick' deposition shows that 160 nm of CdS is equally effective as 250 nm at preventing lateral variations on the small scale. LBIC of thin-CdS devices, on the other hand, reveals variations of some few per-cent on the few-hundreds-of-microns scale.

The variations seen in scans of devices with fairly thin CdS can be simply explained in terms of non-uniformity of the junction. Although the primary difference between SnO_2/CdTe and CdS/CdTe junctions was seen from simulations to be the device voltage, some reduction in the short-circuit collection was also evident. One possible explanation, then, for the areas in the LBIC scans of devices with very thin CdS (within a factor of two of the likely SnO_2 surface roughness) that show collection reduced by 2-10 % is an incomplete coverage of the SnO_2 layer by the CdS deposition. Where a SnO_2/CdTe junction prevails, the reduced band-bending weakens the collection of photocurrent, so the LBIC response is reduced. Even a slight gradient of a few angstroms CdS thickness per micron of lateral distance could induce a transition from a regime of dominating CdS/CdTe junction

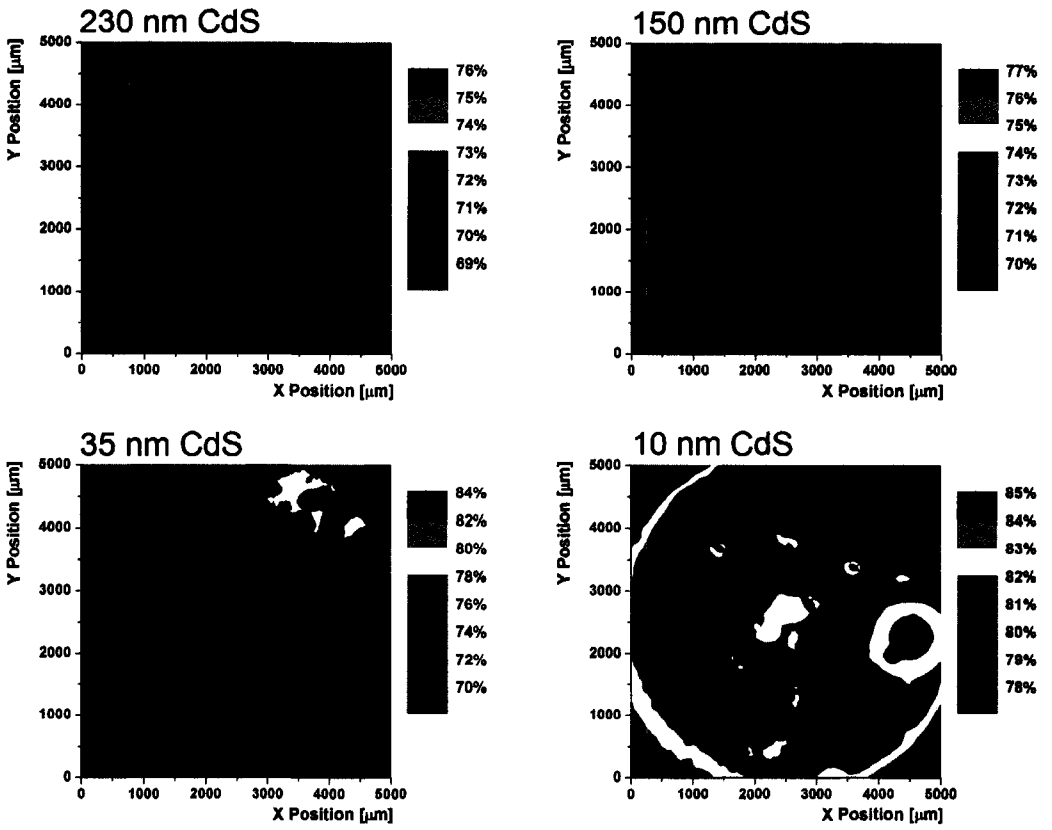

Figure 5.5: Low-resolution LBIC data for representative thick (top) and thin (bottom)-CdS layer devices. The variations obvious in thin-CdS devices may be indicative of SnO_2/CdTe junction regions in parallel with CdS/CdTe.

to SnO_2/CdTe junction over the size of the lab-scale cell under consideration here. That the cell with the thinnest CdS layer shows less variation than devices with $\sim$ 30 nm layers may be because the majority of the cell surface is a (somewhat) uniform SnO_2/CdTe junction, with non-uniformities caused by intermittent separation of the TCO and absorber layers by the thin CdS. This is suggested by the photomap for that cell, which features islands of *higher* response against a background of lower average QE.

5.2.2 University of Toledo devices: CdS layer thickness variation in RF sputtered CdS/CdTe solar cells

After the previous study, a collaboration with the University of Toledo (UT) was initiated to investigate whether a strong dependence on the deposition method exists, as to the

formation of parallel SnO_2/CdTe junctions. The UT devices were fabricated by the RF sputtering technique, which tends to produce smaller grains than CSS. Since the supposition from the previous study is that incomplete coverage of the SnO_2 by evaporated CdS is largely responsible for performance losses at low CdS thicknesses, performing a similar study on devices from a different fabrication technique may yield different results. Two main questions were addressed: (1) does the CdS thickness play a dominant role in the cell behavior as before? and (2) if the trend is similar, does the transition from SnO_2/CdTe dominated to CdS/CdTe dominated behavior occur at a similar value for CdS thickness when the layers are deposited by RF sputtering? We also looked at the degree to which non-uniformity of these cells was influenced by the CdS thickness.

Experimental

CdS and CdTe layers were deposited at the University of Toledo by RF sputtering onto SnO_2:F coated glass substrates (Pilkington TEC-7). The deposition parameters are detailed in publications from that lab [7, 56]. For this study, CdTe thickness was restrained to two microns, to facilitate comparison between these devices and the evaporated devices discussed before. Back-contacts were deposited through a mask with several circular holes of varying sizes, to complete between sixteen and twenty devices per substrate. Six depositions were performed with variation in the sputtered thickness of the CdS layer, and all subsequent processing was identical. The CdS thicknesses as deposited were 0, 30, 45, 80, 160 and 230 nm.

Measurement results and discussion

The results of QE and J-V measurements are given in figure 5.6. In very similar form to the evaporated cells from the previous study, the short-wavelength QE reflects the CdS layer thickness, and the thin-CdS devices show poorer long wavelength collection than for thicker layers. The device with no CdS presents an earlier band-gap drop-off in the QE, suggesting that the CdTe band-gap of the other devices is reduced by sulfur alloying during subsequent processing. Using the same method as before to determine the CdS thickness it is estimated that 15-25 nm of CdS is consumed in all of the CdS-containing devices. Transition to lower

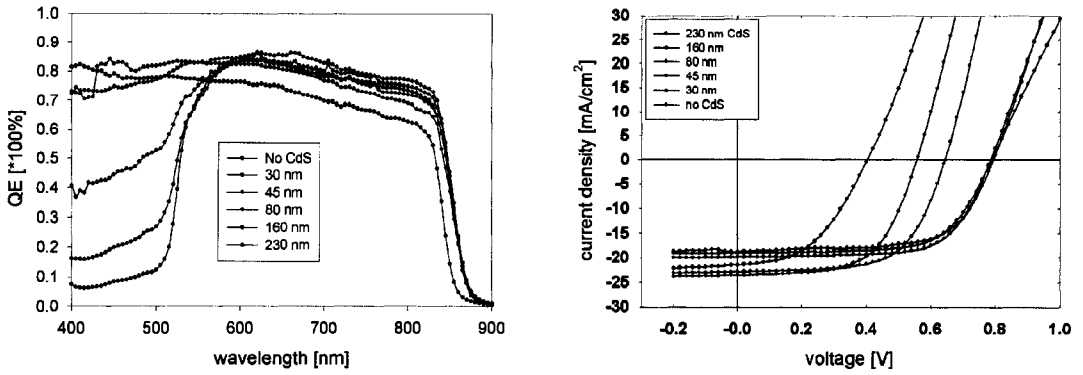

Figure 5.6: V_{oc} is virtually constant for the sputtered devices for CdS thicknesses down to 80 nm (as deposited). All devices with high CdS-region QE have reduced V_{oc} and FF.

V_{oc} and fill factor as CdS becomes thinner is observed in the J-V data, countering the increased J_{sc}, so that performance decreases. Since the performance is almost identical for all cells with $D_{CdS} > 80$ nm as-deposited we conclude that although there is a similar drop in performance as with the CSS devices, the sputtering process is tolerant of somewhat thinner CdS layers before performance begins to suffer. We can estimate that the onset of voltage loss would occur in the 40-60 nm range of CdS thickness, and studies of devices with intermediate CdS layers are ongoing.

Table 5.1: Sulfur/tellurium interdiffusion is reported to occur during $CdCl_2$ annealing and results in thinner effective CdS layers than were deposited.

Device ID	632′	632	631	629	627	622
As-deposited CdS thickness [nm]	0	30	45	80	160	230
QE-inferred CdS thickness [nm]	0	5 ± 5	15 ± 3	65 ± 5	130 ± 10	210 ± 20

The uniformity of the sputtered CdS/CdTe devices tells a somewhat different story than that of the evaporated cells. None of the devices show a particularly high incidence of 100-μm-sized features like the evaporated devices, other than 'dead' spots likely associated with probe damage incurred while contacting for other measurements. Instead, the most noticeable uniformity problems with these devices seem to be associated with the edges. The device with no CdS in particular has an edge related resistive defect, which expands in influence drastically under moderate forward bias (bias photomap not shown). This feature is the likely cause of the somewhat shunted J-V curve. It is suspected that the higher

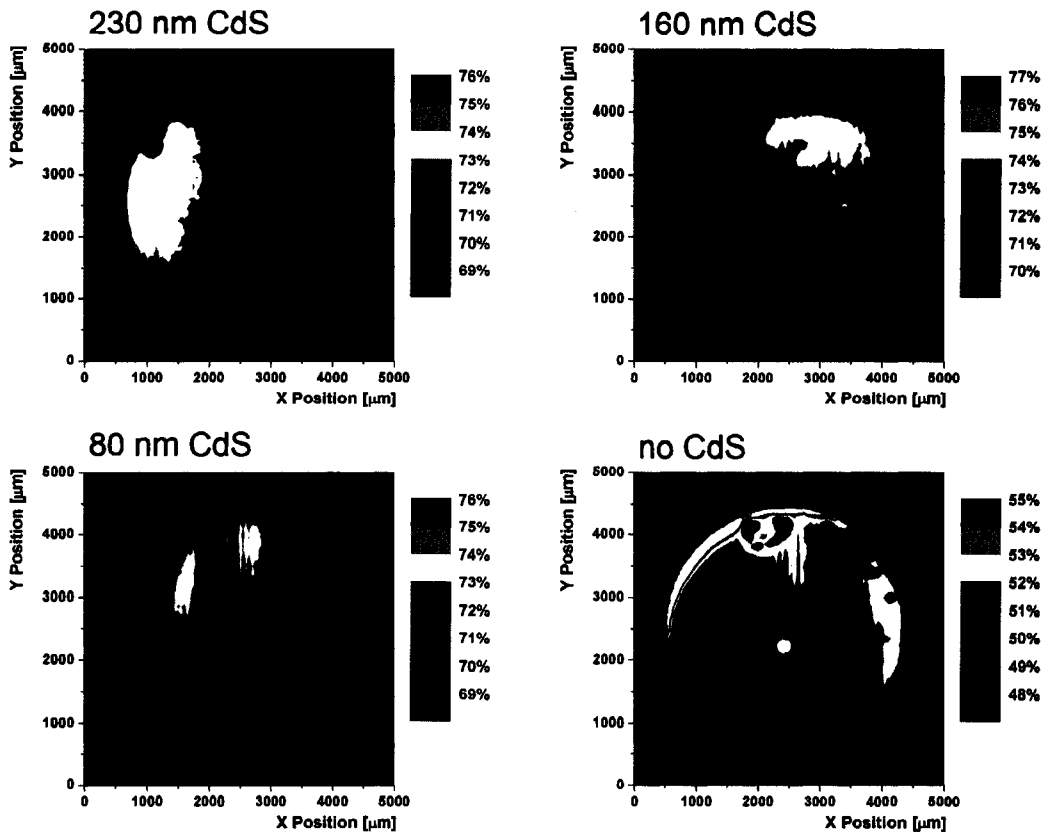

Figure 5.7: UT devices do not show strong variations on the same scales as the CSU devices. Instead edge-related effects seem to be responsible for the dominant LBIC features and may largely control the performance.

ratio of edge-length to device area for these devices allows the more serious edge effects to obscure small-scale variations of the type seen in the CSU cells. Moreover, the very small grain-size (less than 100 nm) characteristic of sputter deposition may set CdS layer defects out of the range of LBIC resolution. The reader is referred to the high-resolution data of fig. 2.13. These scans, from another UT device, shows only modest variations of 1 to 2 % at the highest resolution of the LBIC measurement, suggesting that SnO_2/CdTe junction regions, if they exist, are very small and scattered.

Whether the mechanism for the performance loss at low thickness is formation of SnO_2/CdTe junction areas, increased shunting, depletion of the CdS layer for low thicknesses, or some other phenomenon, it still clearly relates to the CdS thickness parameter, and so while the nature of the weak contribution may be different, it should still agree with

a thickness-dependent model for transition between weak and strong behavior.

5.3 Comparison with modeled non-uniformities

We have seen that one of the more significant effects of the SnO_2/CdTe junction, as opposed to the CdS/CdTe junction is a lower V_{oc}, and it has been suggested that this arises because of the large cliff-offset present in the conduction band, reflecting the electron affinity of SnO_2. J-V data can be interpreted to imply that in thin-CdS devices, the behavior tends toward that of the modeled SnO_2/CdTe junction. Especially for evaporated cells, this coincides with decreased device uniformity as indicated by LBIC. The next obvious question is whether we can describe a device which is clearly not all of one type or the other, but a non-uniform mix of the two. Furthermore, can we relate the strength of influence from the weaker SnO_2/CdTe junction to the CdS thickness? A model was developed by Kanevce [57] to predict overall device voltage based on the input parameters of the strong and weak V_{oc} values, the percentage of area with low V_{oc}, and the sheet resistance of the TCO. In the absence of sheet resistance, the effects may be calculated analytically. Her model lends itself well to our situation, since the voltage is the dominant (though not the only) difference between of SnO_2/CdTe and CdS/CdTe cells (from simulations) and is also the main difference observed in cells with thin and thick CdS.

5.3.1 The Kanevce model for non-uniform V_{oc}

The model proposed in [57] for overall performance of a solar cell with parallel strong and weak junctions assumes uniform photocurrent generation. While LBIC showed that this is not true for the practical devices of interest, the differences in current collection at the LBIC wavelength are overshadowed by the expected differences in voltage for the varying junction conditions–up to 50 %. If the device is modeled as a network of n micro-diodes with identical area then the device current can be expressed as the sum of currents from the individual diodes:

$$I_{tot} = \sum_{i=1}^{n} I_{0_i}(e^{qV/AkT} - 1) - I_L. \tag{5.1}$$

where the assumption of uniform light generated current makes I_L independent of the sum and I_{0_i} is the saturation current of the i^{th} diode. Under the assumption of only two types of diode, labeled strong and weak, the sum has only two terms and then the open circuit voltage—the voltage at zero total current—is

$$V_{oc} = \frac{AkT}{q} ln \left(\frac{I_L}{sI_{0s} + wI_{0w}} - 1 \right) \tag{5.2}$$

where $s + w = n$, the total number of diodes in the sum, and I_{0s}, I_{0w} are the saturation currents for the strong and weak diodes respectively. One might alternatively describe the solar cell by the strong and weak areas. The weak-area-fraction a is defined as $w/(s + w)$, and the strong area is the compliment to this quantity. Then the device voltage can be written as

$$V_{oc} = V_{ocs} - \frac{AkT}{q} ln \left(1 - a + ae^{\frac{q(V_{ocs} - V_{ocw})}{AkT}} \right) \tag{5.3}$$

labeling the individual strong and weak diode voltages as V_{ocs} and V_{ocw} respectively. From equation 5.3 it is clear that the inputs to model calculations are the strong and weak V_{oc} values, and the weak area fraction. Equivalently, one may specify strong and weak saturation currents in equation 5.2.

The only remaining parameter necessary for the analysis is a, the weak area fraction. The approach developed to relate a to the CdS thickness is described in the next section.

Relation of CdS thickness to 'weak' area

The form for the expression used to relate the strong/weak area to the CdS thickness comes from the following thought experiment:

Understanding that the SnO_2 surface is rough, we consider the possible growth processes for the CdS layer. Since the final layer is polycrystalline, at the nucleation stage the CdS layer must consist of islands of CdS on the SnO_2, which form the precursors for the eventual CdS grains. Until the grains become high enough that they spread to touch one another, the islands remain isolated. In the CSU process, the CdS grains are larger in diameter than the SnO_2 grains, so that they do not pack together tightly because of the SnO_2 roughness.

In the sputtering process, though, the size of CdS grains (as deposited) is of the same order as the SnO_2. Even if they do not cover the TCO grains one-to-one, the condition where neighboring grains come into contact is likely arrived at with less total thickness of the layer. In either case, there should be a thickness of CdS at which there is a transition from incomplete to complete coverage of the SnO_2 layer. If CdTe is deposited on an incompletely formed CdS layer, then most CdTe grains will have some contact to the SnO_2 layer, such that the low voltage regime prevails. Once the CdS layer reaches the critical thickness (different for the two deposition methods), the subsequent CdTe growth is likely to remain separated from the TCO, so that the CdS/CdTe junction dominates the behavior, with only modest influence coming from locations where pin-holes or discontinuities allow widely separated points of contact between CdTe and SnO_2.

With this idea in mind, a reasonable description of the weak (i.e. effective SnO_2/CdTe) and strong (CdS/CdTe) area fractions would be a function of the form

$$a_s = \frac{1}{1 + e^{-(d-\delta)/f}} \tag{5.4}$$

with

$$a_w = 1 - a_s \tag{5.5}$$

where a_s describes the strong area fraction, d is the thickness of the CdS layer, δ is the characteristic thickness necessary for effective coverage of the SnO_2, and the form factor f describes the range of thickness over which the transition from weak to strong behavior occurs. The key feature of this type of functional relationship, is that approaching the transition region from either direction causes very little change in the overall behavior. For the increasing thickness regime it may be expected that until the CdS grains become fully formed, CdTe can still come somewhat into contact with the SnO_2, and that if any part of the CdTe grain contacts the SnO_2, then all the current for that grain effectively flows through that junction when the device is operated in forward bias.

Application of LBIC analysis

From the previous discussion, the critical thicknesses of CdS should correspond to the greatest variations in LBIC data so long as the thickness-driven junction non-uniformities are visible at LBIC resolution. Figure 5.8 shows the full-width-half-maximum values for histogram distributions of the LBIC scans of all cells in both the CSU and Toledo studies plotted against the CdS thickness inferred from whole cell QE measurements.

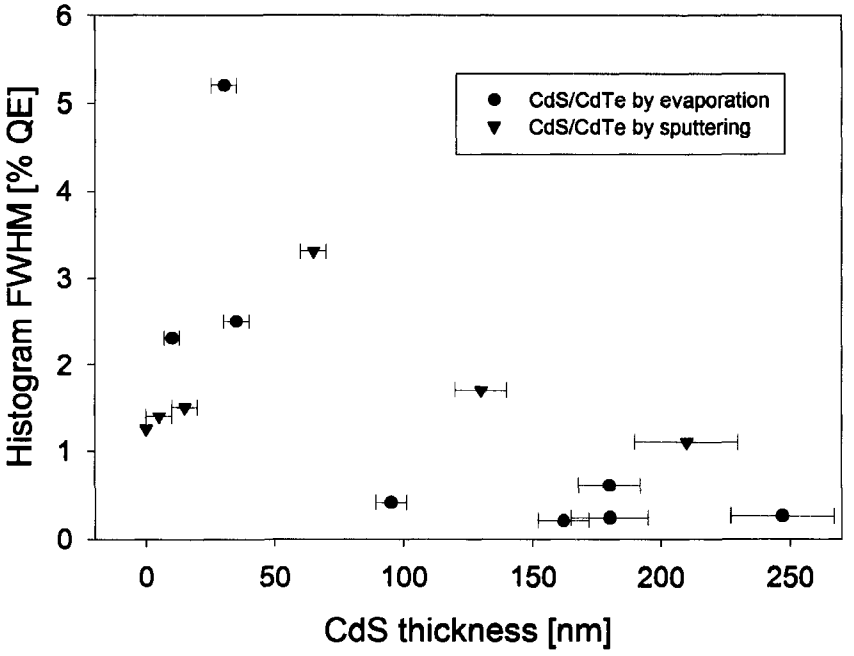

Figure 5.8: The peak in non-uniformity for devices with CdS thickness between about 30 and 60 nm coincides with the transition region from SnO_2/CdTe to CdS/CdTe junction inferred from J-V data. The critical CdS thickness for evaporated devices based on SnO_2-coated window glass is concluded to be in the range of 30 nm.

As discussed previously, the LBIC data of sputtered devices is rather dominated by effects at the edges. While variations due to parallel junctions may exist, they are probably too small in dimension—reflecting the more conformal coverage of SnO_2 by smaller grains—to show up against the edge effects. For the UT cells (green points) the largest variations in the LBIC data are not observed in devices with thin CdS.

A correlation does exist, however, for the CSU devices. At the lowest thicknesses of CdS, junction variations are somewhat suppressed. The average performance of the junc-

tion may be low (low V_{oc}, as predicted in 5.1.3), and variations are not completely absent, consistent with the uncertainty in the SnO_2 electron affinity and interface condition, but non-uniformities of a dominantly SnO_2/CdTe junction are apparently less than the variations observed when parallel SnO_2/CdTe and CdS/CdTe junctions are present. For this reason, FWHM values are reduced at low CdS thicknesses, then climb to a maximum in the transition thicknesses, where J-V behavior changed from low-V_{oc} dominated to high-V_{oc}.

To test whether the non-uniform V_{oc} model (section 5.3.1 and the empirical relation developed for a within the model are consistent with experimental observations, a LabView routine was developed to perform the calculations of eq. 5.2 for a range of CdS thicknesses. The parameters for variation are the quality factor A, the form factor f, the strong and weak V_{oc} values, and the user-defined characteristic thickness of CdS necessary to transition from the SnO_2/CdTe to the CdS/CdTe regime. The results are shown in figure 5.9.

The smooth curves in the plots are the output of the fitting calculations. The input parameters were selected by first setting J_o to the ranges for the extreme groupings of points. Then the quality factor A was selected within the range of experimentally determined values. It should be noted that the discrepancies between measured V_{oc} values and the output of the model are consistent with differences between A-factors obtained for the individual cells and the single A used in the calculations. δ and f were then adjusted so that the J_o curve best agrees with the transitional points at intermediate CdS thicknesses. This procedure yields good fits to the J_o and V_{oc} data.

The curve for J_{sc} is calculated as

$$J_{sc} = J_{absorber} + 0.8 * \int I_{spect}(\lambda) * e^{-\alpha(\lambda)d} d\lambda. \tag{5.6}$$

The integral is taken from 300-510 nm and represents current generation from the photon flux (I_{spect}) transmitted through the CdS window of thickness d, and collected with 80 % QE in the absorber. $J_{absorber}$ is the base-level current generated by CdTe absorption from 520-850 nm.

Fill factor is calculated based on V_{oc} as outlined in Green [58]. Since the model applied here does not account for parasitic resistances, and these can have a strong effect on the

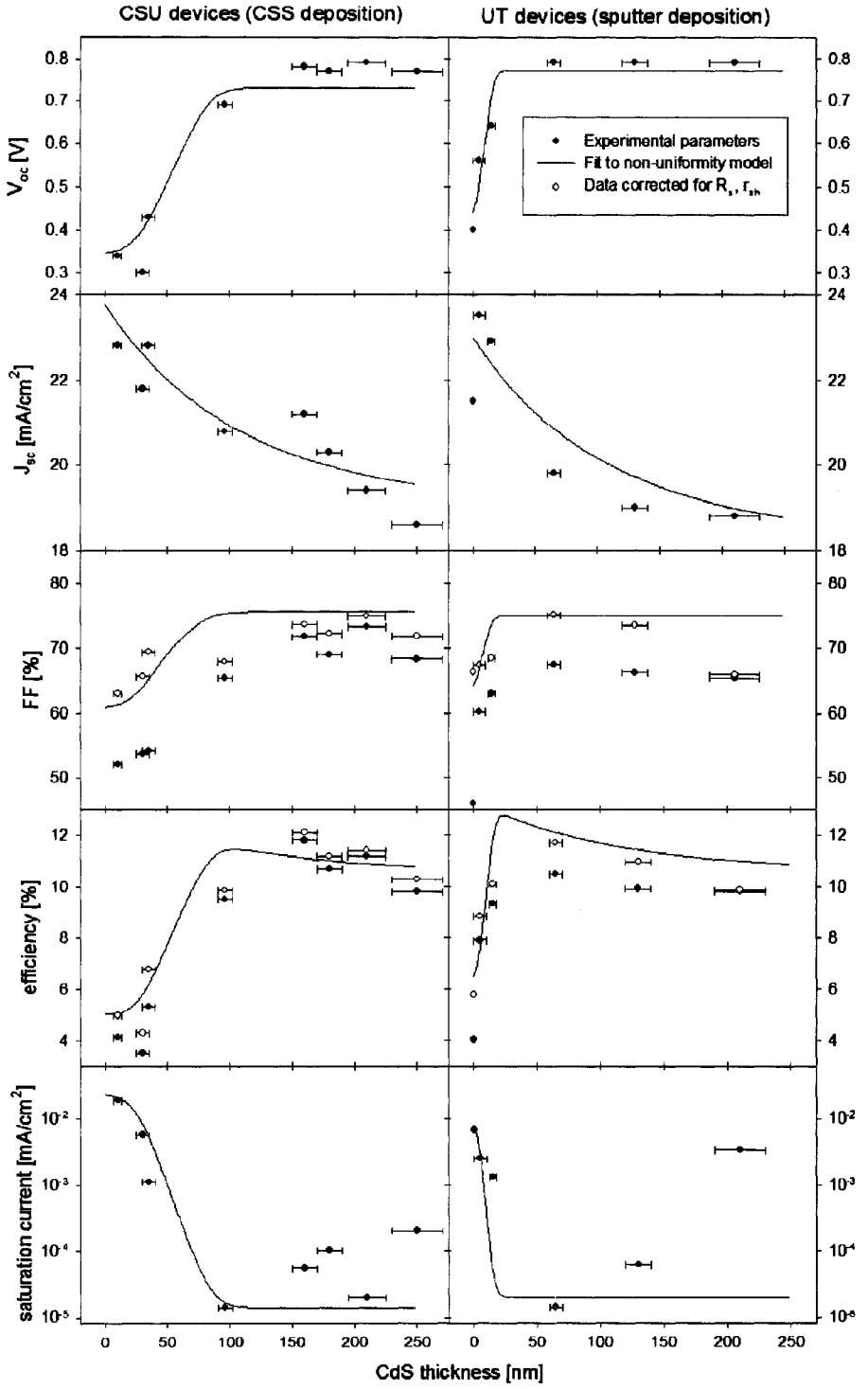

Figure 5.9: First and second level parameters from J-V measurement plotted for CdS thickness inferred from QE. Since the non-uniformity model applied does not include the effects of series and shunt resistances, the FF and efficiency data are plotted without (filled points) and with (open points) series and shunt resistance correction.

fill factor, two sets of points are plotted for FF and efficiency. The open points represent the resistance-corrected values for FF and η using the procedure also described in [58] for determining the ideal FF in the absence of series or shunt resistances.

Non-uniformities which may plausibly be associated with the front contact region of the solar cell have been shown to be correlated to performance loss, mainly in the form of reduced voltage, in CdS/CdTe cells with thin CdS layers. The connection is especially strong in CSS-deposited devices. In sputtered devices, where smaller grain-size is likely to translate into improved coverage of the SnO_2 layer, the uniformity correlation with the performance is weaker. We suspect that this is due to two factors: (1) a much smaller defect size, such that the weak points are averaged with their stronger surroundings in the LBIC measurement, resulting in low-magnitude variations and (2) the presence of large-area edge defects, which dominate the appearance of 2-D photomaps of UT devices. Despite the weak uniformity trend, the range of observed performance is reasonably consistent with the expected performance for a device with simultaneous influence from SnO_2 and CdS junctions with CdTe. The strength of this influence varies with CdS thickness and a 'critical thickness' can be identified for each of the deposition techniques. From these investigations it is recommended that care be taken in device fabrication to ensure uniformity of the front contact, particularly as relates to separating the CdTe absorber from the SnO_2 layer.

Chapter 6

Suggestions for improving front-contact uniformity

From the results of the last chapter, variations in the front contact properties that translate into primary junction issues are to be strongly avoided. Probably the most important non-uniformity to address is the continuity and homogeneity of the CdS layer, in order to prevent parallel junctions of the CdTe directly with the SnO_2. The characterization featured here does not directly probe the physical properties of the contact layer such as the roughness of SnO_2 and the intermittent coverage of the CdS layer, which are suspected responsible for performance losses. However, the performance behaves fairly predictably based on assumptions about the influence of weak junctions associated with thickness of the CdS layer.

The likelihood of problems arising from non-uniform CdS outweighs the potential gains achievable when CdS is thinned beyond a process-dependant critical thickness. Therefore, CdS should only be thinned if measures can be taken to discourage the incidence of contact-related non-uniformities and thus reduce its critical thickness. In this chapter, we briefly discuss the inclusion of a high-resistance buffer layer, encouragement of small-grain CdS growth and the possibility of actively smoothing the TCO layer. All of these approaches are intended to address front-contact-uniformity issues with a minimum of necessary adaptation of the CSU process. Even so, each represents a departure from the fully contained, in-line

deposition concept.

6.1 Bi-layer TCO

The most widely applied strategy to reduce chances of non-uniform junction formation, is to include a high-resistance-transparent (HRT) layer between TCO and CdS. Several groups have had success with this approach, using SnO_2:F/i-SnO_2 [10], CTO/ZTO [11] and ITO/In_2O_3 [16] to name only a few. With this configuration, excess forward current flow from the TCO to CdTe is discouraged. Another interpretation would be that the high-resistance layer increase the thickness of the *i* layer in an n-i-p structure, which prevails if CdS is very thin, or highly compensated, and CdTe doping is low. Uniformity of photocurrent generation was characterized by electroluminescence at the Colorado School of Mines and LBIC at CSU and was found to be improved with the HRT layer in [42]. Though the underlying sources of non-uniformity are not addressed this way, their effects are minimized. However, for compact, industrially scalable processes like the pilot line at CSU where the TCO layer is not prepared in-house, application of a secondary intrinsic layer to the as-received conductive layer may represent a significant change to the overall process. Since the deposition line at CSU is so flexible, and partially modular, perhaps a front-end evaporator for i-SnO_2 or a separate sputtering station could be adapted for the TEC glass to apply an i-SnO_2 layer before sending substrates into the main deposition chamber.

6.2 Growth kinetics of CdS

If the reduction in critical thickness for sputtered cells relative to evaporated devices is correctly attributed to the difference in grain sizes, then reduction of the CdS grain size would be an attractive approach to allow the use of thinner CdS for the CSU process, since it could potentially be done without significant changes to the fabrication layout or design.

The growth of CSS-CdS was shown by Ferekides *et al.* at the University of South Florida to proceed via smaller and more compact grains when the substrate temperature was initially higher than the CdS source [59]. The time constraints of the CSU process (2 min. at every deposition) prohibit as fine a control as was exercised in that study.

However, the substrate could be heated to a slightly higher temperature than the CdS source as an initial condition of the CdS deposition (refer to figure 3.1). Another approach to studying alternative possibilities for CdS layer growth might be to replace the CdTe source with a second CdS source and investigate layers grown with source/substrate temperature profiles using two CdS sources. In this way, one could better reproduce rapid changes in the source/substrate temperature vs. time profile recommended by the results from [59]. One could, for example, arrange the temperature parameters so that the first source was optimized for fine-grained nucleation, and the second source established the final layer thickness. Separating the effects of layer nucleation and growth may suggest a way to change the process to achieve better TCO coverage with a thinner CdS layer using only one station.

Another factor that was identified in [59] to influence the condition of CdS was the O_2 ambient during the layer growth. It was found that higher O_2 concentration encouraged the slower growth of smaller grains. In the CSU system, all stations are subject to a nominally identical residual-gas ambient, which has been optimized for performance of completed devices. It might prove worthwhile to add partial isolation to the various deposition stations, so that the CdS growth condition could have a different O_2 concentration than CdTe or $CdCl_2$. In chapter 3 we saw how the O_2 concentration was critical for high-efficacy $CdCl_2$ treatment. Station-by-station O_2 ambient control is thus doubly recommended, so that each process may be brought to its individual local optimum with respect to O_2 passivation, or so that changing the residual-gas ambient of one deposition does not de-optimize the other steps.

6.3 Addressing surface roughness of SnO_2

The critical thickness for CdS was determined last chapter to be of the order of reported RMS roughnesses of SnO_2:F layers. For sputtering, where small grains dominate, it was perhaps a little less, for evaporation, as much as a factor of two greater. Furthermore, the plateau of device performance was seen to occur for CdS thickness at least twice the critical thickness. For either process, one could expect the critical CdS thickness to decrease if the

SnO_2 roughness were 10 nm or less, allowing the use of thinner CdS layers without risking performance loss due to parallel junction formation.

Studies in the photovoltaic literature have largely focussed on conformal coverage of the TCO layer with thin CdS (i.e. by CBD or other small-grain deposition) or on separation of CdTe from the conductive TCO by other means (HRT layer). Less attention has been given to processes devoted to changing the RMS roughness of the SnO_2 layer itself. A survey of surface preparation techniques from other fields yields a few possibilities which may be investigated for application in smoothing the TCO layer.

Gas-cluster ion-beam irradiation

On the nm-scale, the 6.5 Mohs hardness [60] of SnO_2 films has little meaning, and the surface may be abraded by almost any substance. The roughness of several materials was reduced into the few-nm range by gas-cluster-ion-beam (GCIB) irradiation using argon as outlined in [61, 62]. This technique is akin to sputtering but uses large clusters of atoms (typically the order of 2000 Ar atoms) with only a few ions among them so that large cluster energies may be obtained while the individual particle energies and ion dosage remain low. AFM images in [61] showed smoothing of Cu, Au and diamond surfaces to roughnesses less than 10 nm by normal-incidence irradiation of Ar clusters at 20 keV. A study of the change in critical CdS thickness for the CSU process on smoothed versus unsmoothed glass/SnO_2 substrates may suggest GCIB as a candidate for improvement of front-contact uniformity when using thin-CdS layers.

GCIB bombardment has also been used to do shallow doping. One particularly novel application of this technique may be to *anti-dope* the SnO_2:F surface, effectively combining the smoothing capability of the technique with addition of an i-SnO_2 surface.

SnO_2 surface etch

Perhaps a simpler method, and one which could be integrated into the glass cleaning process already employed prior to semiconductor deposition, is an acid etch of the TCO. SnO_2 is reportedly a fairly difficult material to etch chemically, but etch rates of $\sim$25 nm/min. were achieved recently by Francioso *et al.* using hydriodic acid (HI) [63]. A brief HI-etch should reduce surface roughness since taller grains expose more surface area to the etchant. For either the GCIB sputter, or the HI-etch options an initial investigation should

ascertain whether the surface treatment, which may remove some fifty or more nanometers of material, has a strong effect on the conductivity or transparency of the SnO_2:F.

6.4 Front contact effects summary

As with the back-contact, front-contacts (TCO and CdS layers) to CdTe-based solar cells can harm cell performance through non-uniform properties. Performance loss is especially evident when the CdS layer is made thin. The low-end of the performance spectrum, corresponding to thin or absent CdS reasonably agrees with simulations of SnO_2/CdTe junctions and may as such be largely attributed to parallel influence SnO_2/CdTe and CdS/CdTe junctions. The SnO_2/CdTe junction exhibits low V_{oc}, and depending on the surface recombination, variable current collection and FF. The influence of parallel junctions was predicted by the analytical model of Kanevce, when the 'weak' area fraction was assumed to transition from near one to zero as the CdS thickness passes a critical thickness. The critical thickness appears to be related to the SnO_2 surface roughness and CdS grain size. For CSU devices, LBIC characterization indicated an increase in lateral variations through the transition thicknesses, supporting the notion of parallel areas with different band-structures, influencing the collection efficiency. For UT devices, lateral variations in collection were most likely too small for detection with LBIC, owing to the small grain size of the sputtered CdS layer.

Since effects associated with thin CdS are clearly detrimental to cell performance, some possibilities for reducing non-uniformities in the presence of thin CdS layers were enumerated. One approach, which already has a good record of improvement of otherwise identical thin-CdS devices is the addition of an HRT buffer layer. The present fabrication process at CSU is not equipped for TCO deposition, so the most practical method for inclusion of a bi-layer TCO may be to obtain bi-layer coated glass externally. Alternatively, exploration of process variations for the CdS layer to encourage slower, small-grained layer growth could be undertaken to improve coverage of the SnO_2 layer at intermediate CdS thicknesses. For the CSU process this might include using two CdS sources to allow more sophisticated temperature/time profiles for the CdS growth. Improved isolation of the CdS station in the

deposition chamber could be another 'low-overhead' approach to giving more control over deposition by allowing environmental control of this critical step, separately optimized for CdS layer growth. Lastly, it is plausible that a smoother TCO layer would result in a more uniform CdS layer at low thicknesses. Decreasing SnO_2 roughness could be achieved by gas-cluster ion-beam irradiation, or perhaps by hydriodic acid etching prior to CdS deposition. If any of these strategies for allowing thin CdS proves successful, a re-characterization of the critical CdS thickness will be necessary. Instead of adjusting source temperature to achieve variations of CdS thickness, perhaps an adjustable crucible could be designed for future studies to control the layer thickness via source/substrate separation for the standard process parameters. Ideally, the CdS layer could thus be made thinner without affecting its large-scale uniformity.

Chapter 7

Conclusions

Several investigations were performed on CdS/CdTe thin-film solar cells fabricated by industrially compatible processes, or by high-efficiency lab processes for comparison. The focus of this work includes the likely causes for contact-related non-uniform performance that have a significant impact on the completed devices. Performance was characterized by J-V, QE and capacitance measurements. The results of these measurements were interpreted in the context of knowledge of the fabrication process to establish a physical model for the dominant limitation to device performance on a case-by-case basis. Numerical simulations were made to establish the plausibility of each physical model and to test the extremes of device behavior that the models might predict. LBIC characterization was used to verify the presence of non-uniform photocurrent collection, which could be interpreted as lateral variations in back or front contact parameters that affect the device band structure.

A comment to the application of LBIC studies in this work: The LBIC measurement displays the local photocurrent collection from a 2-D scan over the cell area with a focussed laser beam of comparable power density to the integrated AM-1.5 spectrum. We saw in chapter three that LBIC data was consistent with a model for non-uniformities associated with the back contact of the solar cell. In chapter five we took similar looking photomaps and histograms, and attributed them to front-contact non-uniformities. It is very appropriate to ask how the technique can distinguish between variations originating from different physical phenomena in the solar cell, and how the data may be reasonably

interpreted as front-contact problems, back-contact problems, absorber problems, optical effects, or measurement noise. The answer is that LBIC data is *only* useful in conjunction with other characterization tools that can establish a context for interpretation. By itself, LBIC characterization can indicate that a device does or does not have uniform photocurrent collection, but it can not differentiate among several possible reasons why. Once other device characterization, and perhaps comparison with numerical simulations have established a working model for the average device performance, the LBIC tool can be helpful in identifying the degree of variation of the mechanism that most affects photocurrent collection. It is most reliably interpreted when the development of non-uniformities agrees with band-structure predictions of changes to the collection function under forward or reverse voltage bias. In this work mechanisms relating to front- and back-contact structures were identified, either of which can modify the band structure in the junction region where the LBIC laser light is absorbed. Though the LBIC data in the two studies shared some similarities of appearance, the key cell region in each was identified with confidence.

The significant results of this work fall into three categories.

- The interpretation of LBIC data was advanced by establishing protocols for plotting photomaps and by developing semi-quantitative characterization of histogram distributions of LBIC data using empirical fitting. In some cases, fits to LBIC histograms indicated the extent to which a model accounting for non-uniform influence of multiple mechanisms is relevant or necessary.

- Secondary curvature of J-V curves for devices with significant back-barrier influence was explained with a model including the effects of back-contact related non-uniformities. Fourth quadrant rollover was shown to be correlated with non-uniformity observed in LBIC data. This allowed an extension of the widely accepted two-diode model for solar cells with Schottky back-contacts.

- The impact of a thin CdS window on solar cell performance was found to agree with a non-uniformity model based on regions of high- and low-V_{oc} when the area distribution was taken to be dependant on CdS thickness. The area division was not quantitatively consistent in all cases with photocurrent variations observed in LBIC data, though this could be explained by the limited resolution of the measurement. It was proposed that the

critical thickness for separation of CdTe and SnO_2 layers is determined by the CdS grain size and the SnO_2 surface roughness.

A key feature of this work, and indeed the goal of projects aimed at improving the overall conversion efficiency of photovoltaics, was to draw connections between the mechanisms limiting the device performance and the specific conditions of the fabrication technique used. This enables the identification of possible changes one could make to the fabrication process to improve the device performance, at least relative to the limiting mechanism of a given study. Several strategies were suggested, which could be implemented into a compact, high-throughput process to mitigate the effects of non-uniformities originating at the solar cell contacts. These suggestions form a natural set of ideas for future studies.

Future work

Here is a brief summary of the suggestions from chapters four and six, for possible deviations from the baseline CSU process: (1) Deposit a somewhat thicker layer of CdTe, so that full-depletion no longer occurs, and any non-uniform effects from the back-contact are separated from the collection at the main junction. (2) Include a thin alloyed (CdZn)Te layer at the back surface to reduce the Schottky barrier and insert an electron reflector, which modeling showed should improve device V_{oc}. (3) Explore ways to minimize the surface roughness of the SnO_2 layer before deposition of a thin CdS layer. This could be achieved by chemical etching, or perhaps using gas cluster ion beam sputtering. (4) Encourage the growth of smaller than standard CdS grains by adjusting the process parameters for a higher starting temperature, or perhaps by more individualized control of the chamber ambient at the various deposition stations. (5) Investigate the introduction of a bi-layer TCO, either directly from the manufacturer, or by adding an additional module to the fabrication process to deposit a thin intrinsic layer.

Certainly not all of these measures should be addressed simultaneously. It was found in simulations in chapter three that the electron reflector is most effective when it forms part of an MIS structure, so full depletion of the CdTe would be necessary in that case. Furthermore, suggestions 3-5 above are merely different approaches to solving the same problem, namely effective separation of the SnO_2 and CdTe layers when CdS is thin. Any one of

them may be sufficient to enable CdS layers in the range of 30 nm that yield CdS/CdTe solar cells with higher V_{oc} and FF.

At the time of this writing initial work on thicker CdTe layers is recently underway with promising results. Capacitance results appear to verify a depletion region approximately 2.5 μm in thickness. Without re-optimizing other processes or conditions to the increased CdTe thickness, efficiencies are already better than 11 %, with slight reductions in V_{oc} and FF somewhat compensated by increased current (compared to the base process). Initial interpretation of these results explains the losses in voltage and fill factor as coming from a small volume of high defect density, since the $CdCl_2$ treatment was not adjusted to account for the greater CdTe volume. The increased current appears from QE to be attributable to improved long-wavelength collection, since the generation and electric field volumes are both increased.

Extroit

This work identified several sources of performance loss in CdS/CdTe solar cells, which may be addressed in the fabrication of the contact layers. It is my hope, that the efforts described here will be of use in the pursuit of large-scale, low-cost deployment of photovoltaic energy generation, for the good of many.

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