THESIS

BUCK CONVERTER FOR ON-CHIP REFERENCE GENERATION

Submitted By

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In partial fulfillment of the requirement

For the Degree of Masters of Science

Colorado State University

Fort Collins, Colorado

Summer 2010

COLORADO STATE UNIVERSITY

JULY 8TH, 2010.

WE HEREBY RECOMMEND THAT THE THESIS PREPARED UNDER OUR SUPERVISION BY ABHAY KUMAR RAI ENTITLED BUCK CONVERTER FOR ON-CHIP REFERENCE GENERATION BE ACCEPTED AS FULFILLING IN PART REQUIREMENTS FOR THE DEGREE OF MASTERS OF SCIENCE.

Committee on Graduate Work

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ABSTRACT OF THESIS

BUCK CONVERTER FOR ON-CHIP REFERENCE GENERATION

Most modern day chips use an on chip voltage reference, also known as a bandgap voltage reference generator, to provide a stable reference, independent of power supply voltage (V_{DD}) ripples and compensated for temperature variations. When power supply voltage decreases as the process feature size (gate length) decreases, it imposes challenges in terms of headroom and other factors to achieve a stable bandgap voltage reference. It also needs to be scaled down to $V_{DD}/2$ for practical uses and provide a common mode voltage of $V_{DD}/2$ for on-chip circuits. This thesis discusses a buck converter which uses an alternative to pulse width modulation (PWM) for stable reference generation and directly generates a $V_{DD}/2$ reference using a novel inductor ripple current cancellation technique, which cancels inductor ripple current and therefore does not require a large capacitance for filtering of inductor ripple. An alternative to the pulse width modulation (PWM) technique is proposed, which uses common mode bias and transconductance (g_m) tuning to keep the reference output constant for variable loads, and a temperature compensation technique is used to minimize temperature sensitivity.

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ACKNOWLEDGEMENTS

It has been a real privilege to be a graduate student in the ECE department at Colorado State University, Fort Collins. My experience here has been full of opportunities to learn from faculty and students with wide and deep expertise in engineering.

I would like to thank my advisor, Prof George Collins, for his invaluable guidance throughout my journey as a graduate student in the department. His many years of experience with switching regulators and power electronics have allowed him to focus on the critical and interesting issues of any problem. It has been a unique privilege to be in his group.

I would like to thank the members of my thesis committee for their valuable feedback. I would like to thank Prof Steven Reising for helping me on numerous occasions. I got greatly benefited from his MathCAD program for on-chip inductor design and was able to successfully implement the shunt peaking technique taught in ECE536. His detailed analysis of noise in MOSFETs helped me in day-to-day design activities and while working on output transconductance amplifier (OTA) design for 5^{th} order elliptic filter [22] design project for my Stanford University Signal conditioning class this spring. I would like to thank Prof Azer Yalin for kindly agreeing to be in my committee and taking time to read this thesis.

I would like to thank Prof Kevin Lear for making himself available to me cheerfully whenever I needed his advice on wide variety of device physics related issues.

I would like to thank my parents Chameli and Hira Rai for being a never ending source of inspiration and a sole reason for who I am today.

I would like to thank my wife Arpana Rai for being most patient person in my life and being a source of encouragement, without whose wholehearted support, this goal would have been nearly impossible. I would also like to thank my toddler daughter Kashvi Rai for filling me with energy and teaching me that life is a never-ending learning experience.

Last but not the least I would like to thank my employer Avago Technologies, Inc. for sponsoring my graduate studies and being patient throughout the duration of my graduate studies.

CHAPTER 1 INTRODUCTION

DC-DC Converter

The DC-DC Converter is a circuit employing a switching network that converts one DC voltage to another (Fig 1.1). DC-DC converters are mainly used to provide a DC power supply with adjustable output voltage, for general use.

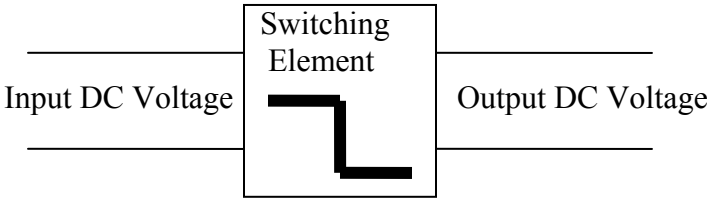


Figure 1.1 DC-DC Converter

There are two ways to achieve the voltage regulation:

1. Pulse Width Modulation (PWM): This is achieved by varying the on period (T_{on}) of the switch while keeping the switching period T constant, as shown in Fig 1.2. Here Duty cycle (D) refers to the ratio of the length of time for which the switch is kept ON to the cycle period. Usually control by pulse width modulation is the preferred method since constant frequency operation leads to optimization of an LC filter and to limit the ripple content in the output voltage.
2. Pulse Frequency Modulation (PFM): Here the on duration (T_{on}) is kept constant and the switching period T is varied as shown in Fig 1.3. The design of the LC filter is difficult in this case.

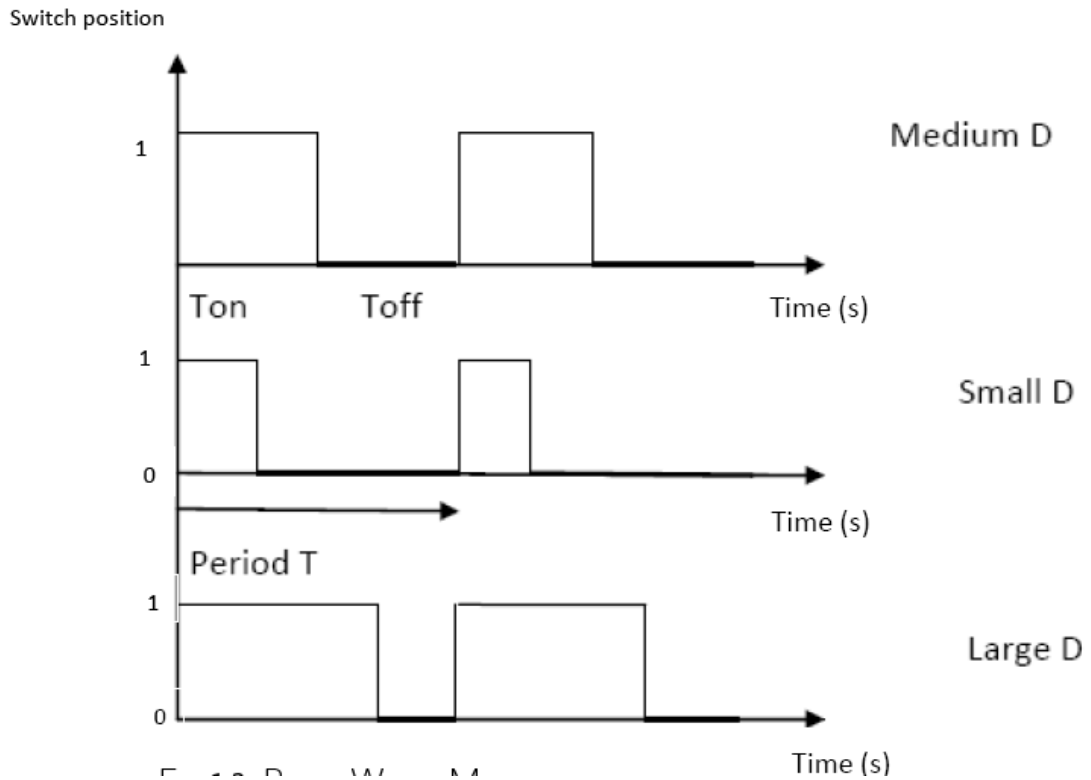


Figure 1.2 Pulse Width Modulation (PWM)

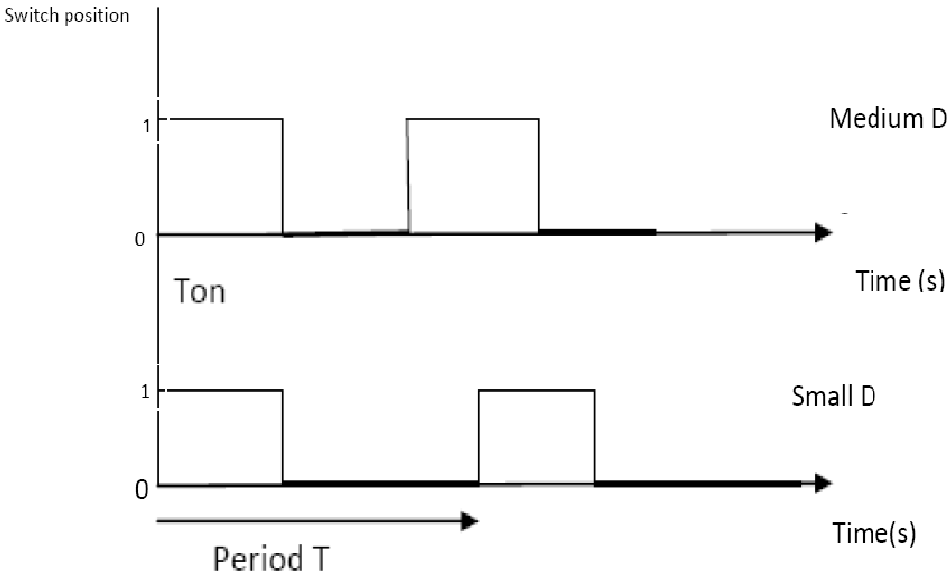


Fig 1.3 Pulse Frequency modulation

There are three basic types of DC-DC converters:

1. Step-down converter (buck converter)
2. Step-up converter (Boost Converter) and
3. Step-up-down converter (buck-boost converter)

Buck Converter

A buck converter or step-down switch mode power supply can also be called a switch mode regulator. The popularity of switch mode regulators is due to their fairly high efficiency and compact size. Switch mode regulators are used in place of linear voltage regulators at relatively high output, because linear voltage regulators are inefficient [1]. Since the power devices used in linear regulators have to dissipate a fairly large amount of power, they have to be adequately cooled, typically by mounting them on heat sinks, which makes the regulator bulky and large. In applications where size and efficiency are critical, linear voltage regulators cannot be used [2]. In general, any basic switched power supply consists of five standard components, as shown in Fig 1.4.

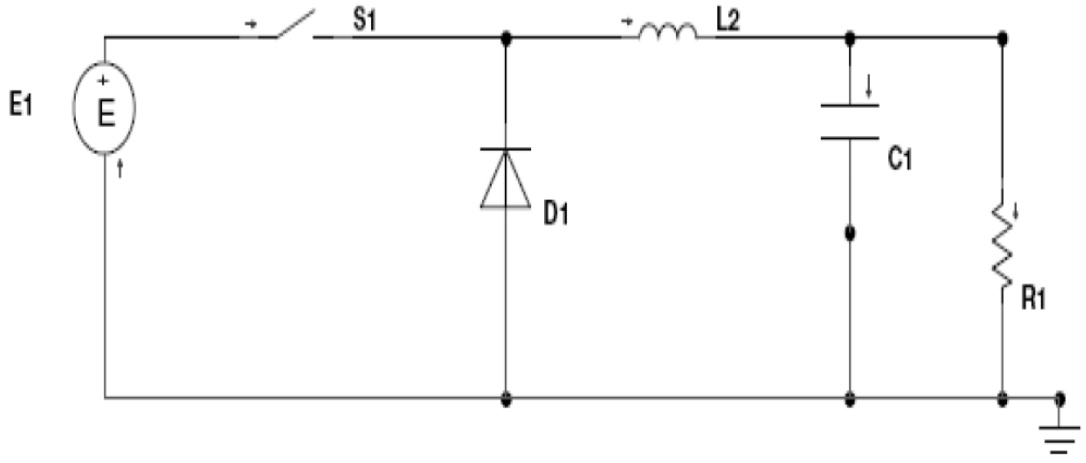


Fig 1.4 Buck Converter

I. A pulse-width modulating controller
II. A transistor switch
III. An inductor
IV. A capacitor and
V. A diode or a non overlapping switch.

Control by pulse-width modulation is necessary for regulating the output since duty cycle can be adjusted to obtain the desired voltage output. The switch is the heart of the switched supply and it controls the power supplied to the load [3]. An inductor is used in a filter to reduce the ripple current. This reduction occurs because inductors oppose change in current. When the current through an inductor decreases, the inductor tends to maintain the current by acting as a source.

A capacitor is used in a filter to reduce ripple voltage. The diode used in a switched regulator is usually referred to as a catch diode [1]. The purpose of this diode is not to rectify, but instead to direct current flow in the circuit and to ensure that there is always a path for the current to flow into the inductor. This diode can be replaced with a non overlapping MOSFET switch in order to eliminate the diode drop.

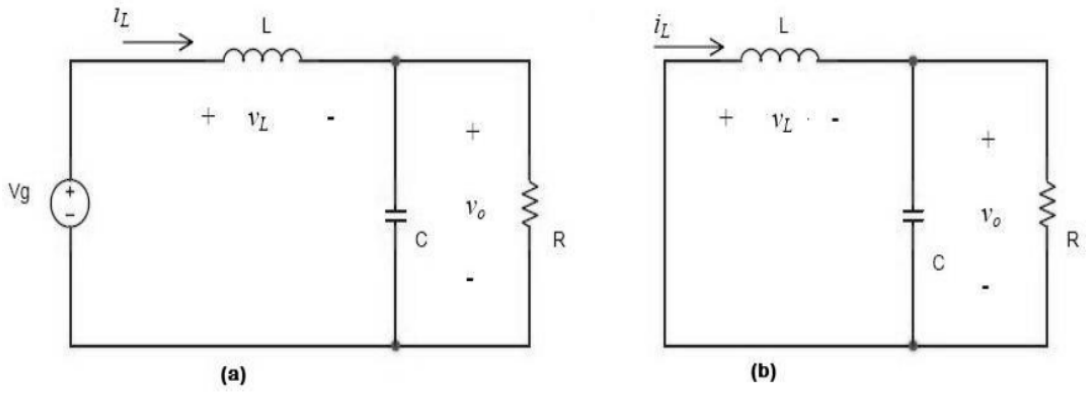


Fig 1.5a Buck converter of Fig 1.4 with Switch closed

Fig 1.5b Buck converter of Fig 1.4 with Switch open

Fig 1.6 shows the current and voltage waveforms through the inductor when switch is open and closed.

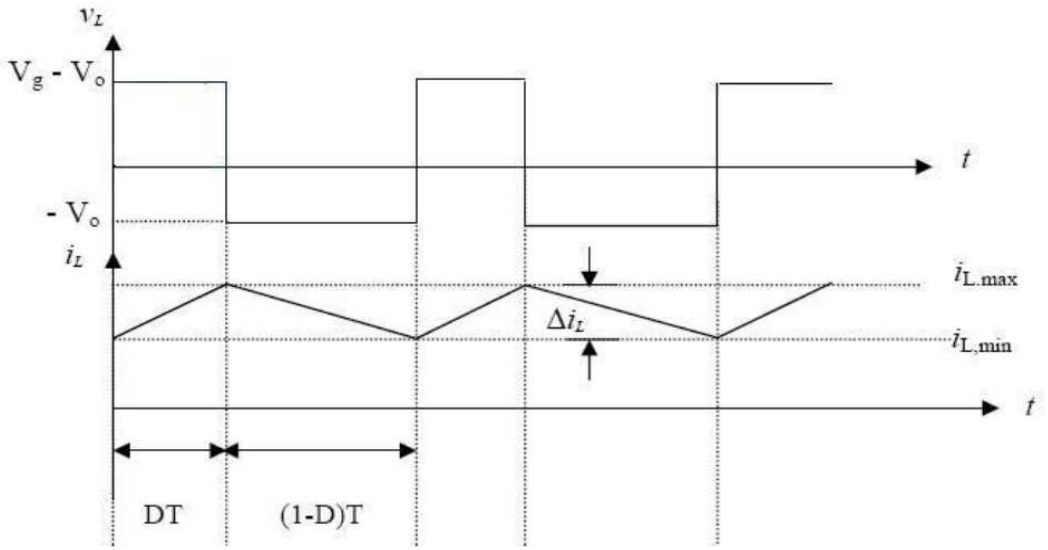


Fig 1.6 Inductor Voltage and Inductor Current Waveforms

This circuit can operate in either of the two states as explained below.

Switch Closed: In the circuit, when the switch is closed, the switch conducts the inductor current (I_L) as shown in Fig 1.5a. This results in a positive voltage across the inductor since the source voltage is greater than the output voltage. This voltage causes a linear increase in the inductor current. When the inductor current rises, the energy stored in it increases. During the state when the switch is closed, the inductor acquires energy [4].

$$V_{LON} = V_{in} - V_0 \quad (1.1)$$

$$T_{ON} = DT \quad (1.2)$$

The capacitor smooths the inductor's current changes into a constant output voltage. Also, the capacitor is large enough so that the output voltage does not change significantly during one switching cycle. In this state the capacitor is charging. When the switch is closed, the elements carrying current are shown in Fig. 1.5a. Since the diode is reversed biased, it is not shown in the picture.

Switch Open: When the switch is open, the inductor maintains current to the load as shown in Fig 1.5b. As the inductor's magnetic field decreases, the current through the inductor decreases linearly, as determined by the voltage across the inductor and its inductance.

$$V_{LOFF} = -V_0 \quad (1.3)$$

$$T_{OFF} = (1-D)T \quad (1.4)$$

Since the average voltage across the inductor is zero in steady state, using the volt-second balance equation

$$V_{LON} \cdot T_{ON} + V_{LOFF} \cdot T_{OFF} = 0 \quad (1.5)$$

$$[V_g - V_0] DT + (-V_0)(1-D) T = 0$$

$$V_g D - V_0 D - V_0 + V_0 D = 0$$

V_0 = D Vg (assuming ideal components) (1.6)

The inductor maintains current flow by reversing its voltage when the applied voltage is removed. The diode acts as a voltage controlled switch. It provides a path for the inductor current. When the switch is open, the inductor current flows through the diode [5].

Modes of Operation

DC-DC converters have two distinct modes of operation: Continuous-current conduction mode (CCM) and discontinuous current- conduction mode (DCM). The buck converter and its control are designed based on both modes of operation.

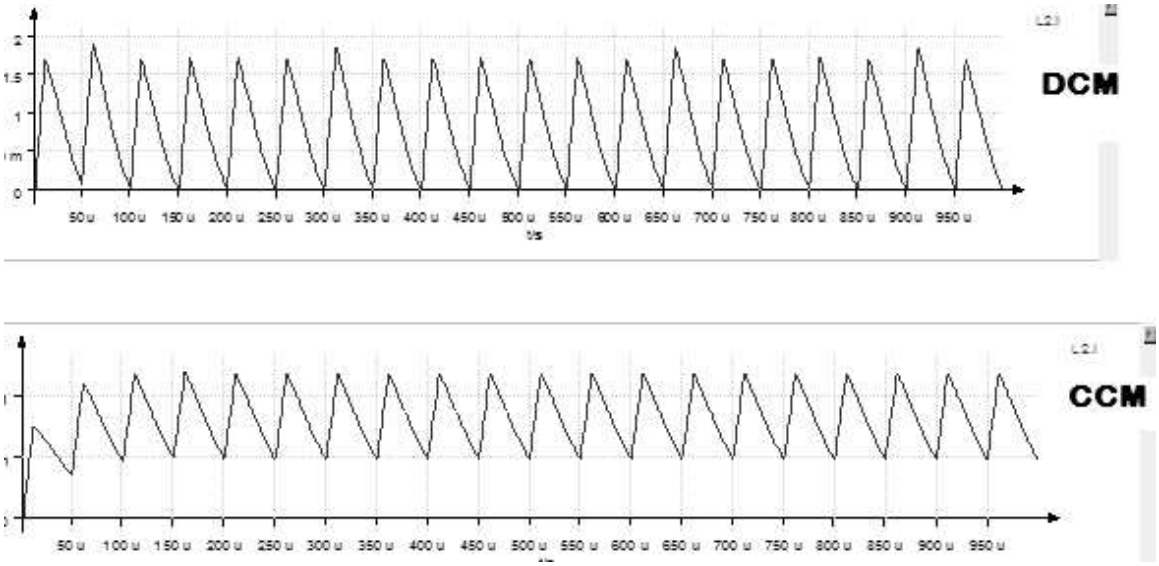


Fig 1.7 DCM and CCM mode of operation

In the continuous conduction mode, the inductor current flows continuously. That is, inductor current is always greater then zero during the OFF period, as shown in Fig 1.7b. Here the voltage output varies linearly with the duty cycle of the switch for a given dc voltage input. It does not depend on other circuit parameters (e.g. inductor and capacitor value) [6].

$V_0/V_g = T_{on}/T$ =Duty Cycle.

Therefore in the continuous current conduction mode (CCM), the output voltage can be controlled by controlling the duty cycle over a range of 0-1.

In the Discontinuous conduction mode (DCM) [13], the inductor current is discontinuous It can be seen in Fig 1.7a that inductor current is in critical state for some time ($I_L = 0$) which causes the average inductor current to decrease to less than half of the inductor ripple current [1]. In the OFF period, the power to the load resistance is supplied by the capacitance alone. Thus in the Discontinuous Conduction mode, the output voltage is dependent on the circuit component values and the duty cycle of the switch [6].

CHAPTER 2 BUCK CONVERTER DESIGN

The voltage output is controlled by using a high frequency pulse-width-modulated control (PWM) signal to drive the switching element (transistor or switch). Typically the frequency of the pulse width modulated control signal is in the range of tens to hundreds of KHz. There are two benefits: First, as frequency increases, components become smaller, lighter and cheaper [1]. Another benefit is that the delay from input to output created by the switching time is lower.

Typically, it is recommended that the buck converter run in continuous mode (CCM) for expected loads due to following reasons

1. The gain is stable. In continuous mode, the output Voltage (V_0) is approximately set by input voltage (V_g) and the duty cycle only, regardless of load or other component values. In discontinuous mode, V_0 depends on V_g, duty cycle, inductor value, load and frequency.
2. For continuous and discontinuous modes, the frequency responses are different. The transient response in continuous mode can be different than in discontinuous mode.
3. Continuous mode operation tends to produce smaller ripple in output Voltage Vo and interference [4].

Selection of Component Values

During component selection, each component's value is selected based on certain circuit parameters.

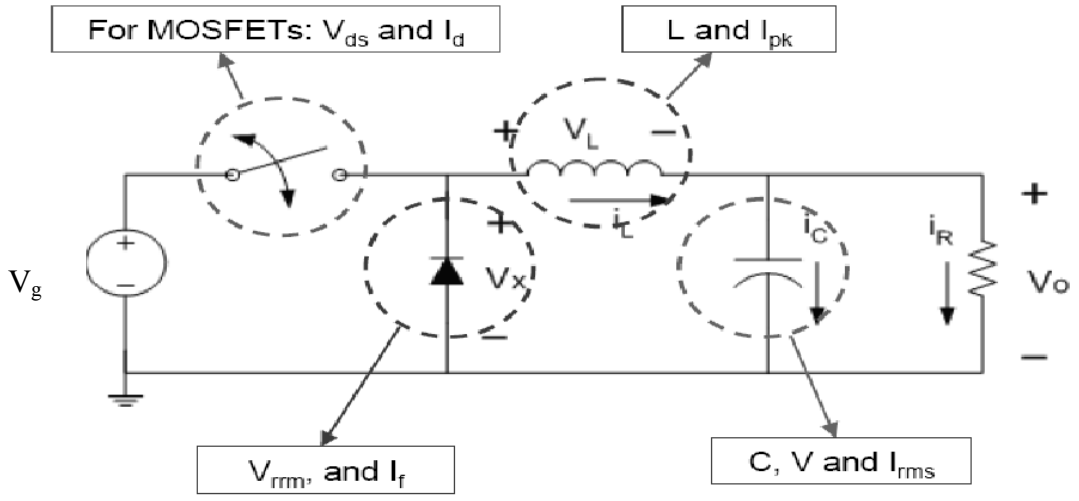


Fig 2.1 Buck converter with factors to be considered in component selection

Inductor

Since the value of the inductor determines the operating mode of the buck converter [13], inductor design plays an important role in buck converter design. The inductor functions by removing energy from the electrical circuit, storing it in a magnetic field and subsequently returning the energy to the circuit [7].

When the inductor is discharging [4]:

$V_L = -V_0 = L\, di_L/dt$ (2.1)

$di_L/dt = -V_0/L$ (2.2)

$\Delta i_{Loff} = -V_0/L * [\Delta_{toff}]$

$\Delta i_{Loff} = -V_0/L * [1-D]T$ (2.3)

When inductor is charging:

$V_L = V_g - V_0 = L\, di_L/dt$

$di_L/dt = [V_g - V_0]/L$

$\Delta i_{Lon} = (V_g - V_0/L)* [\Delta t_{on}]$

$\Delta i_{Lon} = [V_g - V_0/L]* DT$ (2.4)

Fig 2.2 shows the current through and voltage across the inductor.

$I_{LMIN} = I_L - |\Delta i_L|/2 = V_0/R - (1-D)V_0/ 2LF = Vo [1/R - (1-D)/ 2LF]$ (2.5)

$I_{LMAX} = I_L + |\Delta i_L|/2 = V_0/R + (1-D)V_0/ 2LF = V_0 [1/R + (1-D)/ 2LF]$ (2.6)

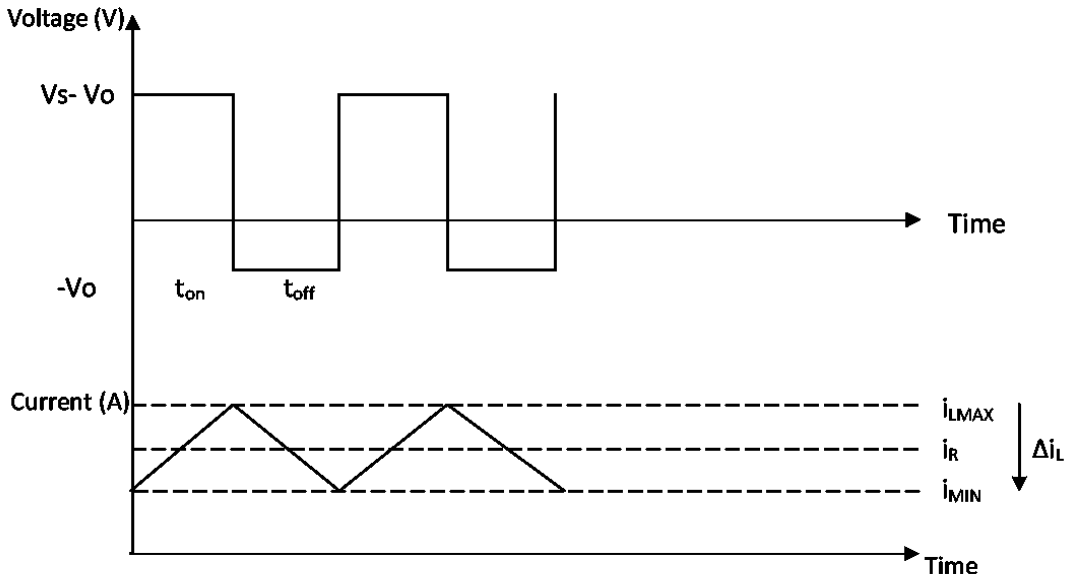


Fig 2.2 Inductor Voltage and current

Critical Inductance (L_C)

The critical Inductance is the minimum inductance at which the inductor current reaches boundary conduction mode. Any inductance value lower than the critical inductance causes the buck converter to operate in the discontinuous conduction mode. The inductance value is critical to maintaining current to the load while the switch is off. It is necessary to determine the minimum inductance necessary to support the required output

current of the Buck converter so that the load is supported under worst-case conditions of output voltage and input current [4].

In order to determine the critical inductance, the maximum inductor current ripple Δi_L or minimum percentage load requirement is specified.

$L_{MIN} = 0 = I_L - [|\Delta i_L|/2] = V_0 [1/R - (1-D)/ 2LF]$

$LC = (1-D_{MAX})R_{MAX} / 2F$ (2.7)

$R_{MAX} = V_0/I_{MIN}$ (2.8)

D_{MAX} = duty cycle calculated at minimum input voltage

F= Frequency

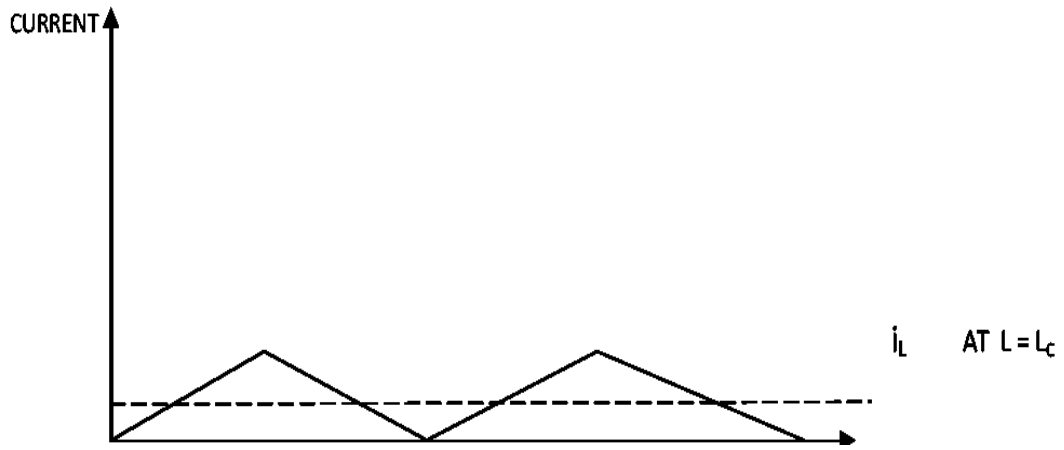


Fig 2.3 I_L and L_C

Peak current through the inductor determines the inductor's required saturation-current rating, which in turn dictates the approximate physical size of the inductor. Saturating the inductor core decreases the converter efficiency, while increasing the temperatures of the inductor, the MOSFET and the diode [4]. The peak current rating of the inductor is

determined with the maximum inductor current. The worst case minimum inductor current occurs at maximum load.

Switch Rating

Transistors designated for use in switching power supplies must have fast switching times and should be able to withstand the voltage spikes produced by the inductor. Voltage rating: For an ideal switch, the maximum switch voltage (V_{switch_max}) is the maximum voltage input [4]. But for a non ideal switch, $V_{switch\_max} = V_{inmax} + V_F$ where V_F is the maximum forward drop across the switch (or forward diode drop) at maximum load current.

Switch current rating is calculated based on the average value of switch current. During T_{on}, the inductor current is equal to switch current. During T_{off} switch current is equal to zero.

$$I_{switch} = (i_{Lmin} + i_{Lmax}) * T_{on} / 2T \quad (2.8)$$

$$I_{switch} = [(i_{Lmax} - \Delta i_L) + i_{Lmax}] * DT / 2T = [2i_{Lmax} - \Delta i_L] * D / 2$$

$$I_{switch} = [i_{Lmax} - \Delta i_L /2] * D = i_L * D$$

$$I_{switch} > i_L * D_{max} \quad (2.9)$$

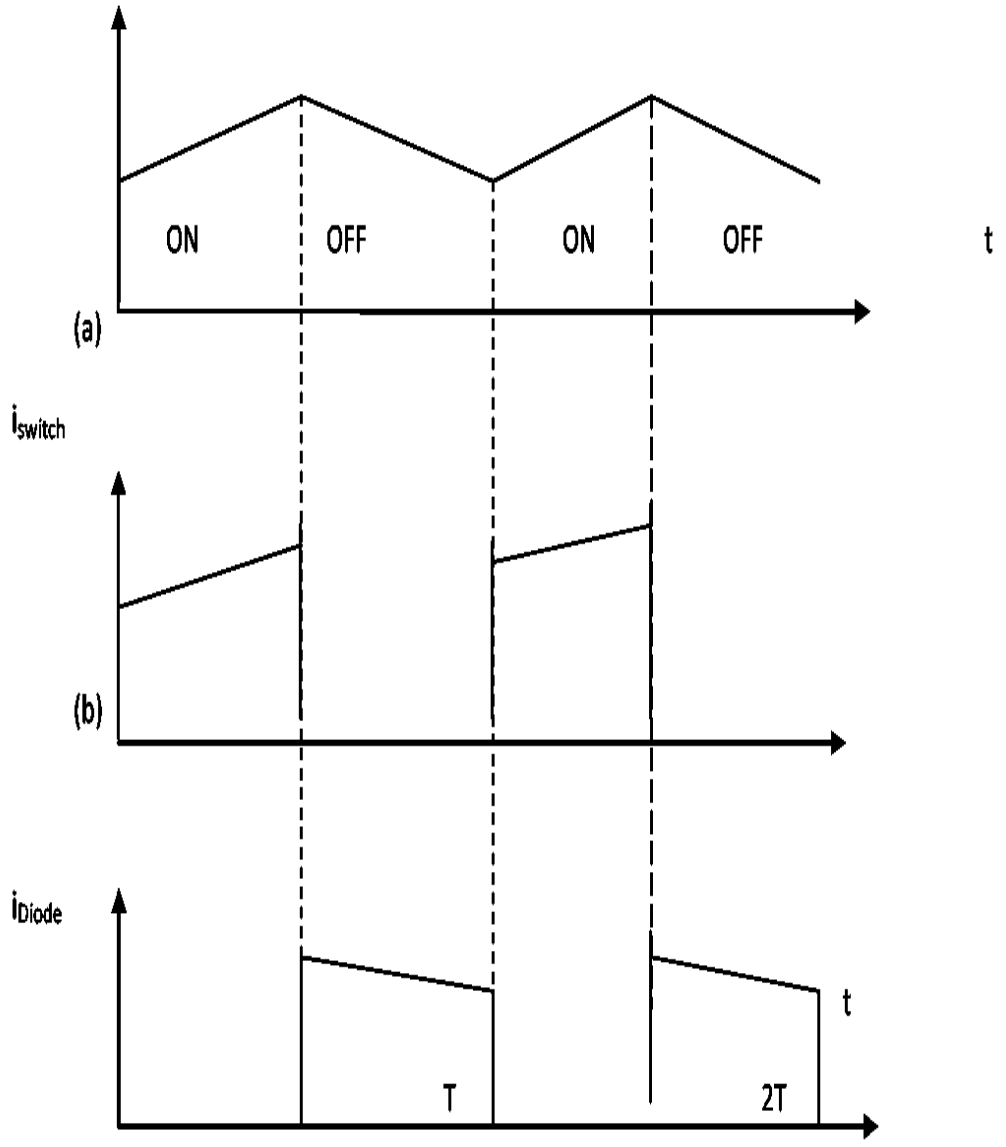


Fig 2.4 Current waveform (a) I_L (b) I_{SWITCH} (C) I_{DIODE}

Diode Rating

It is necessary that the diode should be able to turn off relatively fast. Diodes known as fast recovery diodes are used in these applications. The diode's average current I_D is equal to the load current times the portion of the time the diode is conducting T_{off} as

shown in Fig 2.5. The diode's forward-current specification must meet or exceed the maximum output current [4].

$I_{diode} = (i_{Lmin} + i_{Lmax}) * t_{off} / 2T$ (2.10)

$I_{diode} = [(i_{Lmax} - \Delta i_L) + i_{Lmax}] * (1-D)T / 2T = [2i_{Lmax} - \Delta i_L] * (1-D) / 2$

$I_{diode} = [i_{Lmax} - \Delta i_L /2] * (1-D) = i_L * (1-D)$

$I_{diode} > i_L * (1-Dmin)$ (2.11)

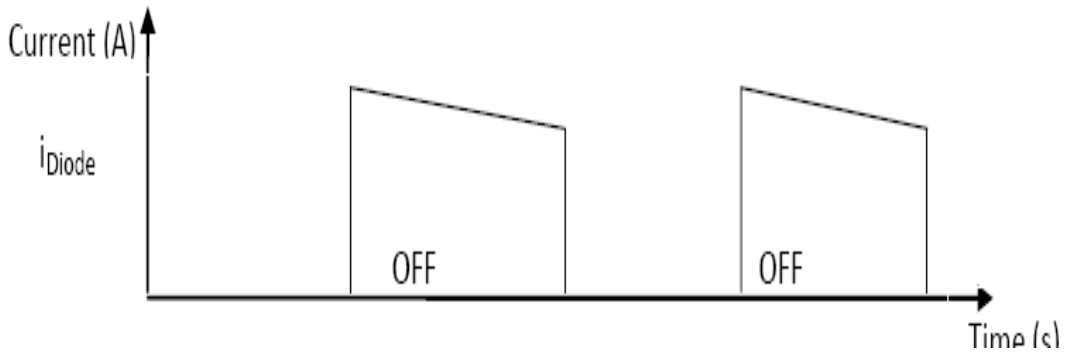


Fig 2.5 Diode current waveform

The maximum reverse voltage across the diode is the maximum input voltage. The current voltage ratings are low enough so that a small Schottky diode or a fast recovery diode could be used for this application.

Power dissipation is the limiting factor when choosing a diode. The worst-case average power can be calculated as follows:

$P_{diode} = (1- D_{min}) * i_L * V_D$ (2.12)

where V_D is the voltage drop across the diode at the given output current I_{OMAX}.

Selection of Output Capacitor Value

The capacitor voltage should withstand the maximum output voltage. Ideally

$$V_{cmax} = V_0 + \Delta V_0/2 \quad (2.13)$$

Where ΔV_0 = ripple voltage

V_0 = output voltage

The output capacitance is chosen to minimize the voltage overshoot and ripple at the output of a buck converter. Since switched power regulators are usually used in high current, high-performance power supplies, the capacitor should be chosen for minimum loss. Loss in a capacitor occurs because of its internal series resistance and inductance. Capacitors for switched circuits are chosen on the basis of effective series resistance (ESR). For very high performance power supplies, sometimes it is necessary to put capacitors in parallel to get a low enough effective series resistance. The maximum allowed output-voltage overshoot and ripple are sometimes specified at the time of design. Thus, to meet the ripple specification for a buck converter circuit, an output capacitor with ample capacitance and low ESR is required.

The output voltage ripple could be reduced by

- Reducing the ESR by combining capacitors in parallel or using capacitors with lower ESR.
- The current ripple is reduced by increasing the circuit inductance or increasing the switching Frequency.

Current ripple in the inductor current flows through the capacitor leaving the average flowing through the load [8].

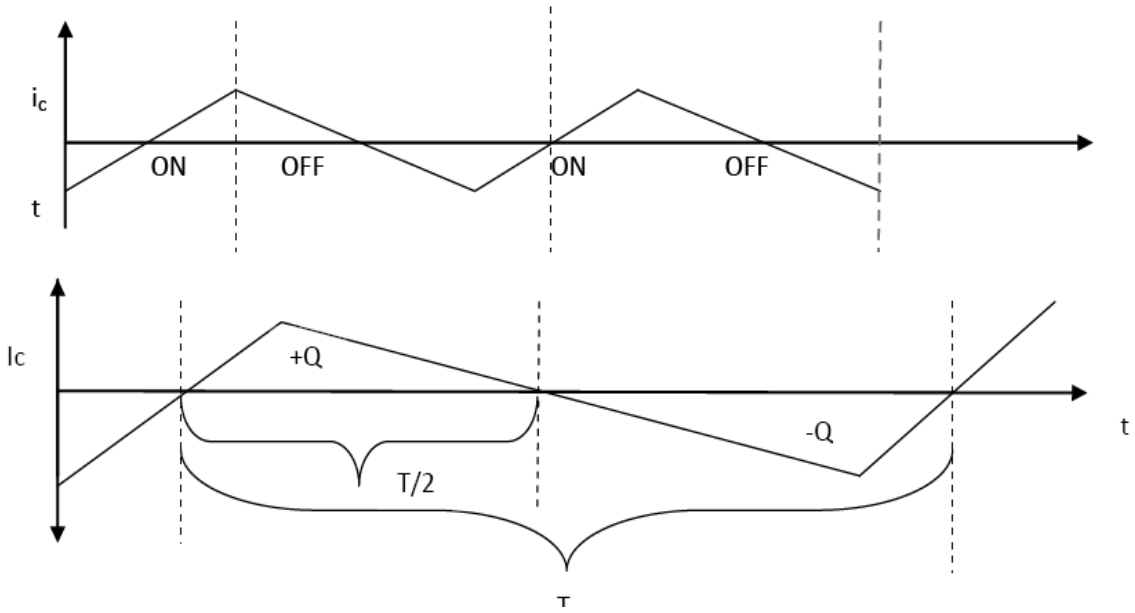


Fig 2.6 Capacitor current waveform

Minimum Output capacitance calculation [9]

$Q = ½ (T/2)(\Delta i_L/2) = \Delta i_L/8F = [(V_0/_L)(1\text{-}D)T] / 8F = (1\text{-}D)V_0/8LF^2$

$Q= C*\Delta V_0$

$C= Q/\Delta V_0 = [(1\text{-}D)\ V_0]/\Delta V_0\ 8LF^2 = (3.14)\ V_0/\Delta V_0 = \dfrac{1 - D_{min}}{(\Delta V/V_0)*8LF^2}$ (2.14)

$\Delta V/V_0 = (1\ \text{-}D_{min})/8LCF^2$ (2.15)

ΔV_0 = ripple Voltage

$\Delta V_0/V_0$ = percentage Ripple

MathCAD calculations for open loop Buck converter

Component values for open loop buck converter were calculated using MathCAD13 and simulated using Cadence Spectre IC5.1.41.

Maximum Input Voltage	$Vinmax := 2.0 \cdot V$	
Minimum Input Voltage	$Vinmin := 1.6 \cdot V$	
Out put Voltage	$V0 := 0.9 \cdot V$	
Switching Frequency	$f := 375 \cdot KHz$	
Max Load current	$Ilmax := 8mA$	
Minimum Load Current	$Ilmin := 3mA$	
Maximum Load Resistance	$Rlmax := \frac{V0}{Ilmin}$	$Rlmax = 300\Omega$
Minimum Load Resistance	$Rlmin := \frac{V0}{Ilmax}$	$Rlmin = 112.5\Omega$
Time Period	$T1 := \frac{1}{f}$	$T1 = 2.667 \times 10^{-6} s$
Minimum Duty Cycle	$Dmin := \frac{V0}{Vinmax}$	$Dmin = 0.45$
Maximum Duty Cycle	$Dmax := \frac{V0}{Vinmin}$	$Dmax = 0.563$
Minimum Required Inductance	$L1 := \frac{(1 - Dmax) \cdot Rlmax}{2 \cdot f}$	$L1 = 1.75 \times 10^{-4} H = \mathbf{L_C}$

To guarantee CCM, and account for switch resistance, ESR and diode drop, or switch resistance of another non overlapping switch, inductance value was chosen as 1mH, which is 5.7 times the critical inductance value.

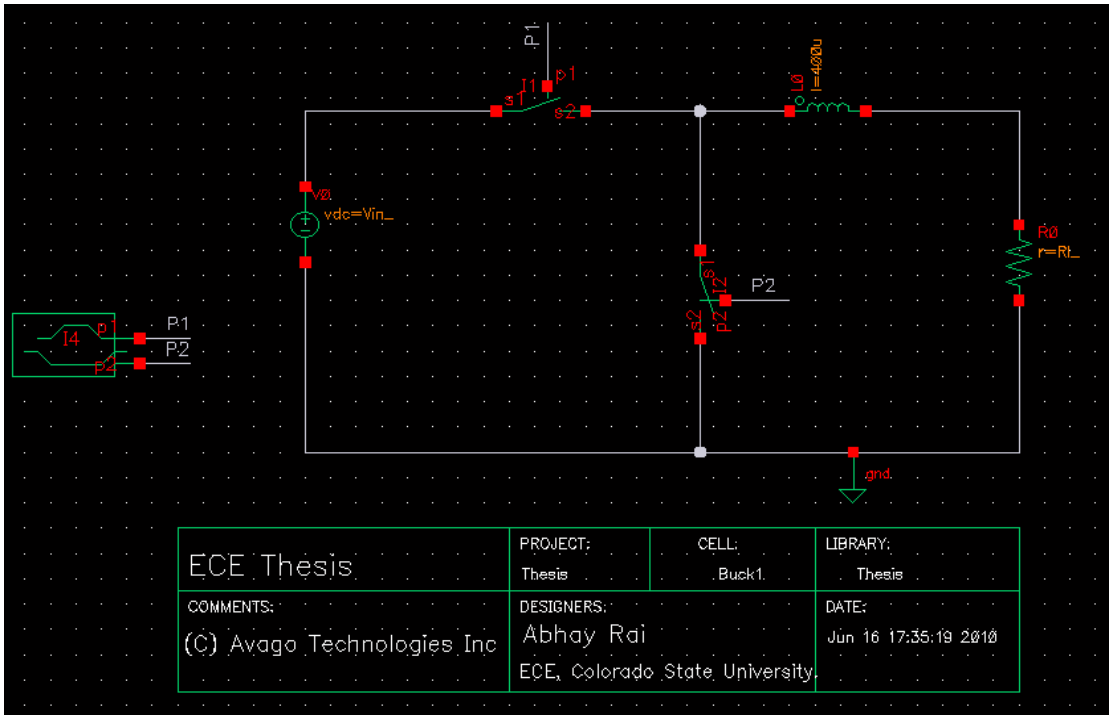


Fig 2.7 Buck Converter Schematic

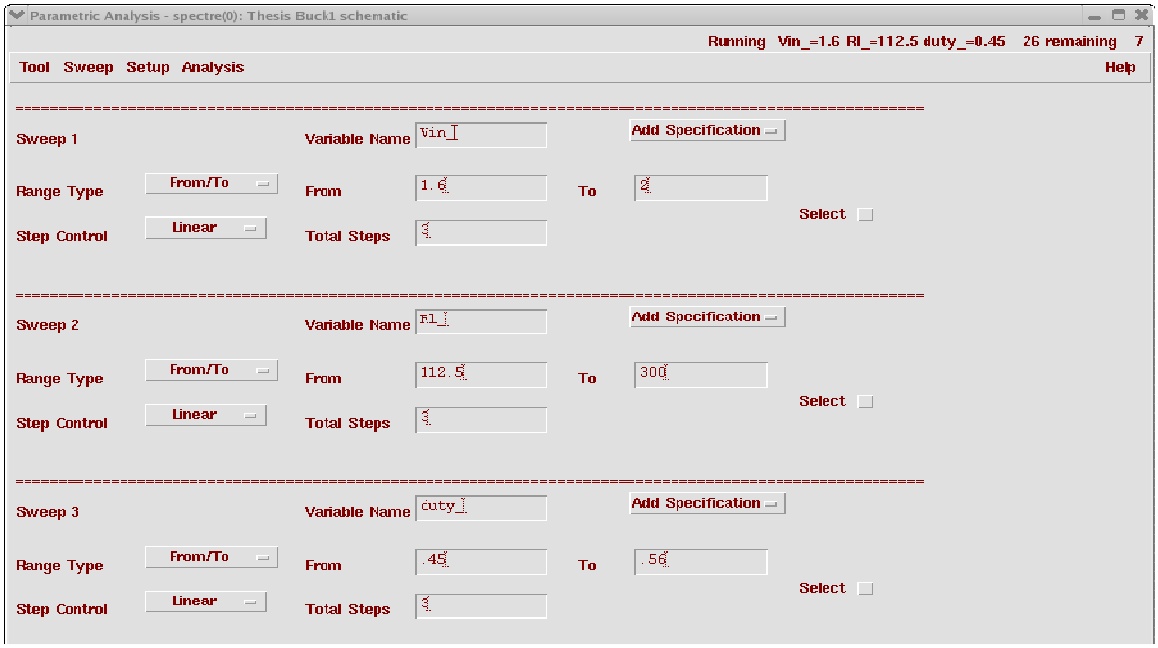


Fig 2.8 Parametric sweep setup

A transient simulation was set up and parametric sweep was performed using Vin, R_L and Duty cycle as variables, as shown in Fig 2.8. Fig 2.7 shows the basic open loop buck converter schematic without ripple current cancellation or filter capacitor. Sw1 and Sw2 use P1 and P2, non overlapping clocks generated by a non overlapping clock generator I1. Non overlap period can be programmed.

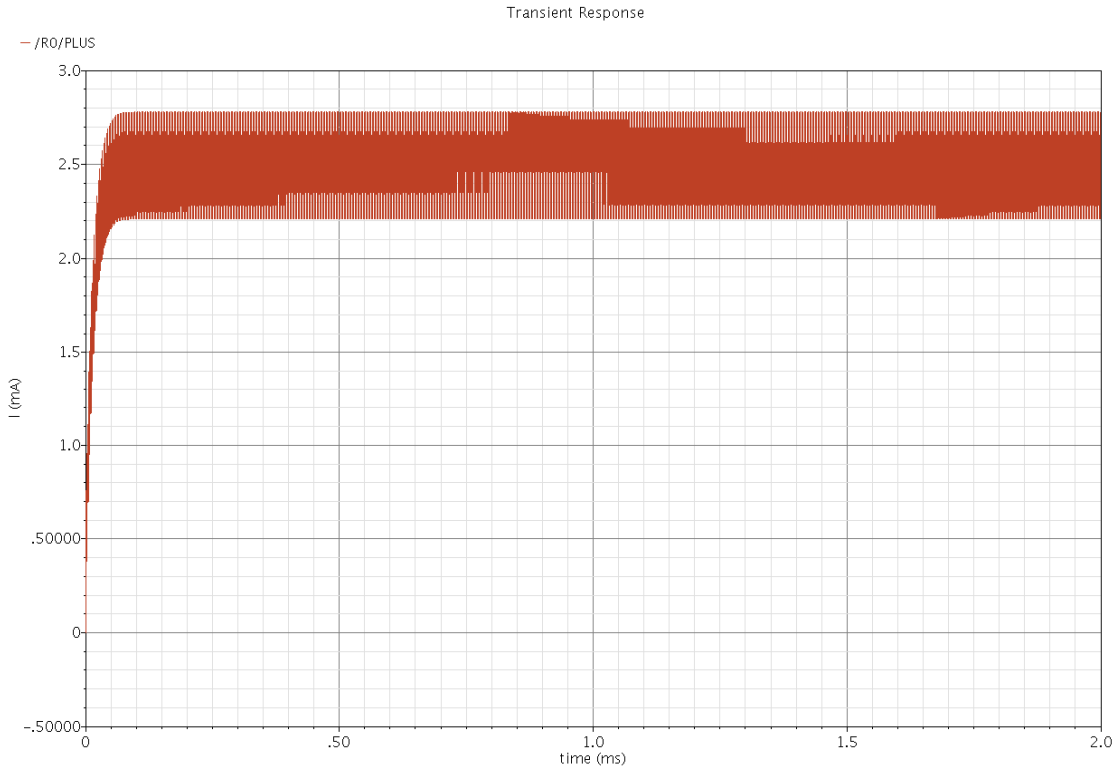


Fig 2.9 Inductor Current

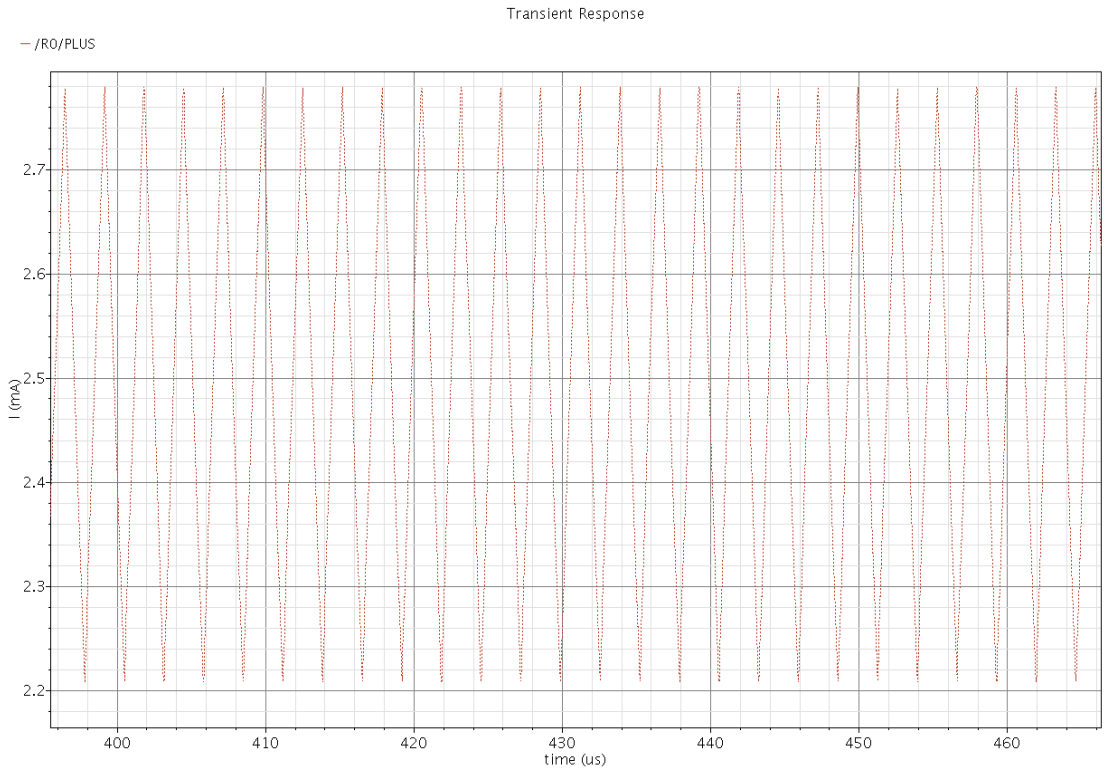


Fig 2.10 Ripple current

Fig 2.9 shows that the buck converter is operating in continuous conduction mode and Fig 2.10 shows the ripple current. Fig 2.11 shows ripple voltage without the use of ripple current cancellation technique or use of a filter capacitor. The maximum value of ripple voltage is 105 mV.

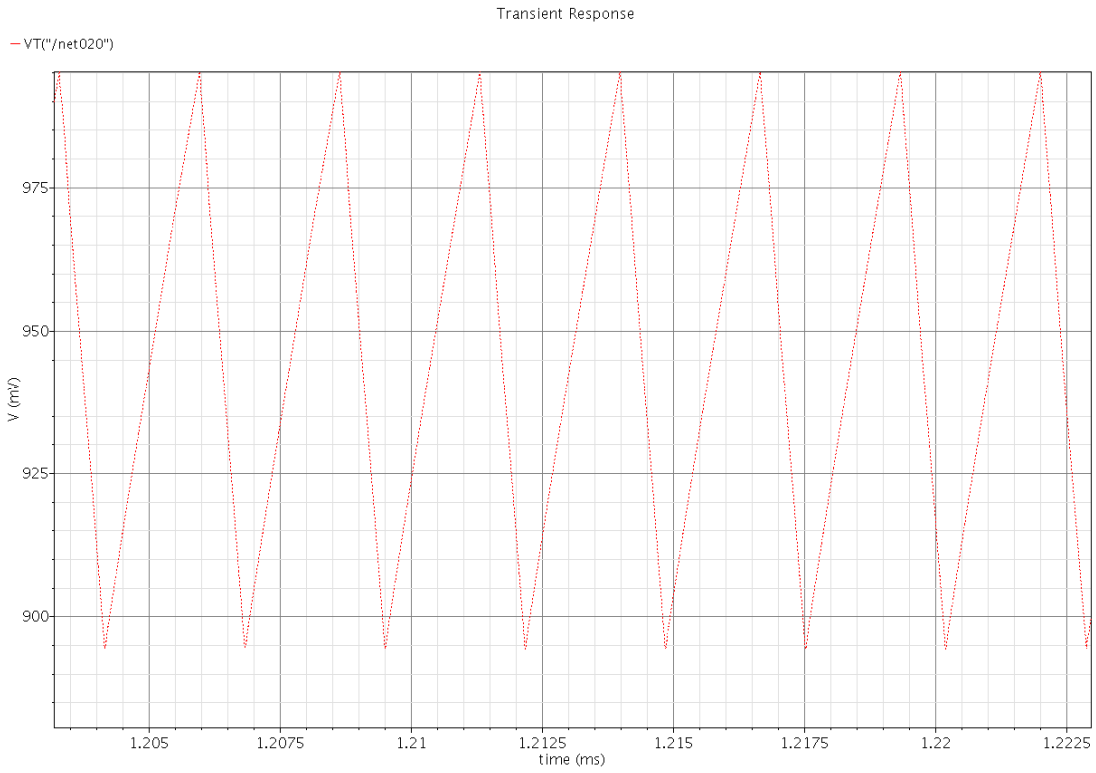


Fig 2.11 Ripple Voltage

Figs. 2.7 – 2.11 show that output ripple voltage and average output voltage depend on input voltage, duty cycle, inductor and capacitor values and their ESR. If this voltage is directly used as an on-chip reference, it will lead to a poor power supply rejection ratio (PSRR) performance and also it will result in an output referred offset in any differential circuit due to common mode variation which will be amplified by a subsequent stage and therefore it will become part of signal resulting in very poor performance.

For this output voltage to be used as an on-chip reference provider as an alternative to bandgap reference, one requires a circuit to eliminate ripple on output voltage and achieve insensitivities to component variations and V_g .

CHAPTER 3 BUCK CONVERTER COMPONENTS DESIGN FOR RIPPLE CURRENT REJECTION, TEMPERATURE COMPENSATION, AND INPUT VOLTAGE INDEPENDENCE

In a differential circuit requiring a common mode supplied by an on-chip reference, any common mode variation will lead to an output referred offset which becomes part of the signal and is amplified by subsequent stages. If this differential stage is part of an analog front end, it will result in severe performance degradation and the front end may become unsuitable for the application. This requires an on-chip reference to provide a constant voltage free of ripple.

In a conventional buck converter, output voltage variation is minimized by using the Pulse Width Modulation (PWM) or the Pulse Frequency Modulation (PFM) technique which minimizes output voltage variation due to change in load or V_g. This technique not only requires a costly PWM or phase locked loop (PLL), but these frequencies may get aliased into base band, degrading signal to noise ratio (SNR) performance of the overall system.

It may also need several frequencies to be generated on chip which may not be a desirable solution for a low power chip for mobile applications.

Conventional ripple rejection technique requires a capacitor which does an inverse action to inductor and therefore average current flows through the load.

However a capacitor may not be a viable solution for mobile applications due to cost and also it requires an extra pin.

A proposed solution described below uses a transconductance tuning mechanism along with a common mode feedback technique to achieve parameter independence.

Ripple rejection and V_{IN} Independence

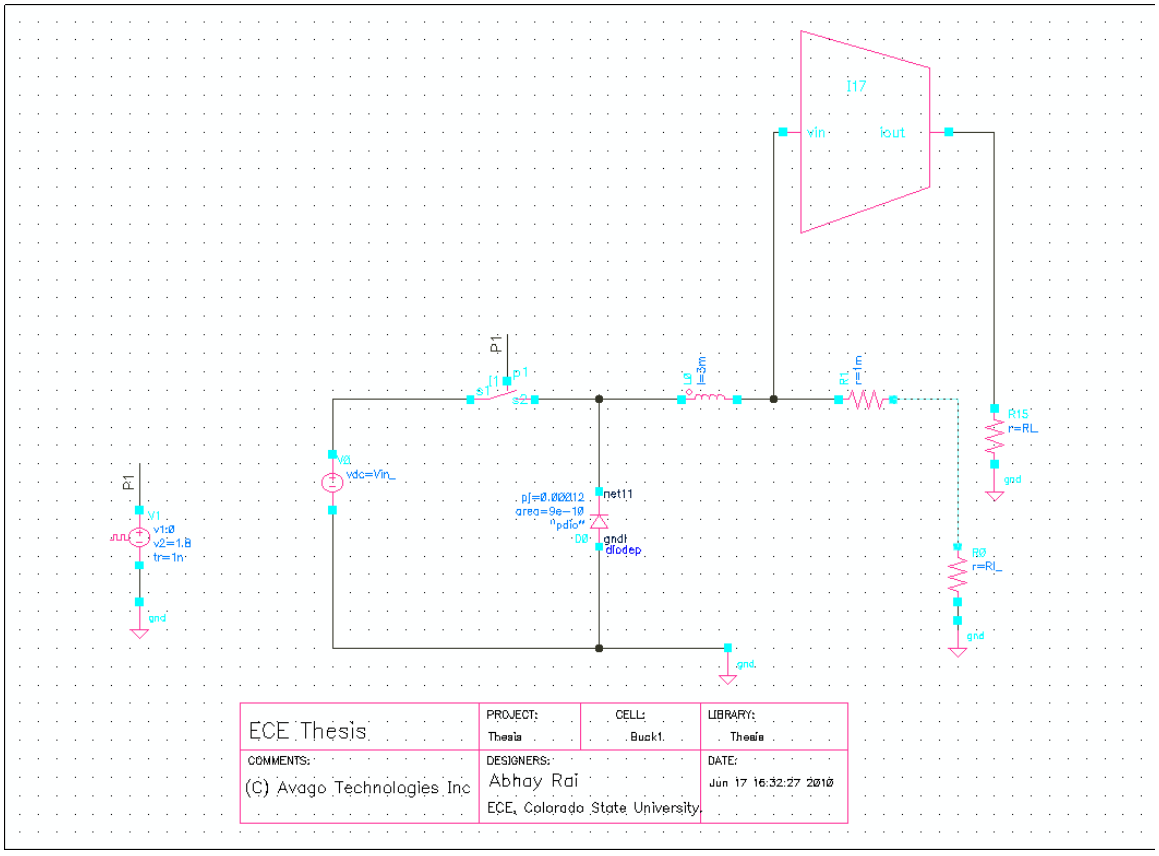


Fig 3.1 Basic ripple current cancellation scheme

Fig 3.1 shows an open loop buck converter with a basic ripple current cancellation scheme. I17 is an ideal Operational Transconductance Amplifier (OTA) which senses voltage and converts it to current with a transfer gain factor g_m.

Fig 3.2a shows current produced by inductor and Fig 3.2b shows OTA current. The two currents are out of phase.

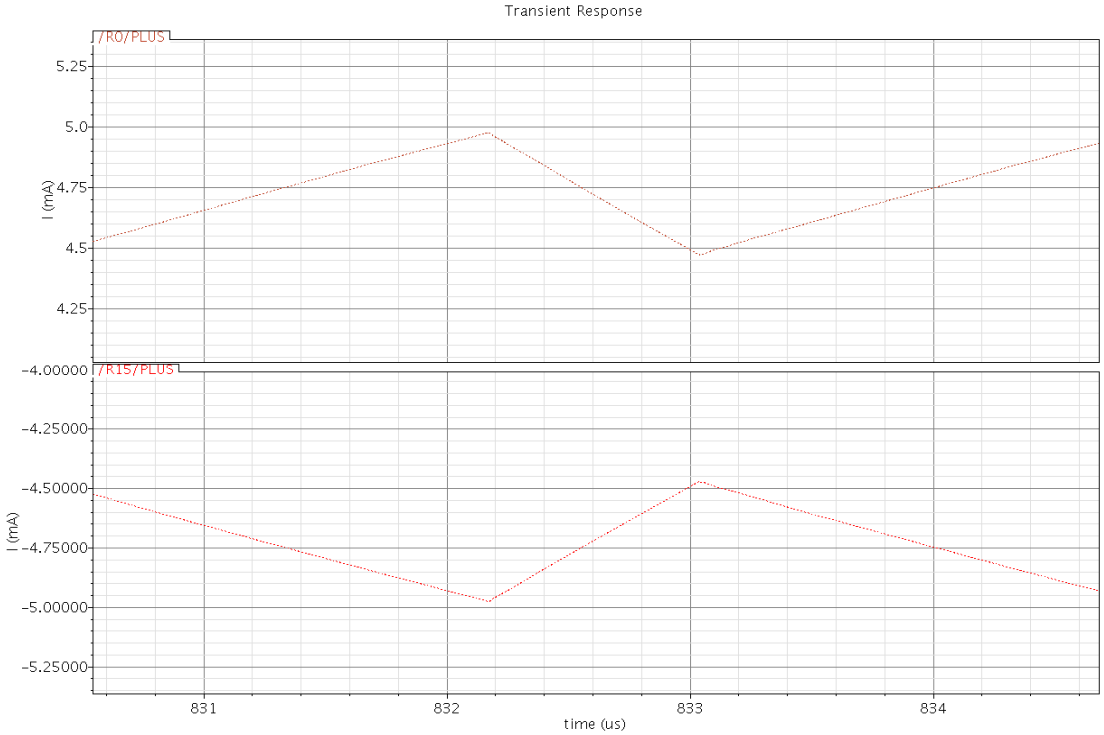


Fig3.2 (Fig 3.2a Inductor ripple current, Fig 3.2b OTA ripple current)

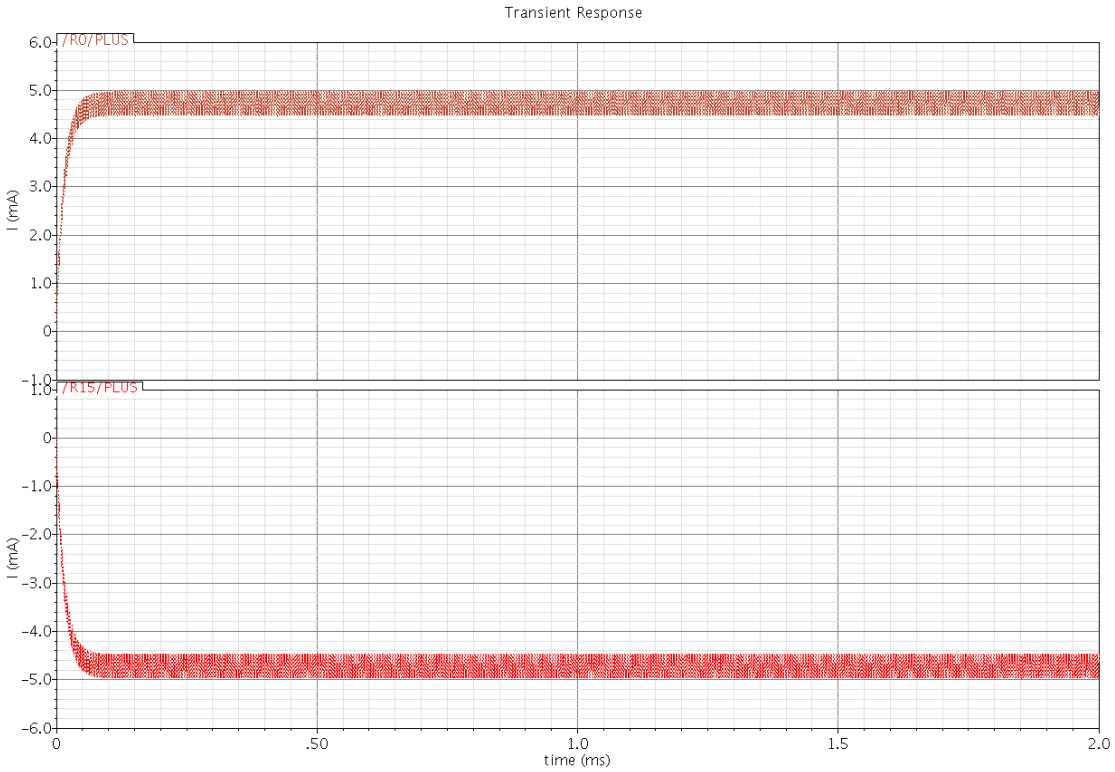


Fig 3.3 Fig 3.2 full view

A transconductance of 5 mS is required to generate a matching out of phase current from OTA, however, if these two currents are added, they will exactly cancel each other and therefore will result in zero load current.

To avoid this, OTA does not need to produce a DC + out of phase ripple current but, it only needs to produce a ripple current which is out of phase with inductor ripple current with a zero DC current. In order to for this objective to be achieved, OTA needs to be biased at a desired common mode voltage of 900 mV as shown in Fig 3.4.

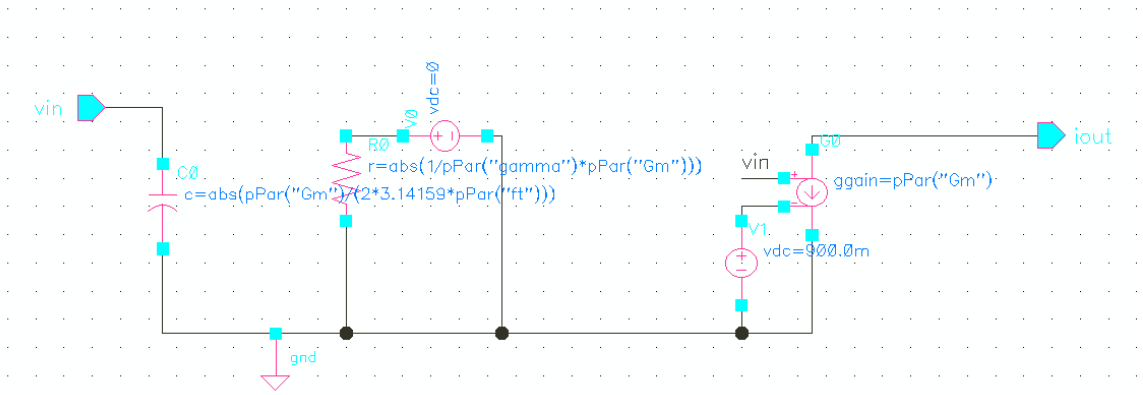


Fig 3.4 Ideal OTA

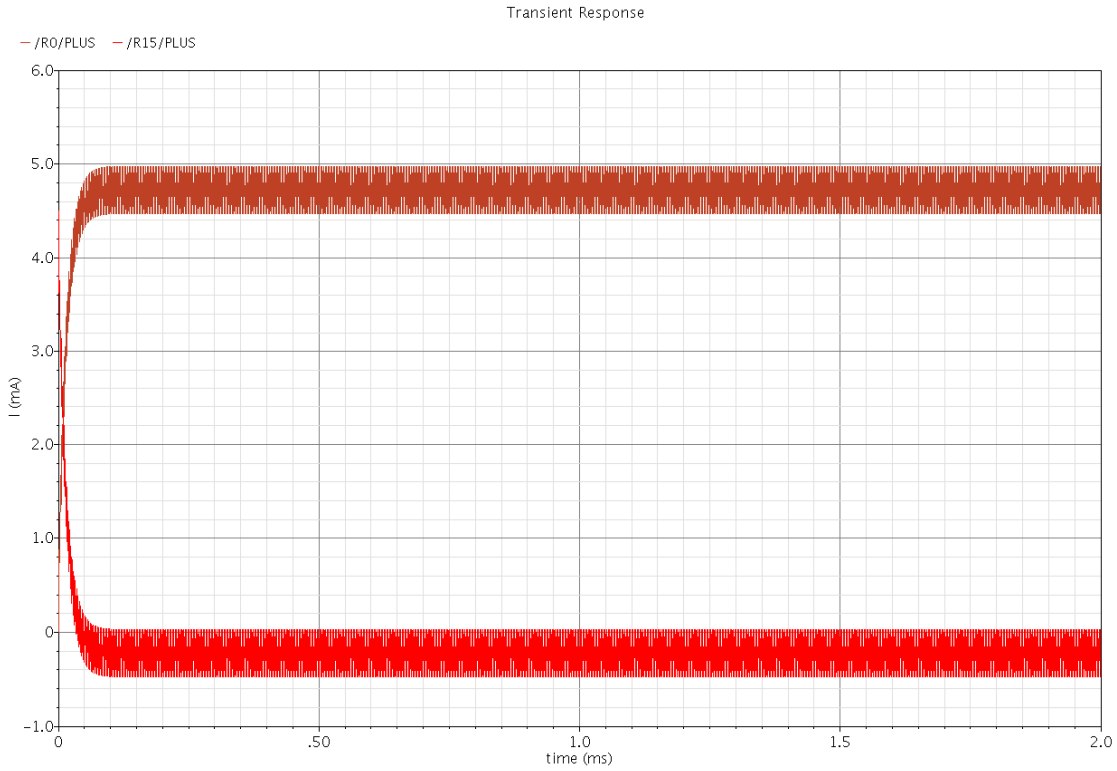


Fig3.5 a Inductor ripple current, b OTA ripple current

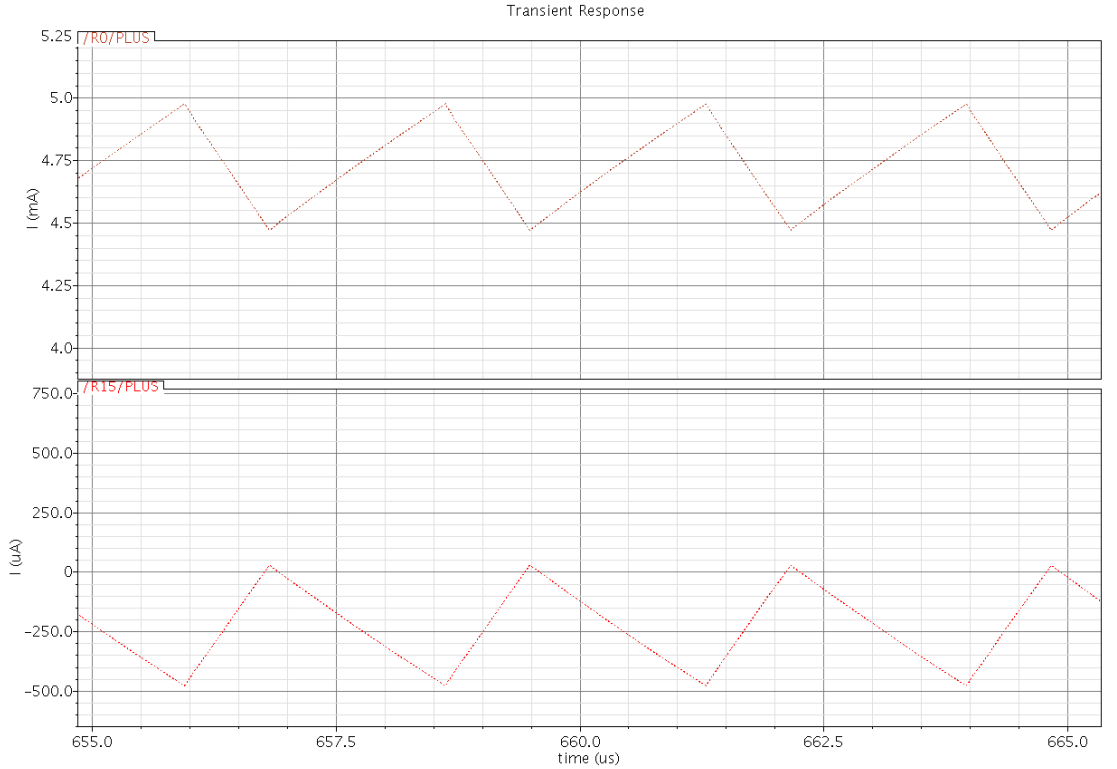


Fig 3.6 zoomed view of Fig 3.5

This technique cancels inductor ripple and produces a dc current to load. A parametric sweep was set up to verify this basic concept for parameter variations like transconductance gm, load resistance $R_{L,}$ duty cycle and input voltage V_{IN}.

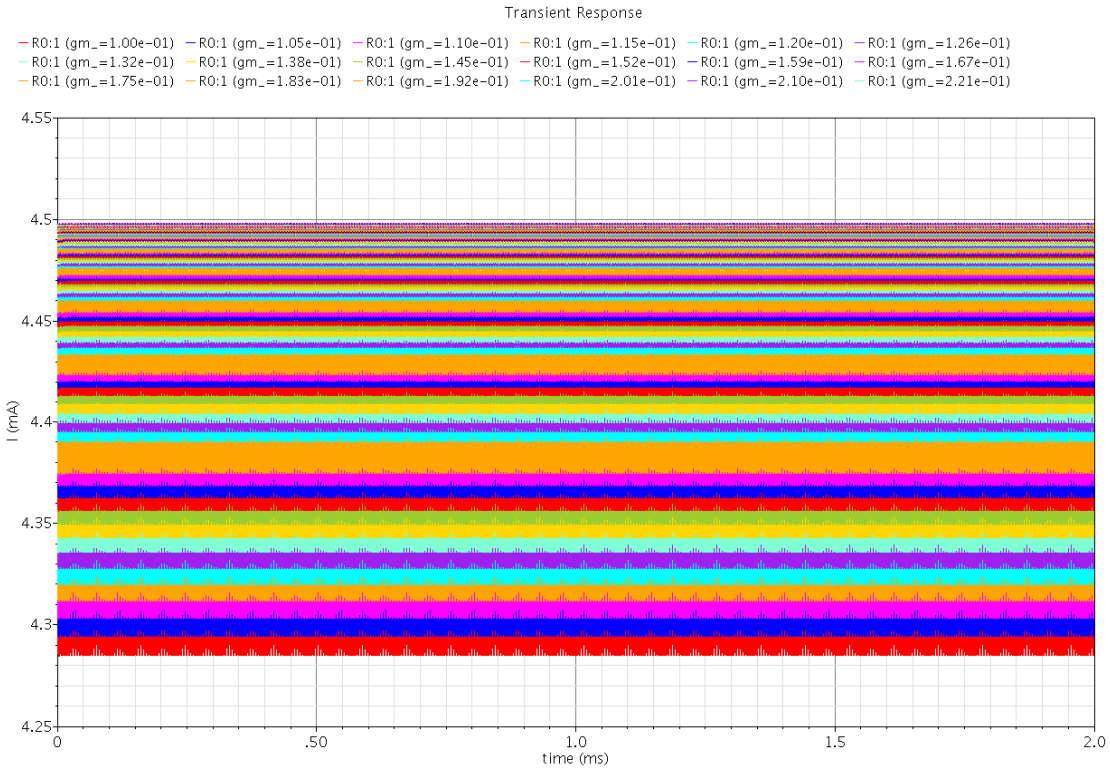


Fig 3.7 Inductor current after ripple rejection

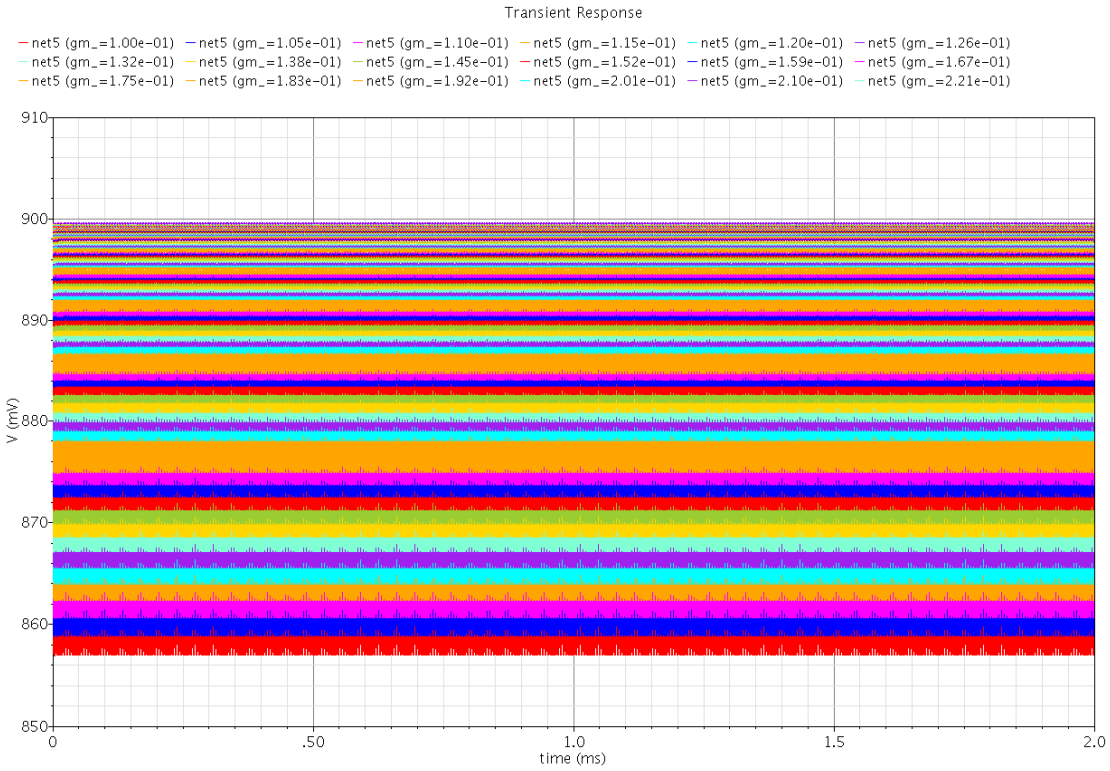


Fig 3.8 Output voltage after ripple rejection

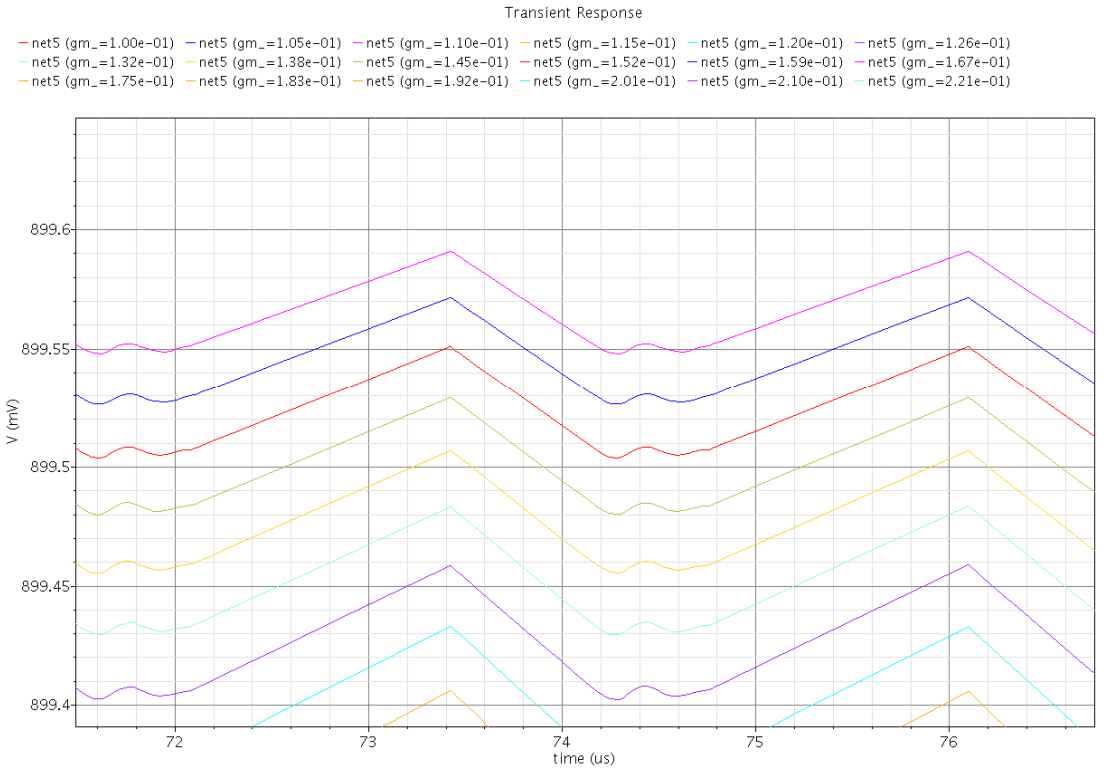


Fig 3.9 Output voltage ripple (Top purple graph for Gm = 1)

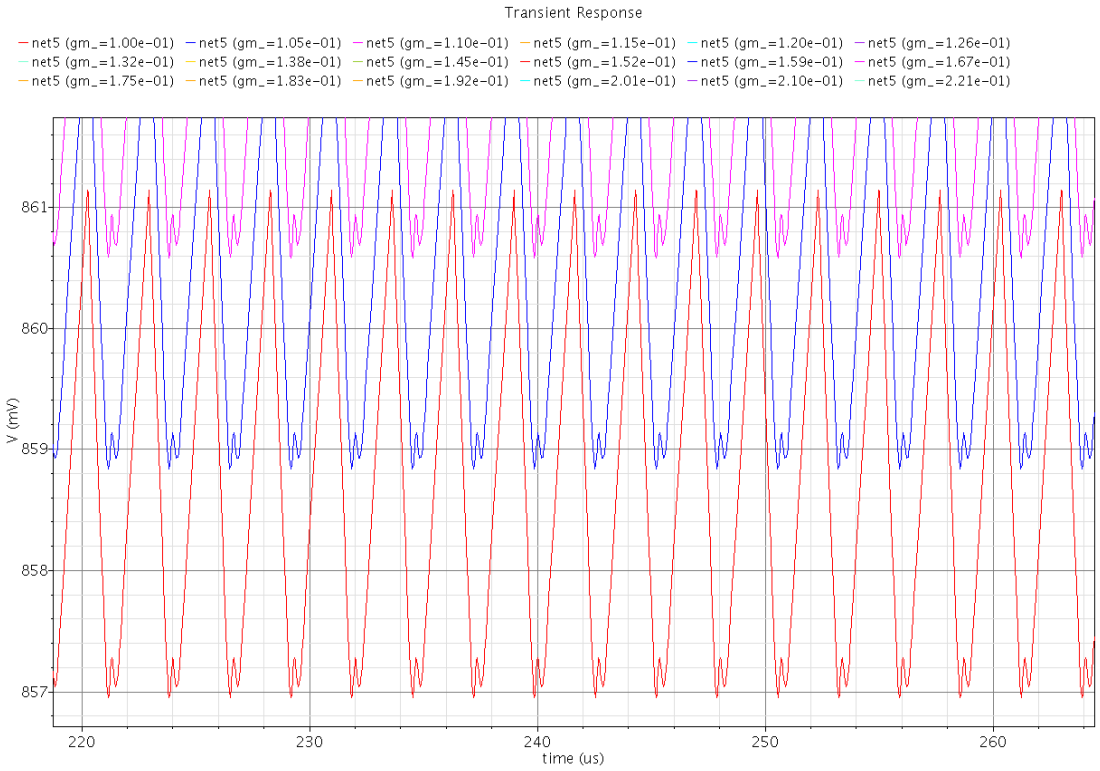


Fig 3.10 Output voltage ripple (red bottom graph for Gm = 0.01)

Figs. 3.7 – 3.10 show the load current and voltages after ripple rejection. The following conclusions are drawn from these simulations

1. Fig 3.9 shows that a final ripple of 8 μV was achieved when G_m was set to 1.
2. Figs. 3.9 and 3.10 demonstrate that if a G_m tuning mechanism is applied, ripple voltages can be controlled.

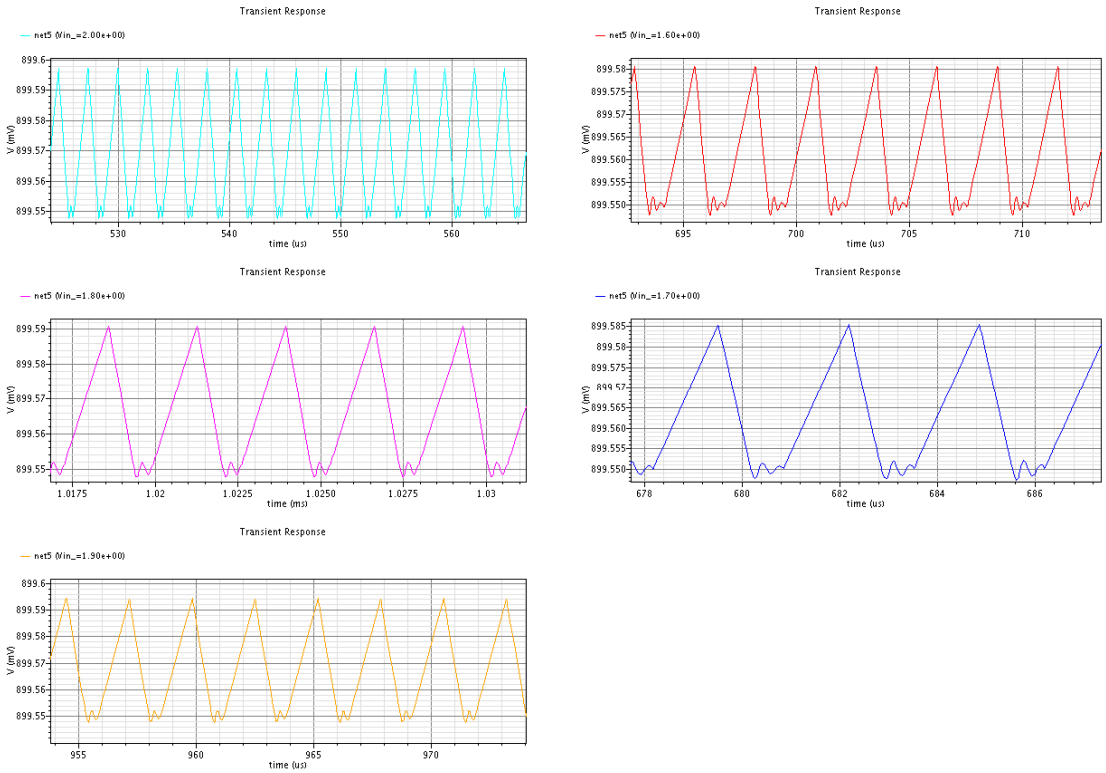


Fig 3.11 Output voltage for various input voltages

Fig 3.11 shows output voltages when V_{IN} is swept from 1.6V to 2.0V which is +/- 10% of nominal supply voltage. This V_{IN} independence was achieved by common mode biasing of OTA.

Temperature Independence

MOSFET drain current is described as

$$I_D = 1/2\mu\, C_{OX}\, W/L\, (V_{GS} - V_{TH})^2 \qquad (3.1)$$

Where

μ is mobility of a charge carrier (electron/hole in NMOS/PMOS)

V_{GS} is drain to source voltage

C_{OX} is oxide capacitance

W is channel width

L is channel length

V_{GS} is gate to source voltage

V_{TH} is threshold voltage

$$\partial I_D/\partial V_{GS} = \mu C_{OX} W/L (V_{GS} - V_{TH}) = g_m \quad (3.2)$$

Mobility (μ) and Threshold voltage (V_{TH}) of a MOSFET are temperature dependent [28] and can be described by eqs. (3.3) and (3.4).

$$\mu \alpha T^{-3/2} \quad (3.3)$$

$$V_{TH} \alpha T^{-1} \quad (3.4)$$

Eqs. (3.3) and (3.4) show that changing μ and overvoltage $V_{OV}(= V_{GS} - V_{TH})$ due to change in temperature does compensate each other up to certain extent, however residue can be compensated using G_m tuning mechanism. However a better circuit [10] is used to do temperature compensation, instead of relying on a G_m tuning mechanism.

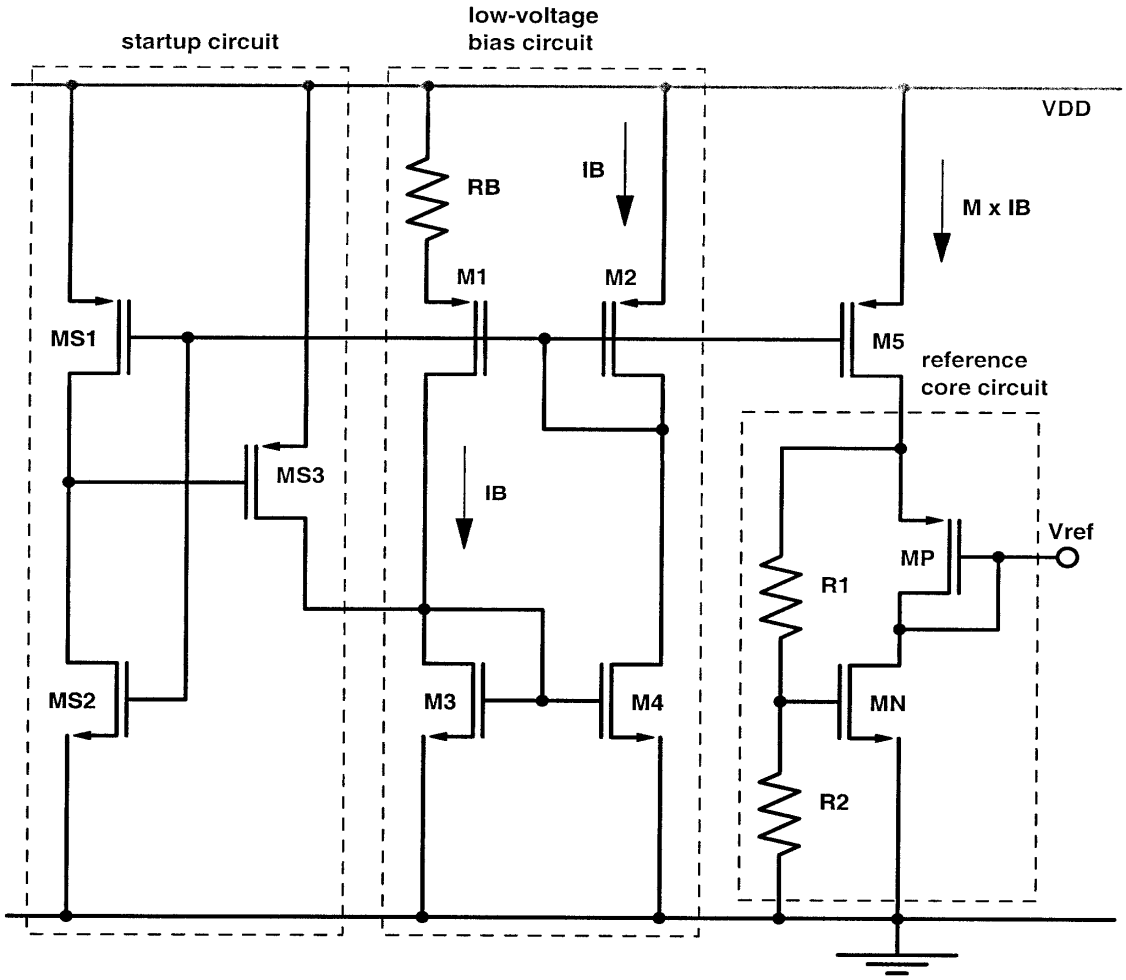


Fig 3.12 Achieving Temperature independence

A temperature insensitive bias generator shown above in Fig 3.12 is based on the different temperature dependencies of threshold voltages of NMOS and PMOS. A low temperature drift reference voltage can be obtained [11] by mutually compensating the temperature drifts of V_{THN} and V_{THP}. Magnitudes of V_{THN} and V_{THP} decrease linearly with temperature and can be modeled as:

$$V_{THN}(T) = V_{THN}(T_0) - \beta_{VTHN}(T - T_0) \quad (3.5)$$

$$|V_{THP}(T)| = |V_{THP}(T_0)| - \beta_{VTHP}(T - T_0) \quad (3.6)$$

Where T_0 is the reference temperature where the design needs to be centered (generally 27ºC), and β_{VTHN} and β_{VTHP} are the temperature coefficients of the threshold voltages of NMOS and PMOS transistors, respectively.

Final voltage reference is obtained by subtracting $|V_{THP}|$ from a scaled V_{THN}.

A low voltage bias circuit is formed by M1-M4 and R_B. A start up circuit formed by MS1-MS3 is embedded. Bias current to core reference circuitry is supplied by M5. Core reference circuitry is formed by MN, MP, R1 and R2. It is noted that the source bulk voltage of MP (V_{SB}) is set to zero to eliminate the back gate bias effect and improve power supply rejection ratio (PSRR). Reference voltage is:

$$V_{REF} = (1 + R1/R2)V_{GSN} - |V_{GSP}| \tag{3.7}$$

Temperature dependence of Vref can be obtained by differentiating eqn 3.7 with respect to T as given by eqn 3.8.

$$\begin{aligned}\frac{\partial V_{\mathrm{REF}}}{\partial T} &= \left(1+\frac{R_1}{R_2}\right)\frac{\partial V_{\mathrm{GSn}}}{\partial T} - \frac{\partial |V_{\mathrm{GSp}}|}{\partial T} \\ &= \left[-\left(1+\frac{R_1}{R_2}\right)\beta_{vthn} + \beta_{vthp}\right] \\ &\quad + \frac{\beta_{\mu_p}}{T_o}\sqrt{\frac{2MI_B(T_o)}{\mu_p(T_o)C_{ox}\left(\frac{W}{L}\right)_p}} \\ &\quad \times \left[\left(1+\frac{R_1}{R_2}\right)\left(\frac{1}{2}+\frac{\beta_{\mu_n}}{2\beta_{\mu_p}}\right)\sqrt{\frac{\mu_p(T_o)\left(\frac{W}{L}\right)_p}{\mu_n(T_o)\left(\frac{W}{L}\right)_n}}\right. \\ &\quad \left. \times \left(\frac{T}{T_o}\right)^{(\beta_{\mu p}+\beta_{\mu n}-2/2)} - \left(\frac{T}{T_o}\right)^{\beta_{\mu p}-1}\right] (\end{aligned} \tag{3.8}$$

This temperature dependence is governed by a linear term and a non linear term. To obtain $(\partial V_{REF}/\partial T)|T=T_r=0$ where T_r is room temperature, the linear term is set to zero by a resistor ratio, which is given by:

$$R1/R2 = \beta_{VTHP}/\beta_{VTHN} - 1 \tag{3.9}$$

And, the non linear term is set to zero at $T = T_r$ by the transistor sizing ratio, given by:

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\frac{\mu_n(T_o)}{\mu_p(T_o)}\left(\frac{T_r}{T_o}\right)^{\beta\mu p-\beta\mu n}}{\left(\frac{\beta_{vthp}}{\beta_{vthn}}\right)^2\left(\frac{1}{2}+\frac{\beta_{\mu_n}}{2\beta_{\mu_p}}\right)^2}. \tag{3.10}$$

Eqns. 3.9 and 3.10 show that temperature coefficients can be optimized by circuit parameters.

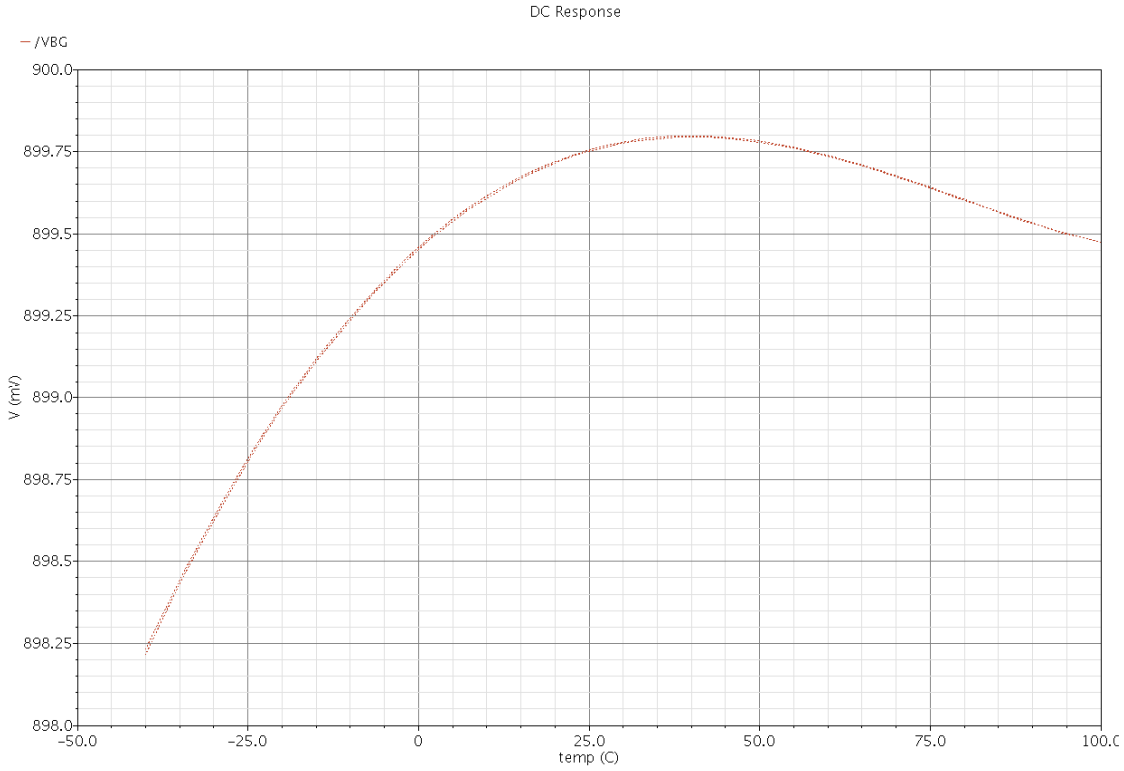


Fig 3.13 Temp Compensation simulation

Fig 3.13 shows the output compensated for temperature variations. It also shows the sweet spot at 27ºC.

CHAPTER 4 OUTPUT TRANSCONDUCTANCE AMPLIFIER (OTA) DESIGN

A study of several possible OTA architectures, including telescopic, two-stage and a simple differential pair with a cross-coupled, current cancelling load was performed, however since analog design is a multi dimension optimization problem [14], after careful consideration and evaluation of all parameters, folded cascode topology was chosen. It was determined that the folded cascode would provide the capability of maximizing the voltage swing at the output while still meeting the gain, bandwidth and noise requirements imposed by the application and specifications. The differential pair with cross coupled load [15] was thought to be of interest until the effect of a mismatch in the g_m of the load transistors was considered. Under realistic mismatch conditions in production, this circuit would not have met the gain requirement. The telescopic topology, while offering some improvement in noise, gain and bandwidth over the folded cascode, imposes significant limitations on output voltage swing. A two stage amplifier could easily meet all specifications, but would likely be less power efficient than the folded cascode.

The design was completed utilizing a "divide and conquer" approach. After all constraints were determined and design equations were derived or researched, a Matlab script was developed based on the design equations. This script was used to search the design space for a circuit that would meet all specifications while minimizing power consumption. The final circuit was designed step-by-step, starting with as many ideal components as possible, and ending with a completed practical circuit, except for an ideal common-mode feedback (CMFB) sub-circuit. The CMFB circuit was not considered to

fall within the scope of this design.

Folded cascade design: First Step

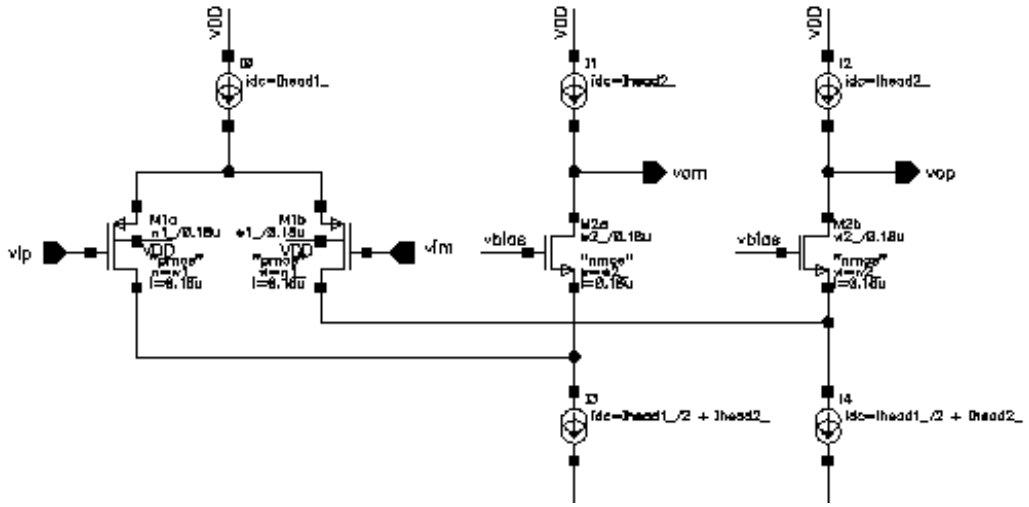


Fig4.1 Folded Cascode with Ideal components

The initial design was modeled with only four transistors. A P-FET input stage was selected for better noise performance as compared with an N-FET input. For the same g_m, a P-FET will require a larger area. The larger capacitance will lead to a lower kT/C for this stage. kT/C is a determining factor for circuit noise floor and therefore important design parameters need to be traded off with this.

The first design parameter that was considered was the closed-loop gain. For this simple circuit, the closed loop gain is:

$$T_0 = \beta \frac{g_{m1}}{g_{ds1}} \left(1 + \frac{g_{m2}}{g_{ds2}} \right) \tag{4.1}$$

Where, g_{m1}, g_{m2} are transconductances of M1 and M2 and g_{ds1} and g_{ds2} are their output conductances. β is the feedback factor.

It is known that the open-loop gain requirement with a small margin is on the order of 120, and that β is on the order of 1/3. So our closed-loop gain requirement is on the order of 40.

If this were the entire gain equation, the requirement for the intrinsic gain or M_1 and M_2 would be approximately $\sqrt{120}$, however the equation for the complete folded cascode gain is:

$$T_0 = \beta \frac{g_{m1}}{\frac{g_{ds1}+g_{ds3}}{1+\frac{g_{m2}}{g_{ds2}}} + \frac{g_{ds5}}{1+\frac{g_{m4}}{g_{ds4}}}} \tag{4.2}$$

The additional terms in the denominator will lower the gain somewhat, however, "back of the envelope" calculations based on practical g_m and g_{ds} values indicate that an intrinsic gain of 20 for all transistors will suffice. Furthermore, for practical values of g_m/I_D, in the chosen 0.18 μm technology, a 0.18 μm length will provide the needed gain for all transistors. This decision can be revisited later in the design process if further calculations indicate that it needs to be increased.

Taking the folded cascode design to the next level of complexity, the cascoded current sources, consisting of two transistors for each side of the differential pair, are inserted in place of the top-side current sources on the right side of the preceding circuit. The additional transistors have already been referenced in eqn (4.2). At this point, the only transistors that are omitted are the head current source for the input stage, the tail current sources for the output stage, and the voltage biases for all stages. The head current in the input stage is referred to at I_{head1} and the tail currents in the output stage are I_{tail2}. The voltage biases are also kept ideal at this point, conveniently spaced assuming V_{gs}

(V_{TH}+V_{OV}) for all transistors is 650 mV. Keeping these current and voltage sources ideal for most of the rest of the design process will simplify searching the design space for a good solution.

Folded Cascode Matlab Model

In order to more efficiently investigate design tradeoffs, a Matlab model for the amplifier was developed. The Matlab code is provided in Appendix A.

The first calculation in the Matlab model relates the transit (unity current-gain) frequency of M_2 to $\omega_{px} = g_{m2}/C_X$, where C_X is an estimate of the load capacitance on M_2. The design equation for the phase margin and its approximate relationship with the transit frequency of M_2 are:

$$PM \approx \tan^{-1}\left(\frac{\omega_{px}}{\omega_C}\right) \qquad \omega_{px} \approx \omega_T / 3 \qquad (4.3)$$

Based on these two relationships, the transit frequency of M_2 can be determined from the choice of PM. A 75° target for PM was selected to maximize bandwidth and minimize settling time for the switched capacitor application of the OTA.

The design script includes three design "knobs", as follows:

$$\frac{C_{gg1}}{C_s + C_f}, \quad \frac{C_{gg2}}{C_{Ltot}}, \quad \frac{C_{gg4}}{C_{Ltot}}$$

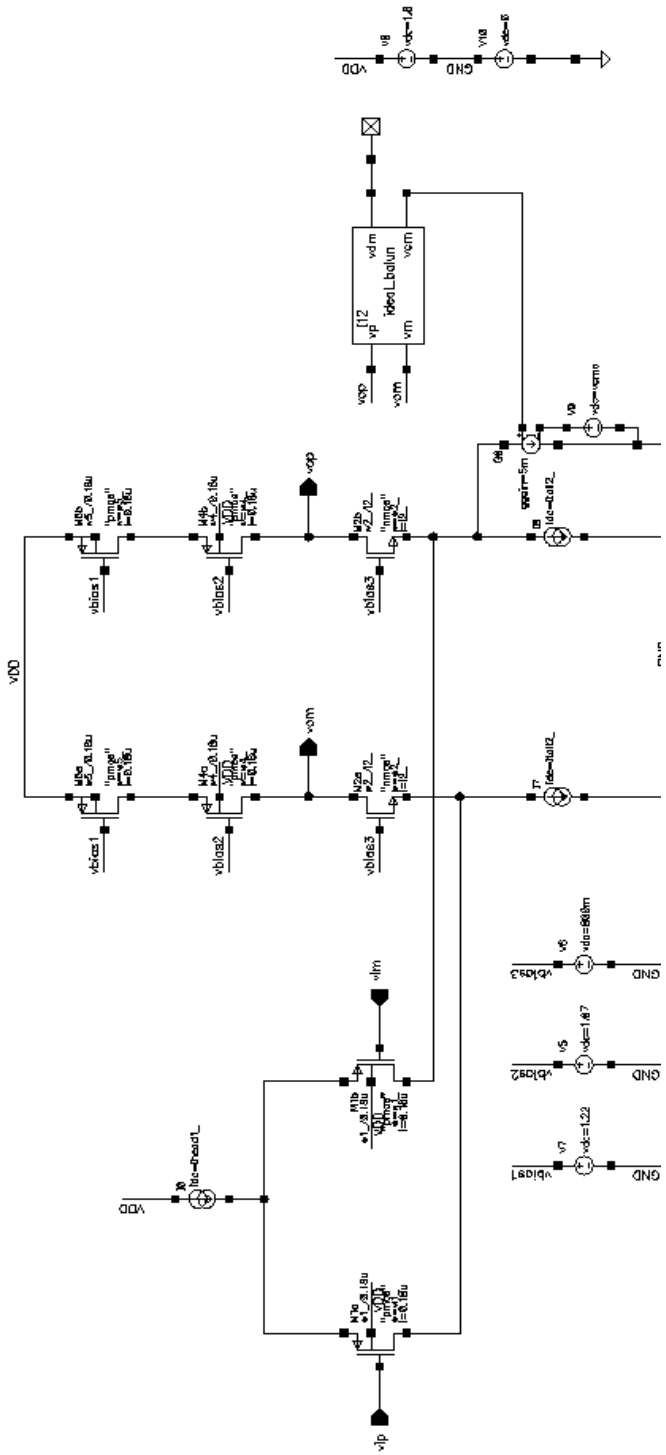


Fig 4.2 Optimized folded cascade with I_{head_ideal} and I_{tail_ideal}.

The total capacitance seen at the load is calculated based on:

$$C_{L,tot} = C_L + C_{dd2} + C_{dd4} + (1-\beta)C_f \tag{4.4}$$

g_m for M_1 is calculated based on the bandwidth requirement using the approximation:

$$\omega_c \approx \frac{\beta g_{m1}}{C_{L,tot}} \tag{4.5}$$

g_m for M_2 is calculated based on the previously calculated transit frequency for M_2 and one of the design knobs. With these parameters in place, the remainder of the design script consists of looking up g_m/I_D for M_1 and M_2, calculating the currents, looking up I_D/W, calculating the widths, and in turn using these data to back out all of the other parameters for all of the transistors in the circuit.

The versatility of this design script was indispensible in the process of converging on an overall solution to the circuit. The design space was searched with several parameters. I investigated whether the transistor lengths affected power consumption and found that the effect was small. Since chosen minimal lengths were also confirmed as sufficient to meet the gain requirements of the circuit, I was able to consider them as fixed and move on to my other design variables. As I worked my way through choosing each of the parameters, I was constrained by the practical limits of the 0.18 μm technology.

The following equation, derived by Y. Guo [20], was used to gain insight into the noise performance of the circuit:

$$\overline{v_0^2} = \frac{1}{\beta}\frac{kT}{C_L}\gamma_p\left(\begin{array}{l} 1+\frac{\gamma_n}{\gamma_p}\frac{g_{m2}}{g_{m1}}\frac{\omega_C}{\omega_{pX}}+\frac{\gamma_n}{\gamma_p}\frac{g_{m3}}{g_{m1}}+ \\ \frac{g_{m4}}{g_{m1}}\frac{\omega_C}{\omega_{pY}}\frac{1}{1+\frac{\omega_C}{\omega_{pY}}}+\frac{g_{m5}}{g_{m1}}\frac{1}{1+\frac{\omega_C}{\omega_{pY}}} \end{array}\right) \tag{4.6}$$

This equation indicates that keeping the other transconductances in the circuit small as compared to g_{m1} would reduce noise. Since both g_{m1} and g_{m2} are constrained by other design decisions, we investigated the power consumption and practical implications of minimizing g_{m3}, g_{m4} and g_{m5}, and in fact found that keeping these small improved the power performance as well as the noise performance. We found that within the practical limits of the technology, 0.3 was a reasonable choice for g_{m3}/g_{m1} and 0.1 would be reasonable for g_{m4}/g_{m1} and g_{m5}/g_{m1}.

Of our remaining design knobs, again, by using the Matlab design function to do some searches of the multi-variable design space that we had defined, $C_{gg4}/C_{L,tot}$ was determined to be approximately 1/1000 to minimize power. With all of these selections in hand, we plotted the current through M_3 as a function of $\frac{C_{gg1}}{C_s+C_f}$ *and* $\frac{C_{gg2}}{C_{Ltot}}$, resulting in Fig 4.3 below:

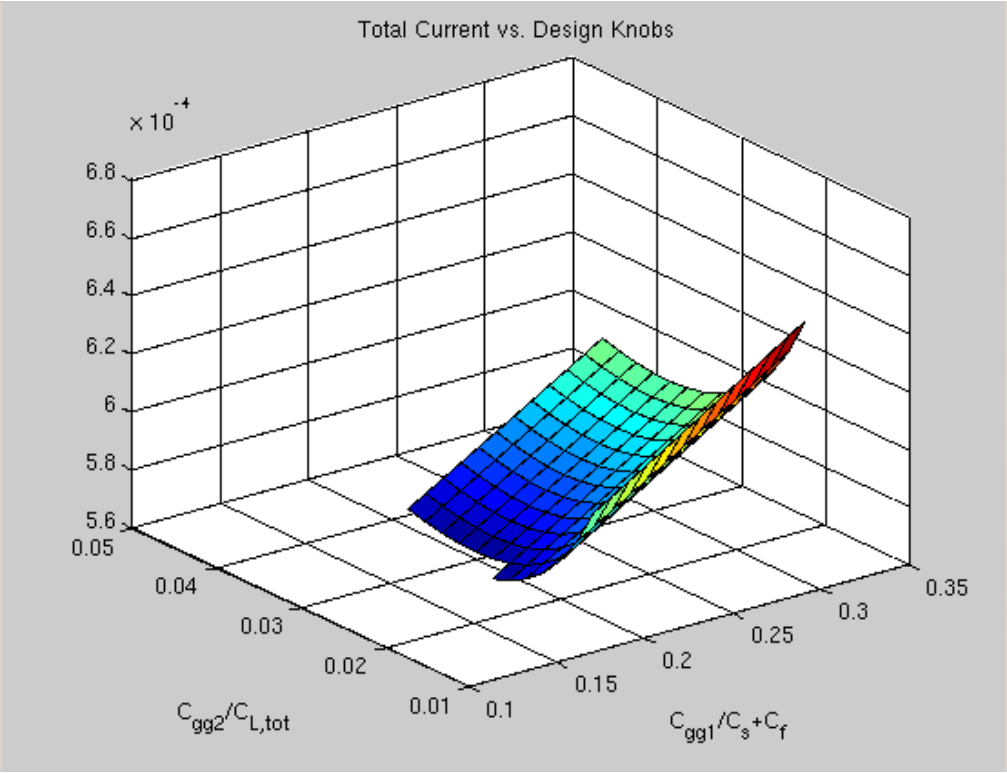


Fig 4.3 Matlab Contour plot for favorable design spot

The Matlab program that generated this plot was set up to leave blank any cell in the design space that was impractical from the standpoint that g_m/I_D was not realizable or any of the resulting devices would be impossible or impractical for any other reason. For example, we chose to disallow device widths greater than 300 μm. For this reason, we do not see the characteristic bowl shape, but a shape that does have a minimum along the $C_{gg2}/C_{L,tot}$ axis, but falls off to impractical values along the $C_{gg1}/(C_s+C_f)$ axis. The script also automatically produced a function call to generate the lowest-power practical design:

```
[m1, m2, m3, m4, m5] = fc_new(0.157, 0.0345, ...
  0.001, 0.18e-06, 0.18e-06, 0.3, 0.1, 0.1, tech)
```

The final values from this process are (to two significant digits):

W1 = 200 μm

W2 = 38 μm

W3 = 50 μm

W4 = 30 μm

W5 = 30 μm

I_{head1} = 800 μA

Itail2 = 440 μA

At this point, the circuit in Fig 4.6 was simulated and determined that design script was indeed coming up with reasonable values. The gain was correct, and the passband performance met specifications. The noise was extremely low, leaving plenty of room in the noise budget for the bias circuitry.

The stop band attenuation specification was not met, coming out to be approximately 33 dB instead of 35 dB. Upon further investigation, it was found that the phase margin was 101°, not the target of 75°. However, since M_3 was not yet in the circuit, and the drain capacitance of M_3 would have the effect of decreasing the phase margin, we deferred judgment on this until the circuit was completed.

Completing the Design

Bias Voltages and Current Sources

A voltage insensitive bias circuit was designed to generate V_{TH}+V_{OV} where V_{TH} is 0.5 V for PMOS and NMOS devices in TSMC 0.18 μm mixed signal process technology (t018ms) and V_{OV} was chosen to be 150 mV. Cascode PMOS devices required a V_{GS} (=

$V_{TH} + V_{OV}$) of 1.15 V and 900 mV and NMOS devices need 650 mV and 800 mV. An off-chip current reference of $I_{head1}/10$ was used to generate a 1 V reference using the configuration in Fig. 4.4. To bias the cascode devices, a stack of devices driven by a current source is used. This scheme provides a high swing cascode bias [1]. M1 in Fig. 4.4 is in saturation and M2 operates in the triode region. The size of the composite combination determines the reference voltage, V_{GS2}, which is used to bias subsequent stages. Fig. 4.5 shows the actual biasing block, which generates cascode biases and mirror currents.

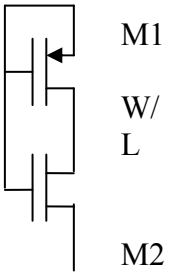


Fig 4.4 Bias generation

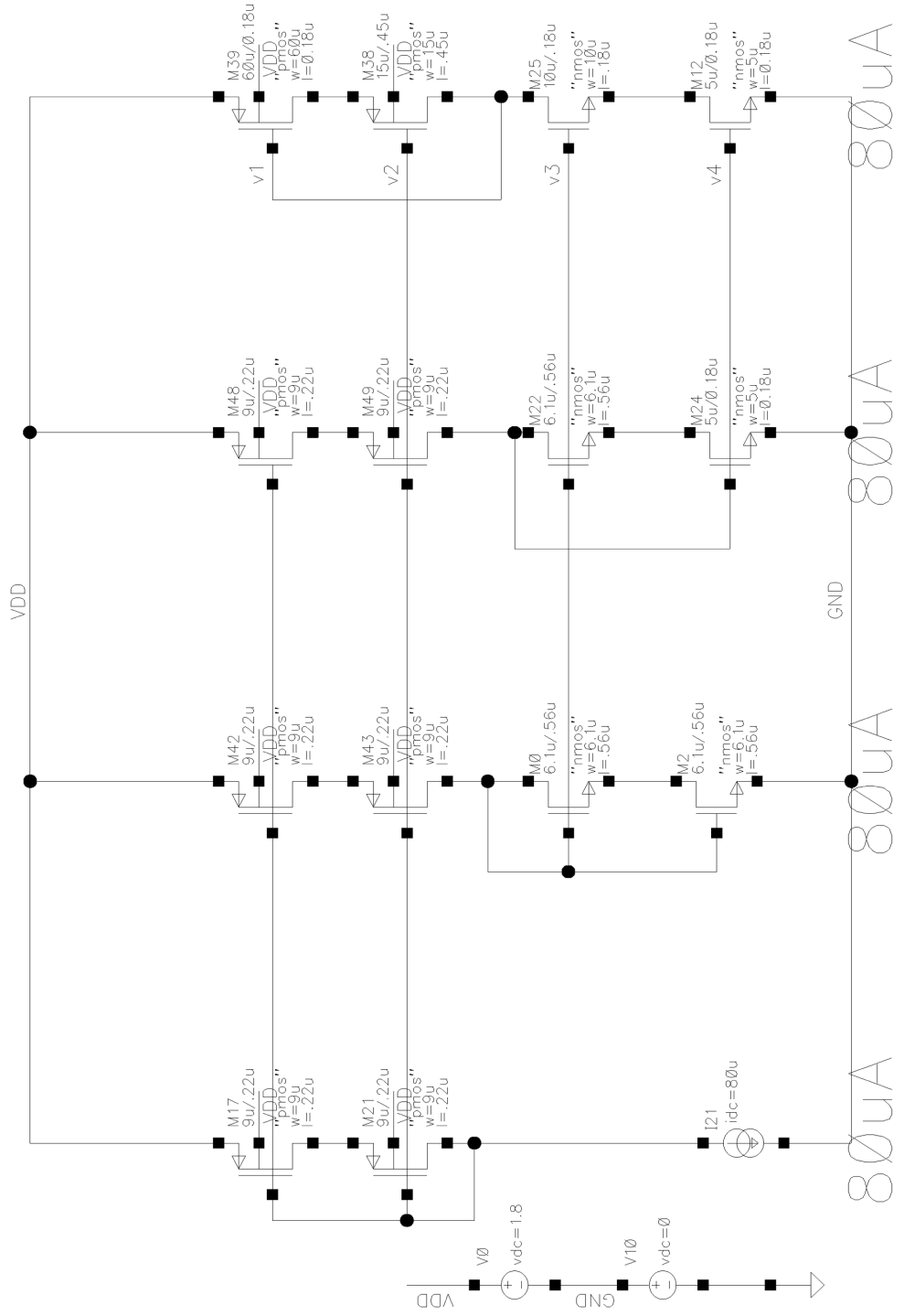


Fig 4.5 Final bias generation block

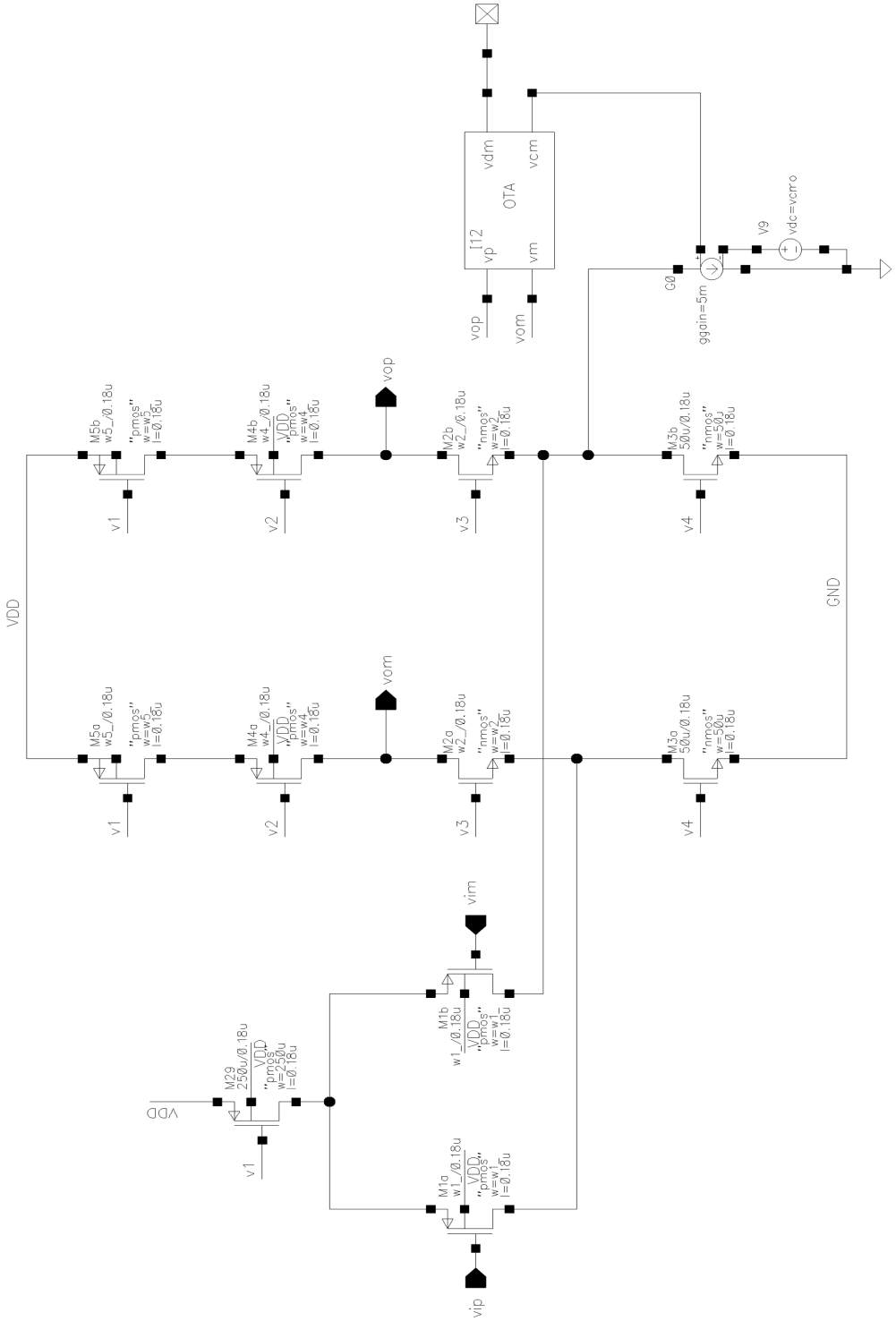


Fig 4.6 Folded cascode final schematic

Folded Cascode Design Evaluation

The transient response of folded cascade OTA to a 20 mV step is shown in Fig 4.7. The step begins at 100 ns and a sampling period is ~9.65 ns. In this case, 0.1% dynamic settling is confirmed. We also ran several other transient simulations. For larger steps, the settling can get beyond 0.1%, but is never greater than 0.5-1.0%. In the specific application that I am designing for, I have not seen steps of greater than 20 mV in practice for input signals in the pass band.

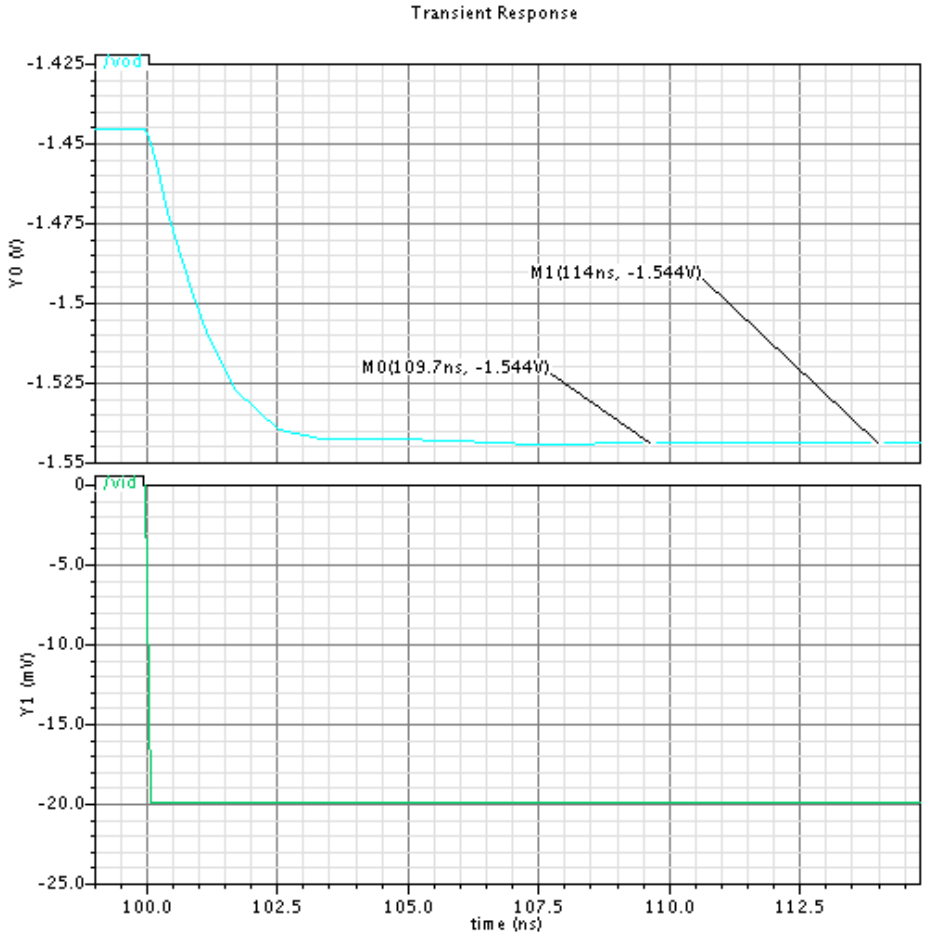


Fig4.7 step response of folded cascade OTA

For Fig. (4.8), an input signal was chosen that intentionally clips at the output. This clearly shows one of the greatest strengths of the folded-cascode. The maximum output

swing is within less than 15 mV of the supply rails. This figure also shows some artifacts of distortion at higher drive levels, as has been previously discussed.

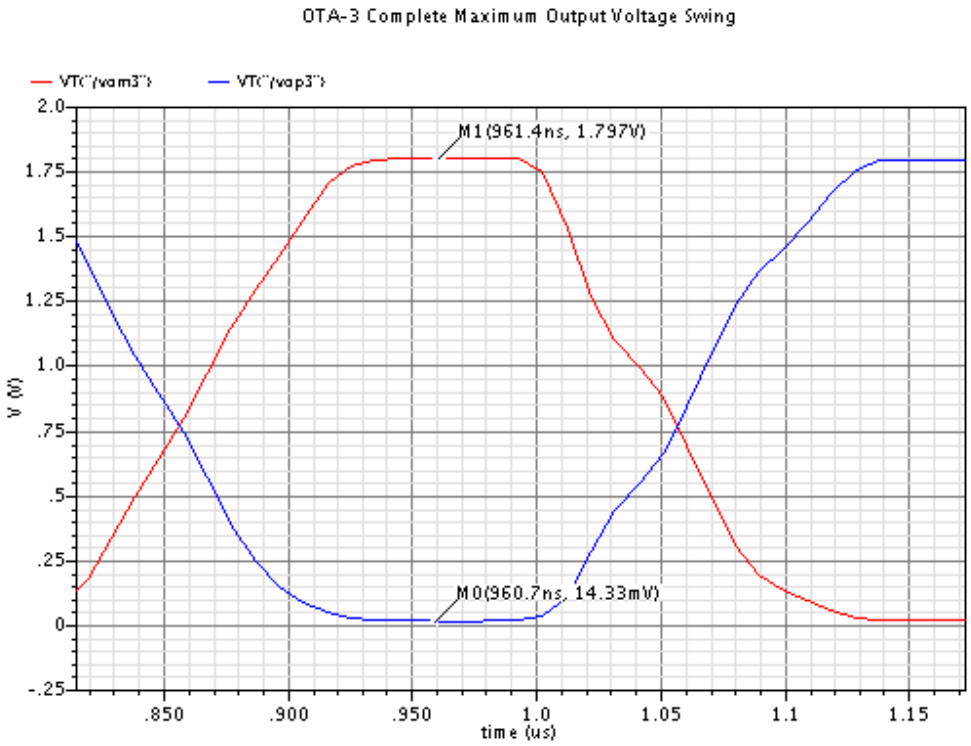


Fig 4.8 *Maximum Output Swing*

A closed-loop Bode plot for the intermediate version is shown in *Fig. 4.9*. The closed loop gain and bandwidth agree perfectly with the results of the design process using the Matlab model. The phase margin is 102°. This is right on target to achieve a 75° phase margin once the ideal tail currents are replaced with M3a and M3b, which will introduce a drain capacitance that will decrease phase margin.

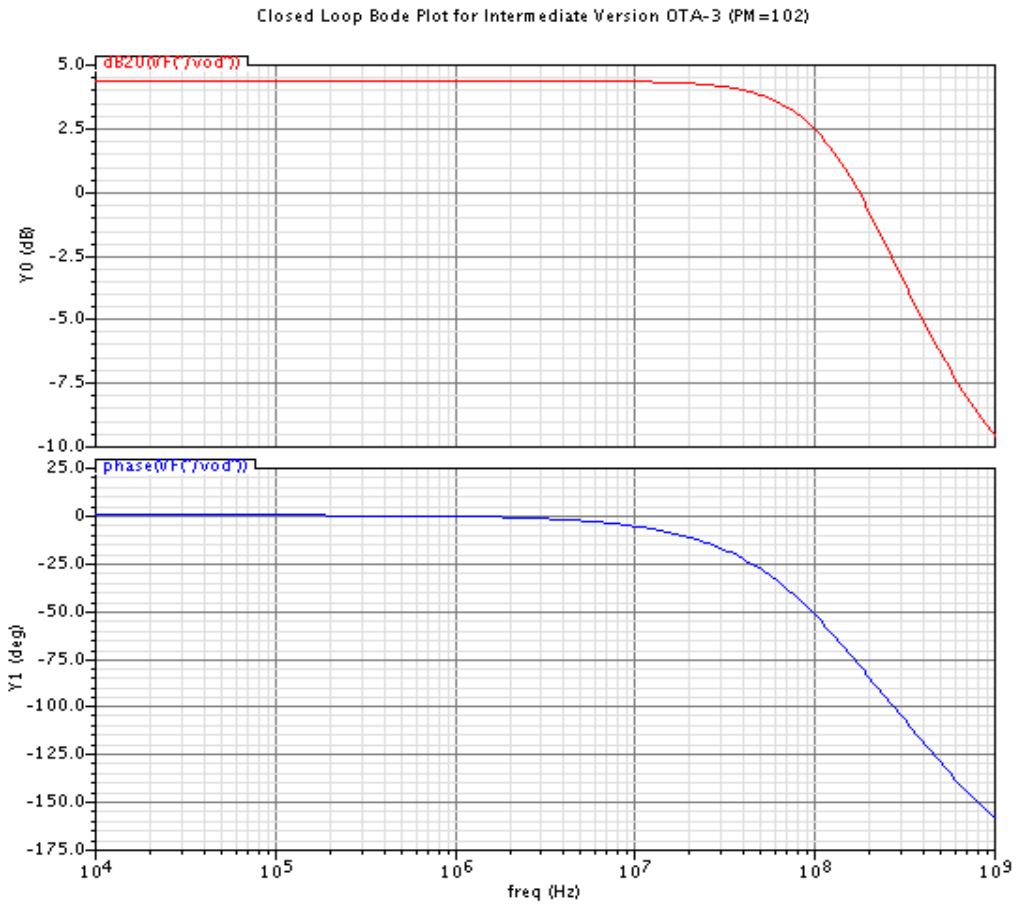


Fig 4.9 *Closed Loop Response for Intermediate Version*

Fig. 4.10 is the closed loop response for OTA-3, complete with the bias circuitry. This AC simulation indicates a problem with the gain that was not present until the bias circuit was introduced. This plot actually shows an increase in the phase margin, where we should be seeing a decrease from 102° to approximately 75°. However, the shape of the magnitude plot indicates the bandwidth enhancement that we are looking for is indeed present. The problem is with gain, and this problem is caused by the current sources. If this were fixed, the gain margin would be correct.

The circuit parameters selected through careful modeling and using Matlab to search the multi-variable design space led to a design that meets all of the specifications perfectly.

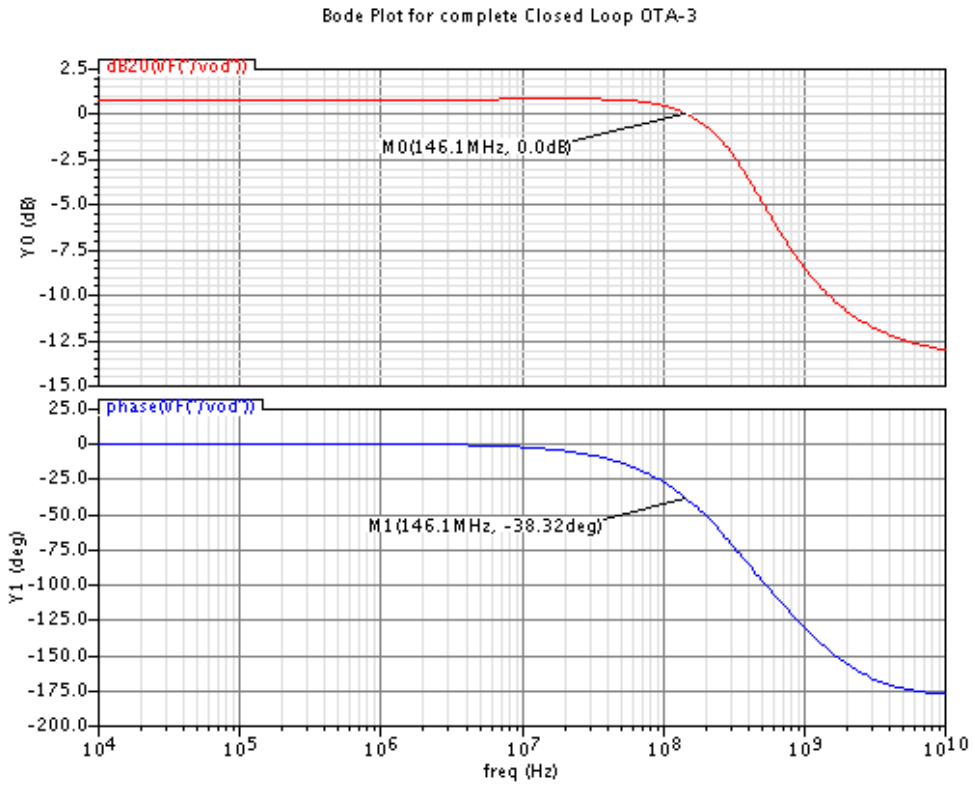


Fig 4.10 Closed loop response for complete OTA design

CHAPTER 5 FUTURE WORK

Gm Tuning for OTA

Fig 4.6 shows the completed OTA which uses bias current for g_m tuning. However a better technique could be combination of a folded cascade with the following arrangement as the first stage.

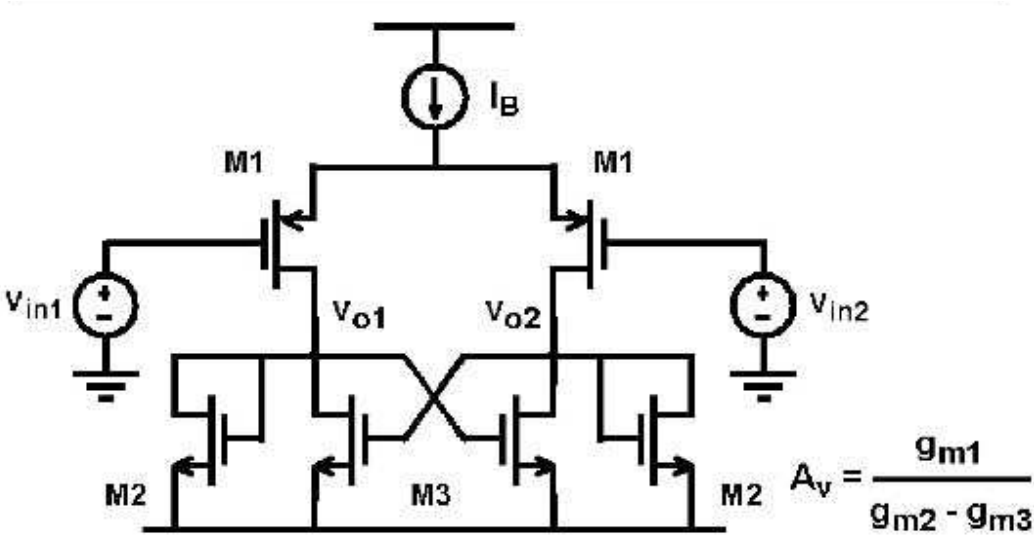


Fig 5.1 First stage of OTA for tuning mechanism

The idea of the final circuit of Fig. 5.1 came from bootstrapping and current cancellation. Fig. 5.2 shows that if large resistor values can be afforded then they can yield a self biased circuit. This topology results in a virtual (AC) ground between the gates which therefore results in twice the output resistance seen from either side. Therefore

$Av = g_m1. (R|| r_0).$ (5.1)

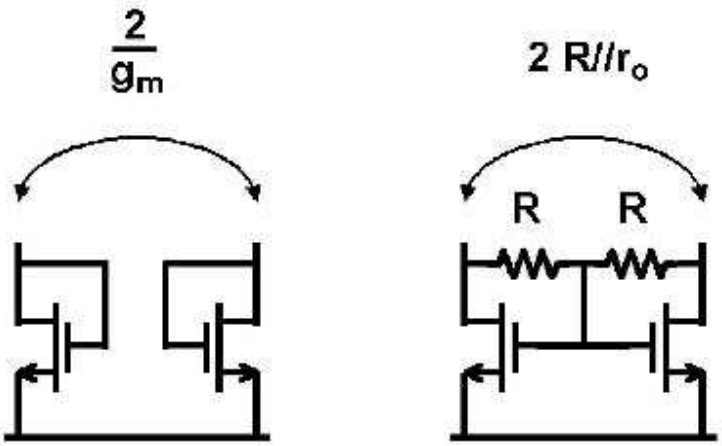


Fig 5.2 Self biased load

Circuit utilizing a self bias outlined in Fig. 5.2 will act as common mode feedback due to AC current cancellation. The gain of this configuration is moderately high.

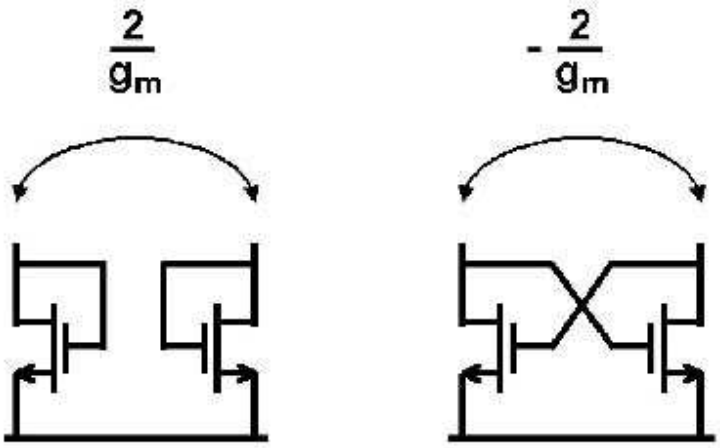


Fig 5.3 AC current cancellation technique

Even more gain can be obtained by current cancellation. For this purpose, we need to use differential diode connected MOSFETs. Two of them provide a differential small-signal resistance of $2/g_m$. Cross coupling them creates a positive feedback amplifier with two stages. As a result, the differential resistance becomes negative or $-2/g_m$. This negative resistance is easily controlled through the current. This is often used in oscillators, RF voltage-controlled oscillators and in wideband amplifiers.

Connecting a set of positive diode resistances with negative ones allows realization of any resistance between $1/g_m$ and ∞. By choosing device sizes to be same cancels AC current in the circuit, which results in very high differential output (infinite with 100% matching). This load is therefore an ideal load for a differential circuit. Another advantage of this kind of circuit is that since there is an AC current cancellation, it does not present any pole to the circuit and therefore two differential stages can be directly coupled without need for compensation. The final circuit is shown in Fig. 5.1.

Load devices need to be matched to avoid a mismatch error in a general purpose OTA, however for this kind of application, changing the size of load devices changes the load impedance and therefore changes the overall G_m.

Slew Rate Control for Non Overlapping Switching Action

A break before make strategy is applied which results into non overlapping clock generation. However, non overlapping clocks have a fixed amount of delay which affects the converter's efficiency. Using the slew rate techniques [23] described below, one switching action can be made faster and another switching action can be made slower. Two schemes are proposed for better and cost effective controllability of slew in a high side switch.

First Scheme:

In first scheme (as outlined in Fig.5.4),when EN goes high, a pulse generator generates a high pulse with a high duration of one clock period, which resets the counter to 0000 and one-hot decoder turns on switch SW1 which converts V_{DD} to the gate of PMOS. In next clock, counter advances one count and one hot decoder output turns on switch two which

connects 0.9 V_{DD} to PMOS gate and by virtue of which it slightly turns on the PMOS. In the next step, the counter advances to the next count and SW turns on. This process continues until the counter reaches its last count, forcing the last SW to turn on, which connects 0 V to the PMOS gate, which ensures that PMOS is fully turned on.

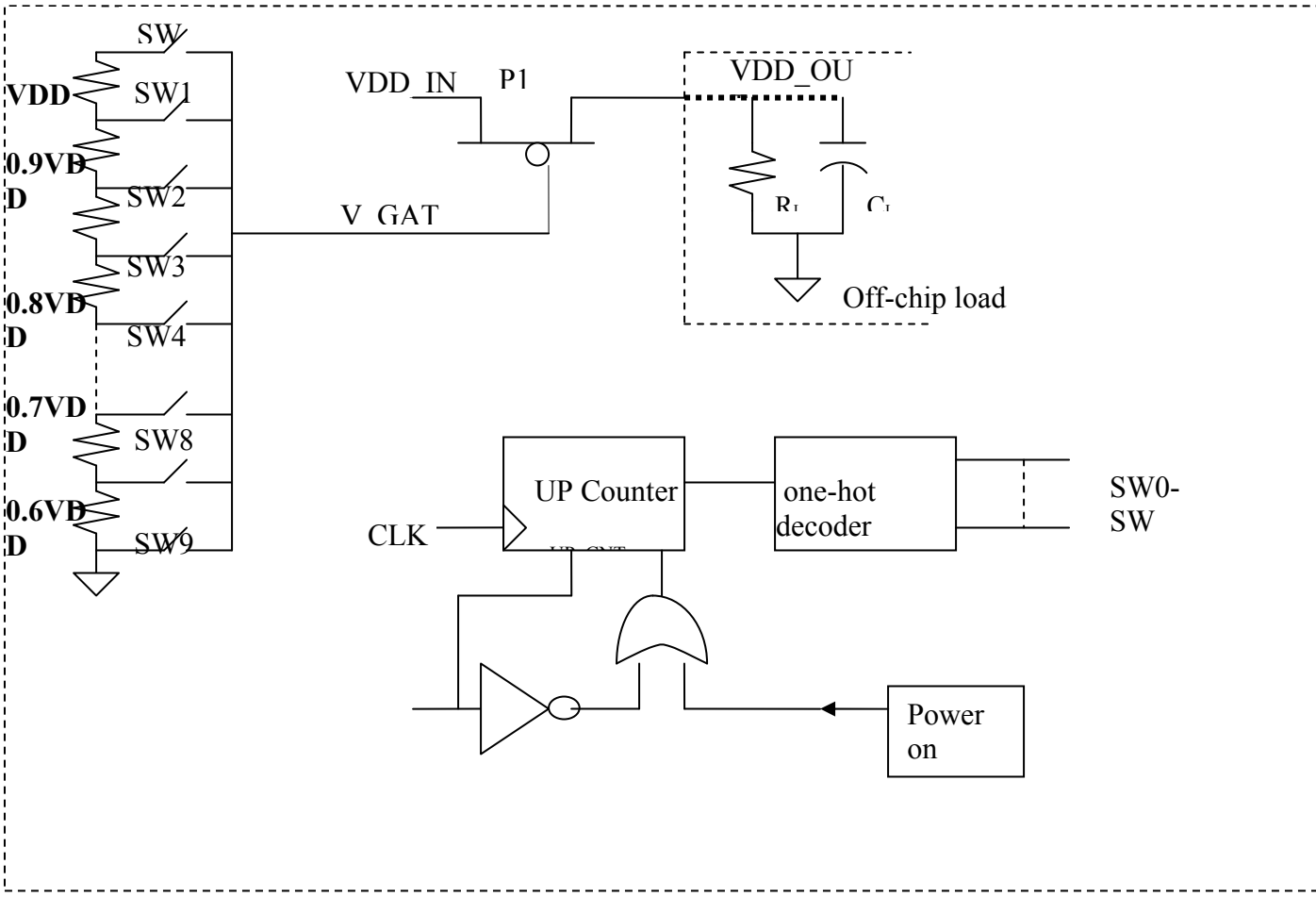


Fig 5.4 Slew rate control method I

This method uses controlled turn-on of high side switch P1 by controlling its gate voltage in several finer steps which controls the r_{ds}(on) by virtue of which it effectively controls the slew. P1 is a very big PMOS in order to support the large amount of current.

Turn on of P1 can also be delayed by this method, which helps prevent the switching transient generated due to the switching of the power supply.

Switching on the power supply results in a high power on reset (POR) signal generated by POR block. POR signal is ORed with EN' to control the reset of up counter. A low EN signal or a high POR signal can reset the up counter to 0000. EN controls the upward counting of the counter. When EN is high, the counter is incremented by 1 count with every clock edge. When the up counter reaches 1010 it stops, and stays at count 1010 until EN is high.

The up counter is connected to the one-hot decoder which is responsible for turning on a particular switch and turning off the others. Turning on a particular switch connects a particular reference voltage to the gate of the high side switch P1.

The high side switch needs to be on while the EN signal is high and it will be off when EN = 0. When EN signal is deasserted (EN = 0), it resets the up counter, which sets the default count value to 0000.

The resistive network on the left of Fig. 5.4 is used for generating references to be applied to gate for controlling the turn on of the high side switch P1. A R-2R DAC can also be used to generate more accurate reference voltage and to avoid a potential divider arrangement.

References generated can be non linear by having smaller potential steps in beginning and larger potential steps later.

At power up, POR block generates a high pulse which resets the up counter to 0000. One hot decoder turns on SW0 and turns off SW1-SW10 which connects V_{DD} voltage to gate of high side switch P1 ensuring that it will be fully turned off. When EN goes high it deasserts the reset and counter starts up counting with every rising clock edge. A count

output of 0001 ensures that 1 hot decoder will turn on SW1 and turns off other switches which will connect $0.1V_{DD}$ to gate of PMOS. This process will start incremental turn on of high side switch P1. When count reaches a value of 1010 it will turn on SW10 and turn off the other switches. Turing on switch SW10 will connect GND to the gate of P1, ensuring that switch is fully turned on. The counter will stop counting after reaching a value of 1010 until EN is high, which ensures that until EN is high, P1 is turned on.
A low EN will reset the counter, and the whole process will start again.

In order to delay the start of gradual turn on, for a few clock cycles V_{DD} can be connected to PMOS which will ensure that P1 will remain be switched off.

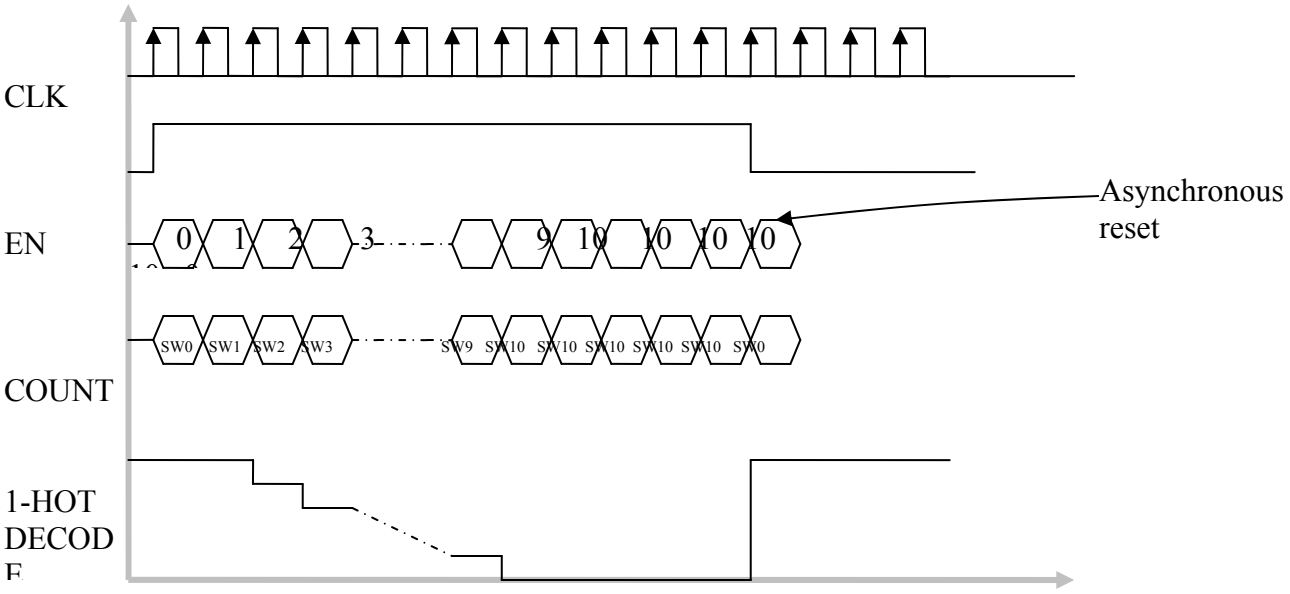


Fig 5.5 Slew Rate Control waveforms

Second Method

In another implementation, high side PMOS switch is implemented using several small PMOS switches P1 to Pn which have all the sources connected together and all the drains connected together. Gates are individually controlled to control the slew rate.

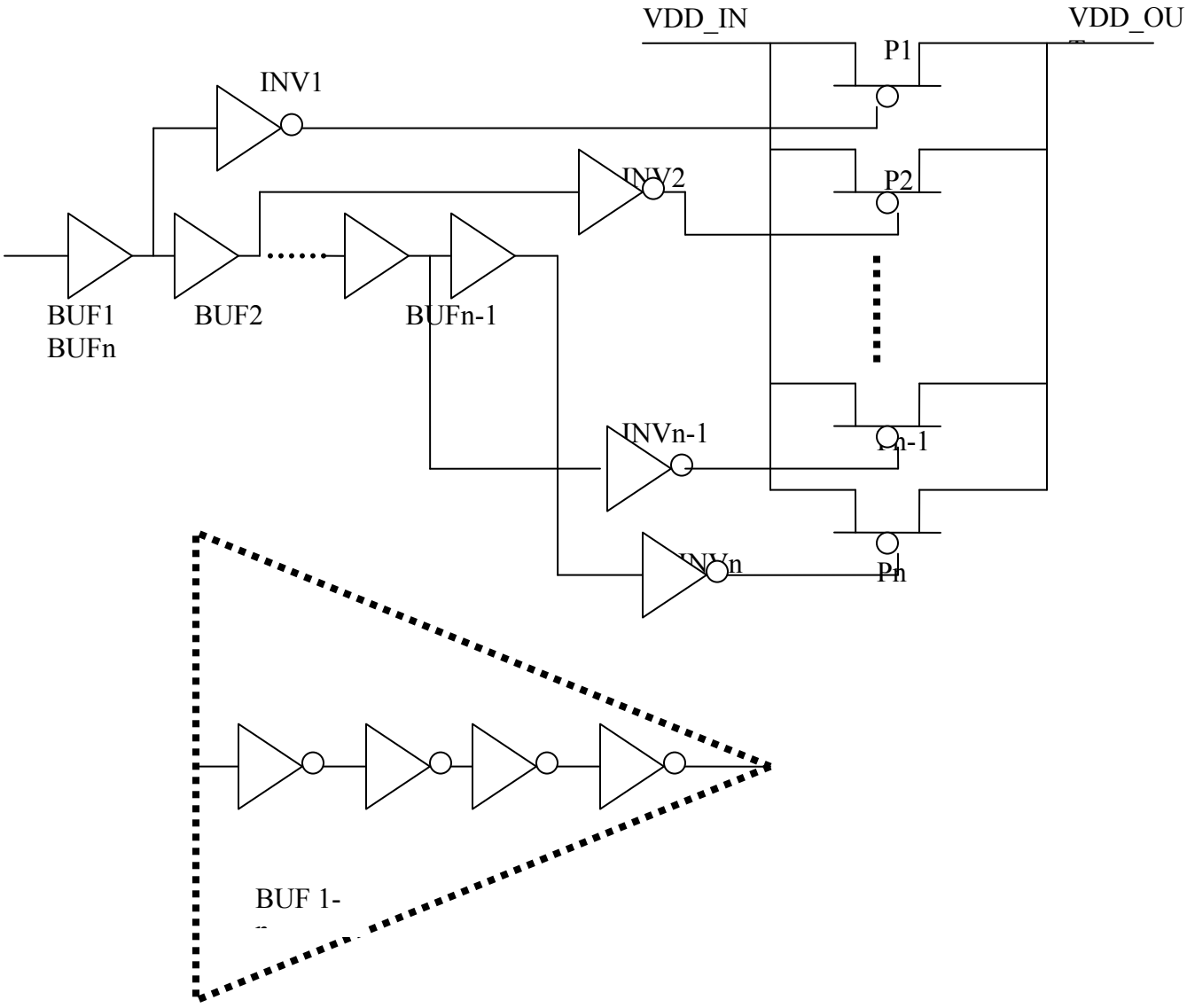


Fig 5.6: Slew Rate control Method II

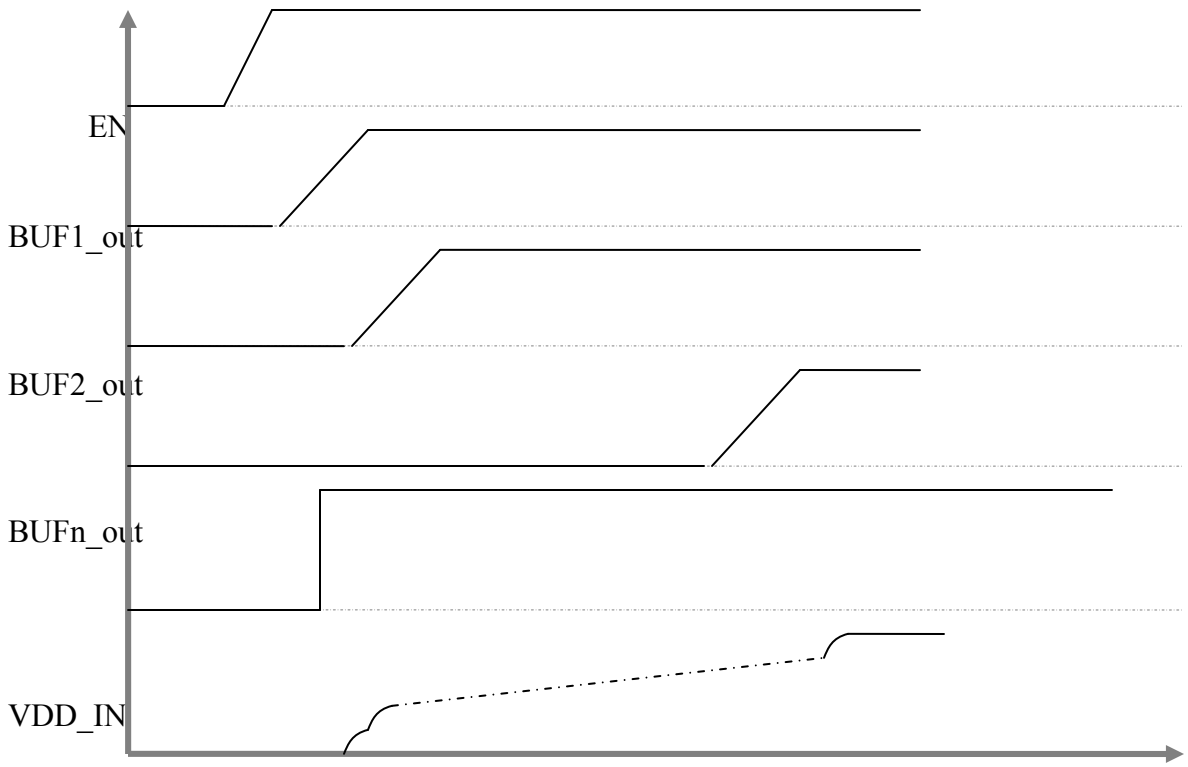


Fig 5.7 Slew Rate control waveforms for method2

Fig 5.8 shows the simulation result for different slew rate in turn on and off.

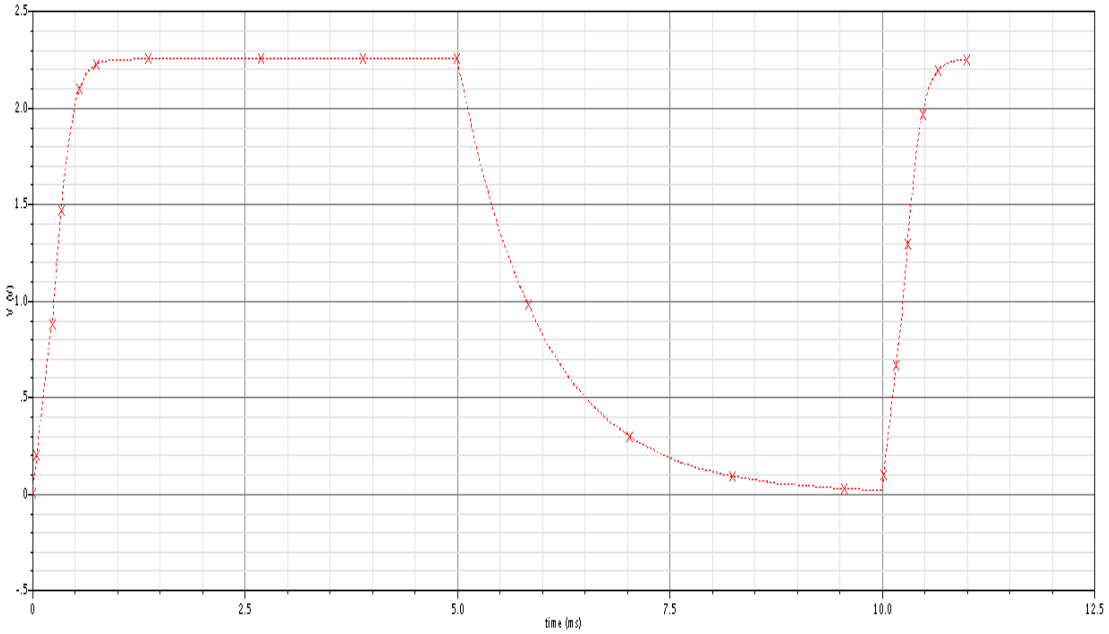


Fig 5.8 Different Slew rate for turn on and off.

Common Mode Feedback Design

An ideal balun was used as a common mode feed back block which needs to be designed in the future.

Fig. 5.9 shows the top level of the OTA design which uses ideal common mode feed back comprising an ideal balun and a voltage controlled current source as shown in Fig. 5.10.

Fig. 5.11 shows ideal balun schematic.

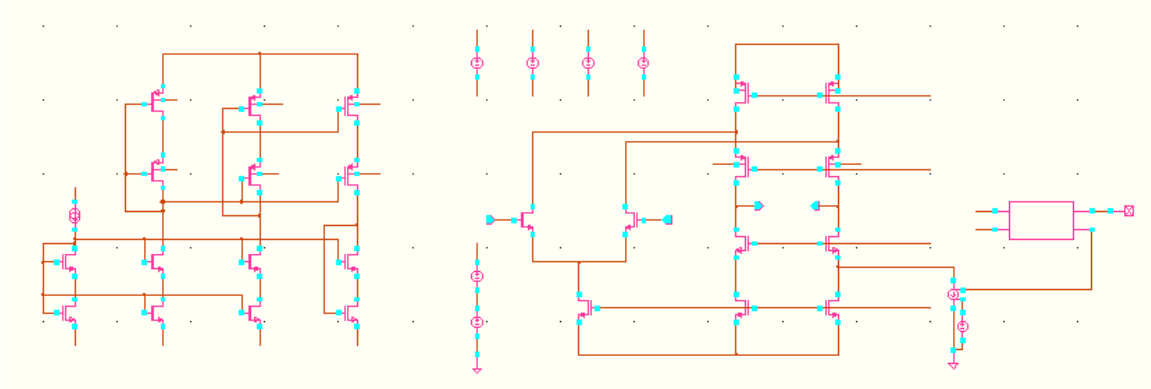


Fig 5.9 Top level OTA schematic

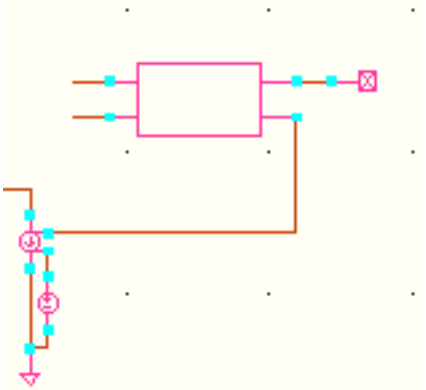


Fig 5.10 Common mode feed back implementation

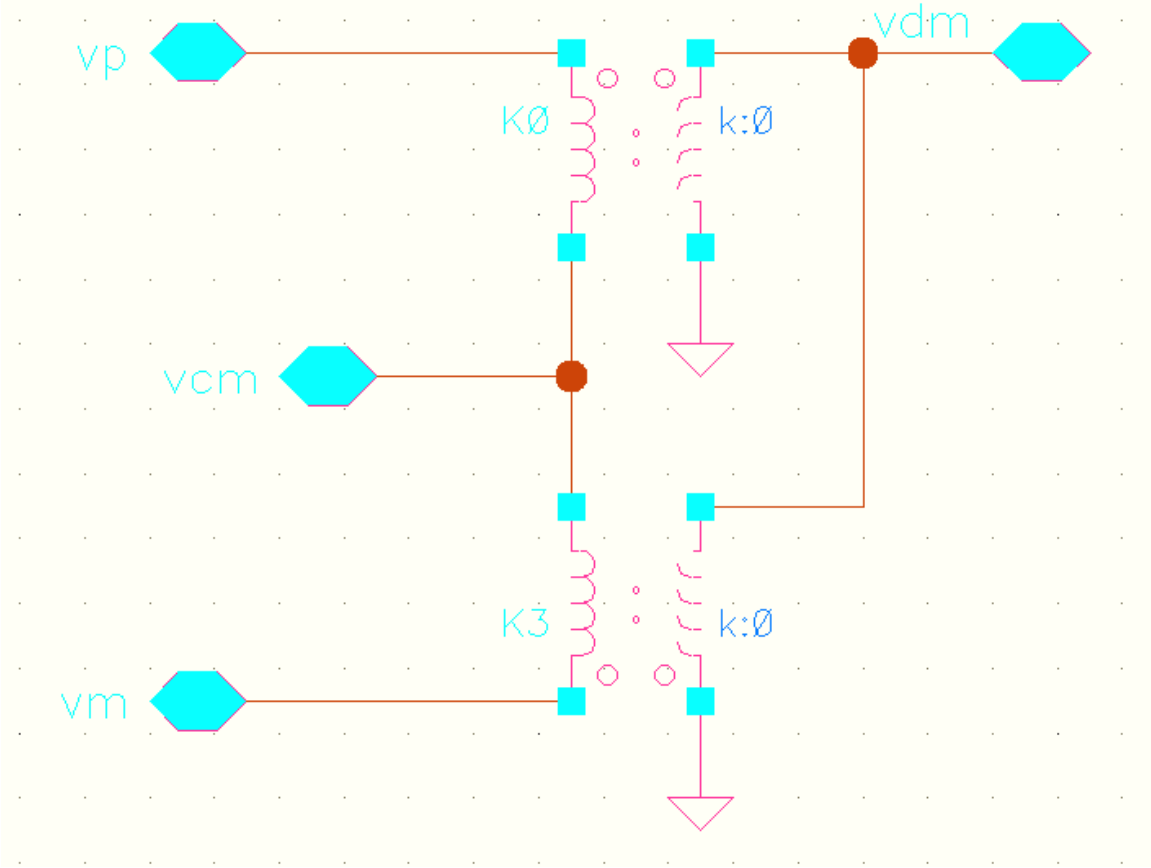


Fig 5.11 Ideal balun

Built in Self Test

A built-in self test scheme can be implemented to measure peak to peak ripple and average voltage using the following scheme [24]:

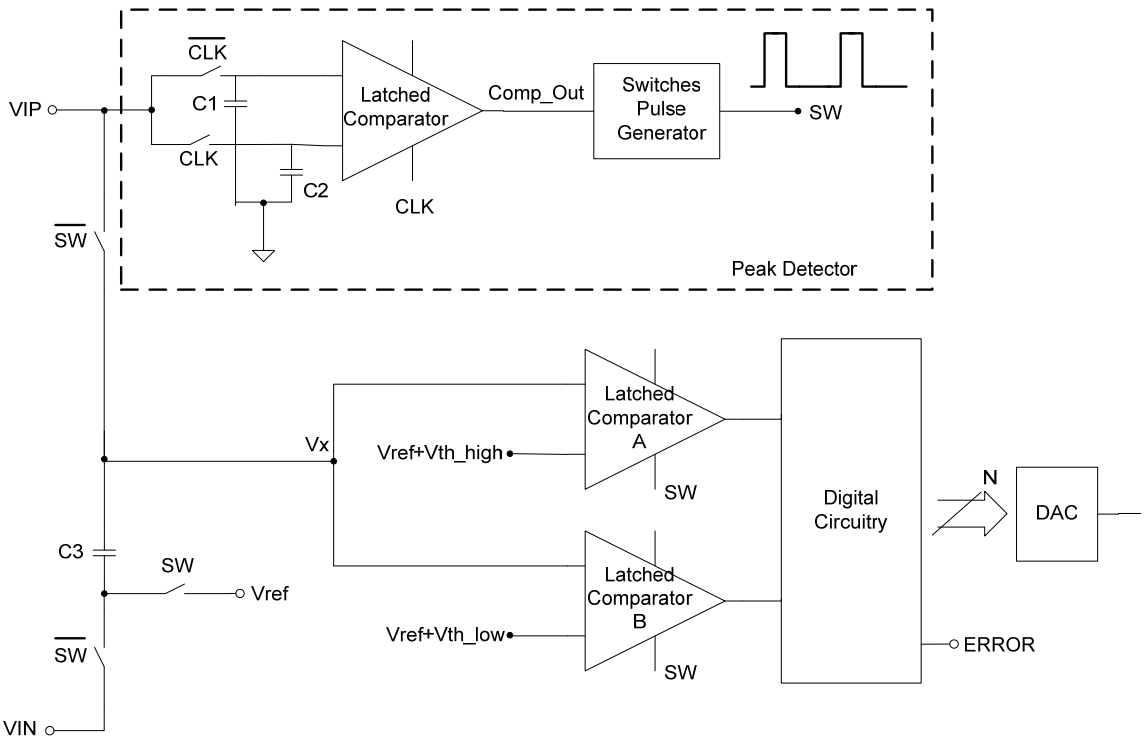


Fig. 5.12: Peak Detector

Peak detector detects peak and valley of the input signal. It generates a pulse whenever a peak voltage is detected. Peak detection is done in two steps:

1. Detection of occurrence of peak signal
2. Measurement of peak to peak voltage

The peak detection can be achieved by sampling the input signal with two matched capacitors ($C_1 = C_2$) at different instants of time (Φ_1 and Φ_2) and comparing the potential developed across the capacitors.

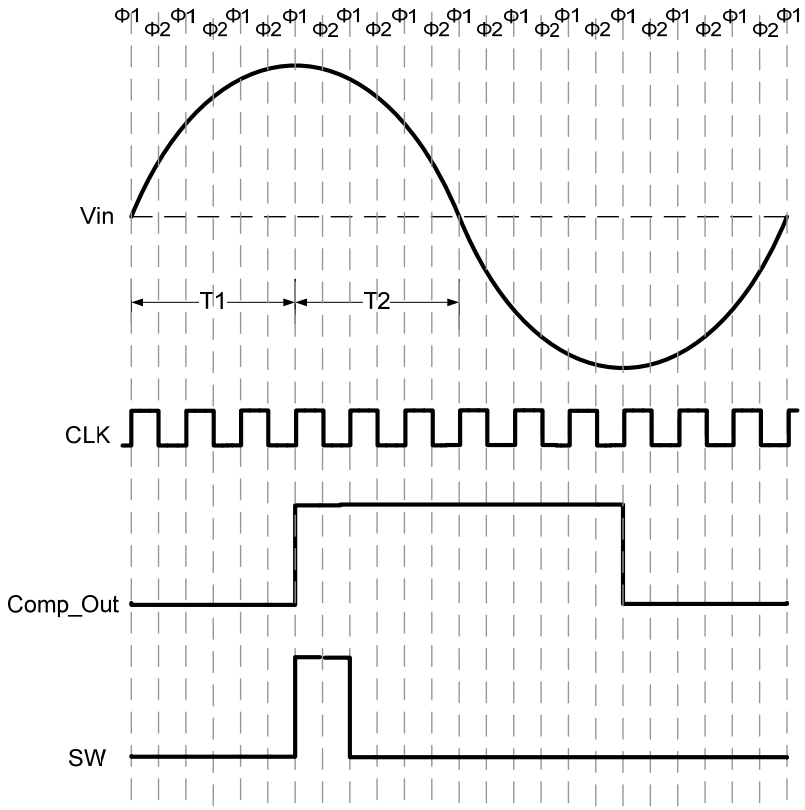


Fig: 5.13 Peak detector waveform

The input signal increases monotonically during the time frame T1, and it decreases monotonically during the time frame T2. The transition between these two time frames is the time when input signal reaches its peak value.

When capacitor C_2 is connected to input at the instant Φ_2, capacitor C_1 will hold the charge of the previous Φ_1 sample. Therefore, during time frame T1 when the input sinusoidal signal is monotonically increasing, capacitor C_2 will always have a higher potential than capacitor C_1, forcing the latched comparator to be low at its output. The latched comparator will continue to hold at low until the input sinusoidal signal reaches its peak value. During time frame T2 when the input sinusoidal signal is monotonically decreasing, capacitor C_2 will always have a lower potential than capacitor C_1, forcing the latched comparator to be high at its output.

A low to high transition at the latched comparator will enable the switched pulse generator to generate a pulse (high for a clock cycle) to isolate input signal from capacitor C_3 and compare the potential developed at V_x (eq 5.2) with the reference voltages.

$$V_X = V_{ref} + (V_{IP} - V_{IN}) = V_{ref} + \text{differential signal amplitude} \quad (5.2)$$

The switches pulse generator realized in Fig. 5.14 detects rising edge and output a pulse (continuously high for 1 clock cycle) for peak detection.

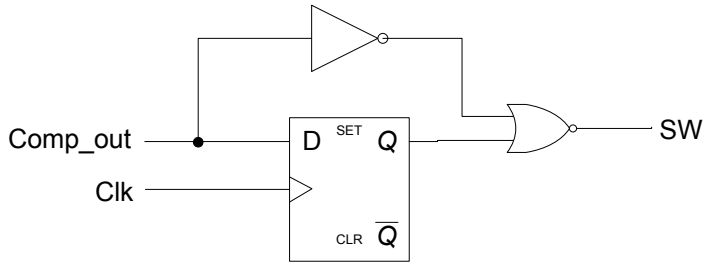


Fig 5.14 Pulse generator for peak detection

Similarly, the pulse generator can be modified to detect falling edge and output a pulse for valley detection, as shown in Fig. 5.15.

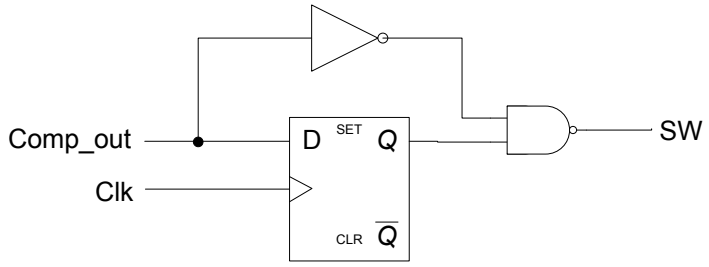


Fig 5.15 Pulse generator for valley detection

CHAPTER 6 SUMMARY

A novel, state of the art technique is presented in this thesis based on g_m tuning and common mode feedback, which is an alternative to the expensive PWM and PFM technique.

The new technique is a better solution from an area efficiency point of view which results in lower cost. Many mobile applications require a modulator to shift the baseband signal to a higher and quieter frequency for analog processing. Hence, for this kind of application PWM is not a suitable technique as it will introduce switching noise, which will be aliased to base band, resulting in poor system level SNR.

The specific research contributions of this work include:

1. Generating an out of phase current to the inductor current using an OTA and injecting it for the purpose of ripple rejection.
2. Identifying a suitable technique to compensate for component and input voltage variations as well as local and global device mismatches.
3. Compensating for temperature variations across the chip.

An interesting continuation of this work would be reliability testing of the presented techniques including current cancellation as well as implementation and testing of the g_m tuning mechanism. To first order, the principle of operation is sound, but still need to be demonstrated by manufacturing the circuit and testing it. Extensive verification was done using circuit simulators, however statistical analysis based on process variations was beyond the scope of this thesis.

APPENDIX I FOLDED CASCODE MATLAB MODEL

```
% folded cascade design
% author: Abhay Rai and Jeff Stone
% © Avago Technologies Inc
% all rights reserved
function [m1,m2, m3, m4, m5] = ...
  fc_new(cgg1_cs_plus_cf, cgg2_cltot, ...
  cgg4_cltot, Ln, Lp, gm3_gm1, gm4_gm1, ...
  gm5_gm1, tech)
%
% specifications


% normalization cap, based on noise
% estimate/allowance from filter analysis
spec.cn = 130e-15;


% feedback and loading estimates from table in
% Appendix I of project statement
spec.cf = 7.5*spec.cn;
spec.cs = 13*spec.cn;
spec.cl = 7.8*spec.cn;


% bandwidth requirement determined from full
```

```
% filter analysis in simulation with non-ideal
% OTA model
spec.fc = 200e6;
spec.wc = 2*pi*spec.fc;

spec.pm = 75*pi/180;
spec.es = .001;

% from the intrinsic gain charts, if gm/Id > 10,
% gm/gds = 20, .18 for the NMOS and PMOS will
% suffice

choices.Ln = Ln;
choices.Lp = Lp;

choices.gm3_gm1 = gm3_gm1;
choices.gm4_gm1 = gm4_gm1;
choices.gm5_gm1 = gm5_gm1;

% estimate m2 ft based on phase margin requirement
wpx = spec.wc*tan(spec.pm);
m2.ft = wpx*3 / (2*pi);
```

```
% look up cgd/cgg and cdd/cgg for our nfets and
% pfets
ncgd_cgg = interp1(tech.Lvector, ...
  tech.ncgd_cgg, choices.Ln);
pcgd_cgg = interp1(tech.Lvector, ...
  tech.pcgd_cgg, choices.Lp);
ncdd_cgg = interp1(tech.Lvector, ...
  tech.ncdd_cgg, choices.Ln);
pcdd_cgg = interp1(tech.Lvector, ...
  tech.pcdd_cgg, choices.Lp);

% estimate return ratio for amplifier in the
% filter circuit
beta = spec.cf / ((spec.cf + spec.cs) ...
  * (1 + cgg1_cs_plus_cf * (1 + pcgd_cgg)));

% estimate load capcitance that will be seen by
% amplifier
cltot = (spec.cl + (1 - beta)*spec.cf) / ...
  (1 - ncdd_cgg * cgg2_cltot - pcdd_cgg * ...
  cgg4_cltot);

% calculate gm for m1 - m5 based on either design
```

```
% specifications or chosen ratios

% m1 gm based on bandwidth requirement
m1.gm = spec.wc * cltot / beta;
% m2 gm based on pm requrement and a design "knob"
m2.gm = 2*pi*m2.ft*cgg2_cltot*cltot;

m3.gm = m1.gm * choices.gm3_gm1;
m4.gm = m1.gm * choices.gm4_gm1;
m5.gm = m1.gm * choices.gm5_gm1;

% cgg parameters based on design "knobs"
m1.cgg = cgg1_cs_plus_cf * (spec.cs + spec.cf);
m2.cgg = cgg2_cltot * cltot;

% m1 ft is fully determined at this point
m1.ft = m1.gm / (2*pi*m1.cgg);

% the rest of the device parameters are simple
% calcualtions or lookups
m1.gmid = lookup_gmid(tech, 'p', ...
  choices.Lp, m1.ft);
m2.gmid = lookup_gmid(tech, 'n', ...
```

```
  choices.Ln, m2.ft);


m1.id = m1.gm / m1.gmid;

m2.id = m2.gm / m2.gmid;


m1.idw = lookup_idw(tech, 'p', choices.Lp, ...

  m1.gmid);

m2.idw = lookup_idw(tech, 'n', choices.Ln, ...

  m2.gmid);


m1.W = m1.id / m1.idw;

m2.W = m2.id / m2.idw;


m3.id = m1.id + m2.id;

m4.id = m2.id;

m5.id = m2.id;


m3.gmid = m3.gm / m3.id;

m4.gmid = m4.gm / m4.id;

m5.gmid = m5.gm / m5.id;


m3.idw = lookup_idw(tech, 'n', choices.Ln, ...

  m3.gmid);
```

```
m4.idw = lookup_idw(tech, 'p', choices.Lp, ...
  m4.gmid);
m5.idw = lookup_idw(tech, 'p', choices.Lp, ...
  m5.gmid);

m3.ft = lookup_ft(tech, 'n', choices.Ln, m3.gmid);
m4.ft = lookup_ft(tech, 'p', choices.Lp, m4.gmid);
m5.ft = lookup_ft(tech, 'p', choices.Lp, m5.gmid);

m1.gds = m1.gm / lookup(choices.Lp, ...
  tech.Lvector, m1.ft, tech.pft, tech.pgmgds);
m2.gds = m2.gm / lookup(choices.Ln, ...
  tech.Lvector, m2.ft, tech.nft, tech.ngmgds);
m3.gds = m3.gm / lookup(choices.Ln, ...
tech.Lvector, m3.ft, tech.nft, tech.ngmgds);
m4.gds = m4.gm / lookup(choices.Lp, ...
  tech.Lvector, m4.ft, tech.pft, tech.pgmgds);
m5.gds = m5.gm / lookup(choices.Lp, ...
  tech.Lvector, m5.ft, tech.pft, tech.pgmgds);

m3.W = m3.id / m3.idw;
m4.W = m4.id / m4.idw;
m5.W = m5.id / m5.idw;
```

```
% calculate loop gain
T0 = beta * m1.gm / ((m1.gds + m3.gds) / ...
  (1 + m2.gm / m2.gds) + m5.gds / ...
  (1 + m4.gm / m4.gds));

% the following constraints, although currently
% commented out, were used during various searches
% of the design space to reject unreasonable or
% impractical designs.

%if m1.gmid > 20 || m2.gmid > 20 || ...
%  m3.gmid > 20 || m4.gmid > 20 || ...
%  m5.gmid > 20
%  m1.id = nan; m2.id = nan; m3.id = nan;
%  m4.id = nan; m5.id = nan;
%end

%if m1.W > 300e-6
%  m3.id = nan;
%end
```

APPENDIX II CADENCE SCHEMATICS

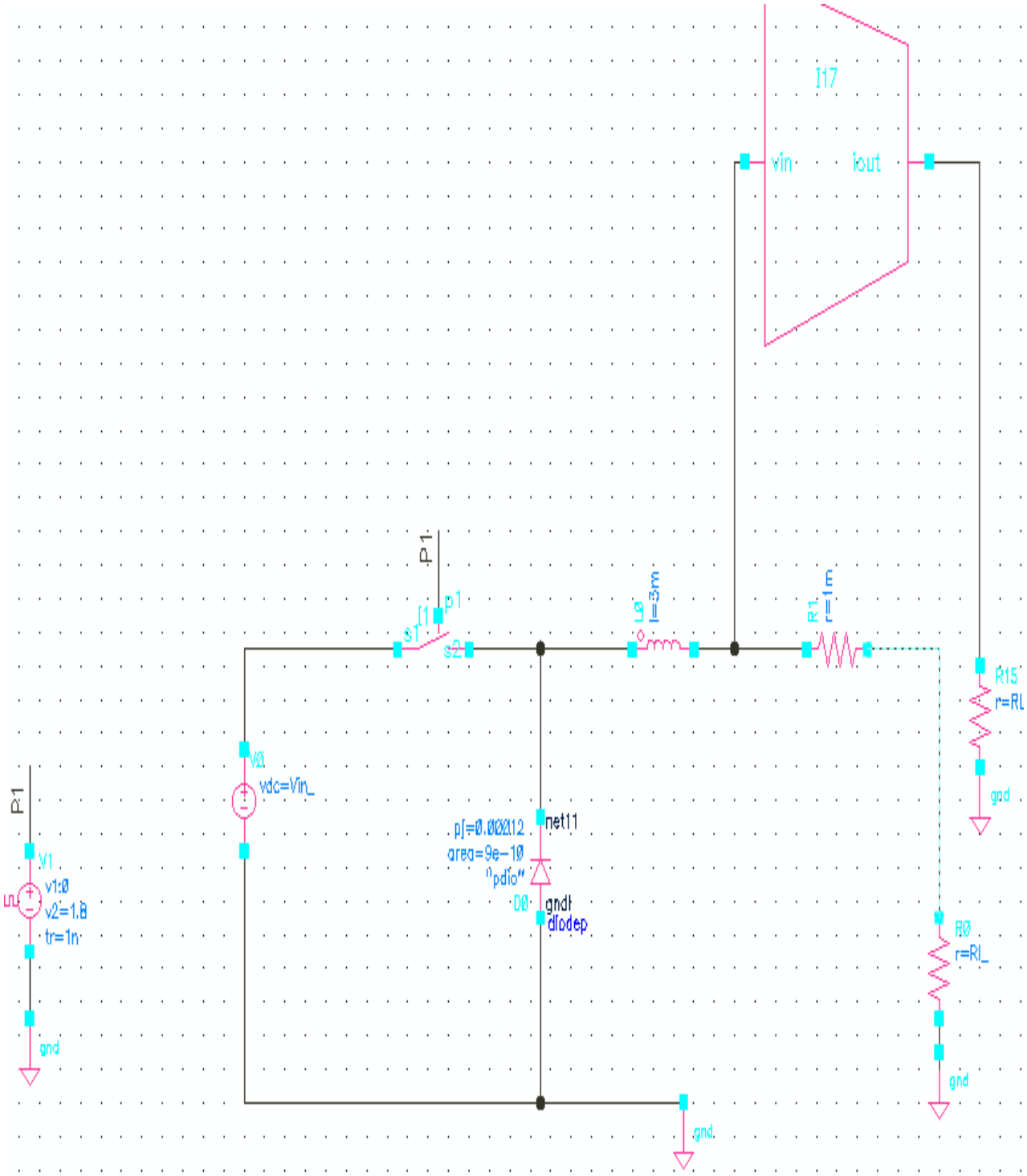


Fig A2.1 schematic of Fig3.1

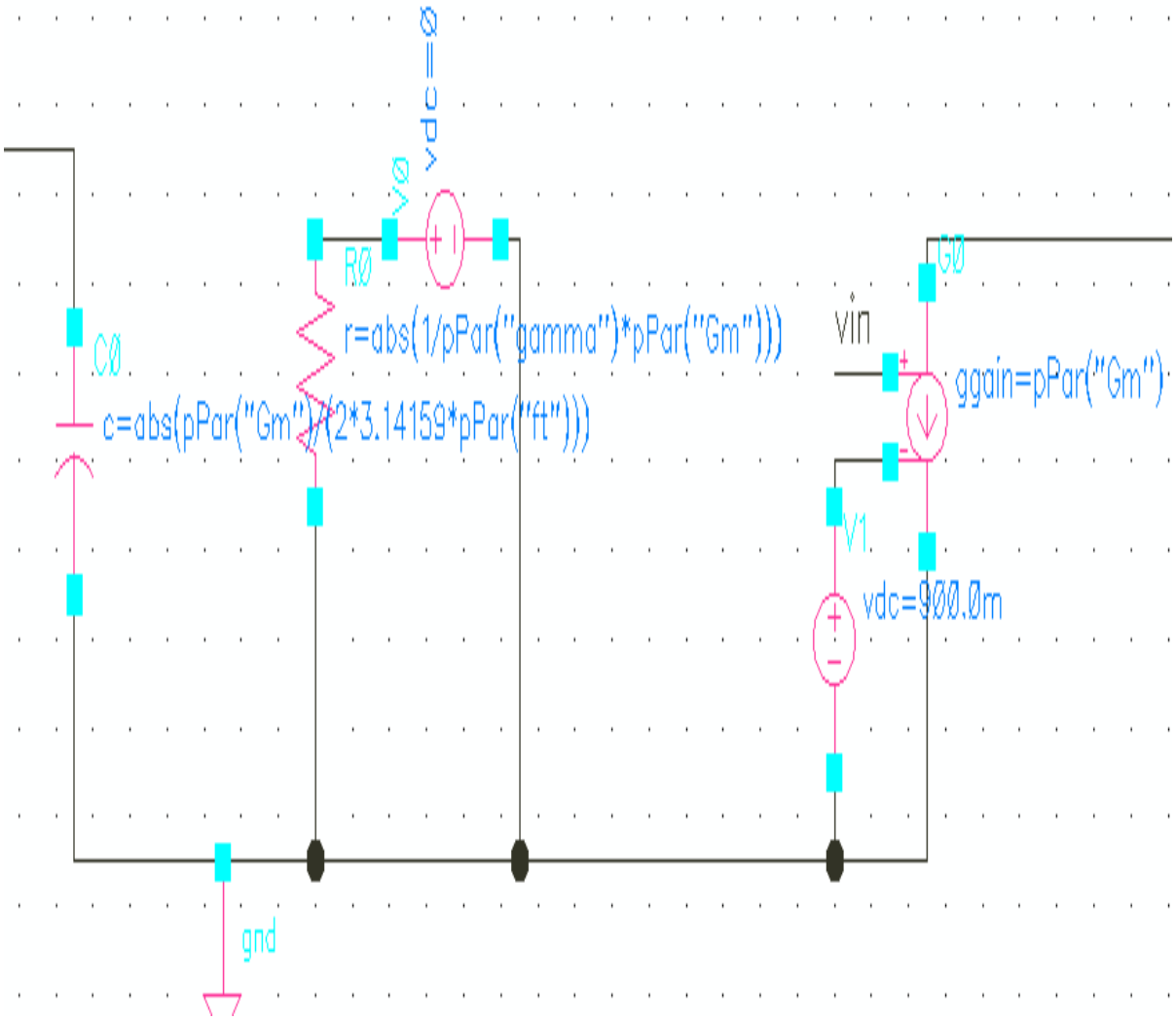
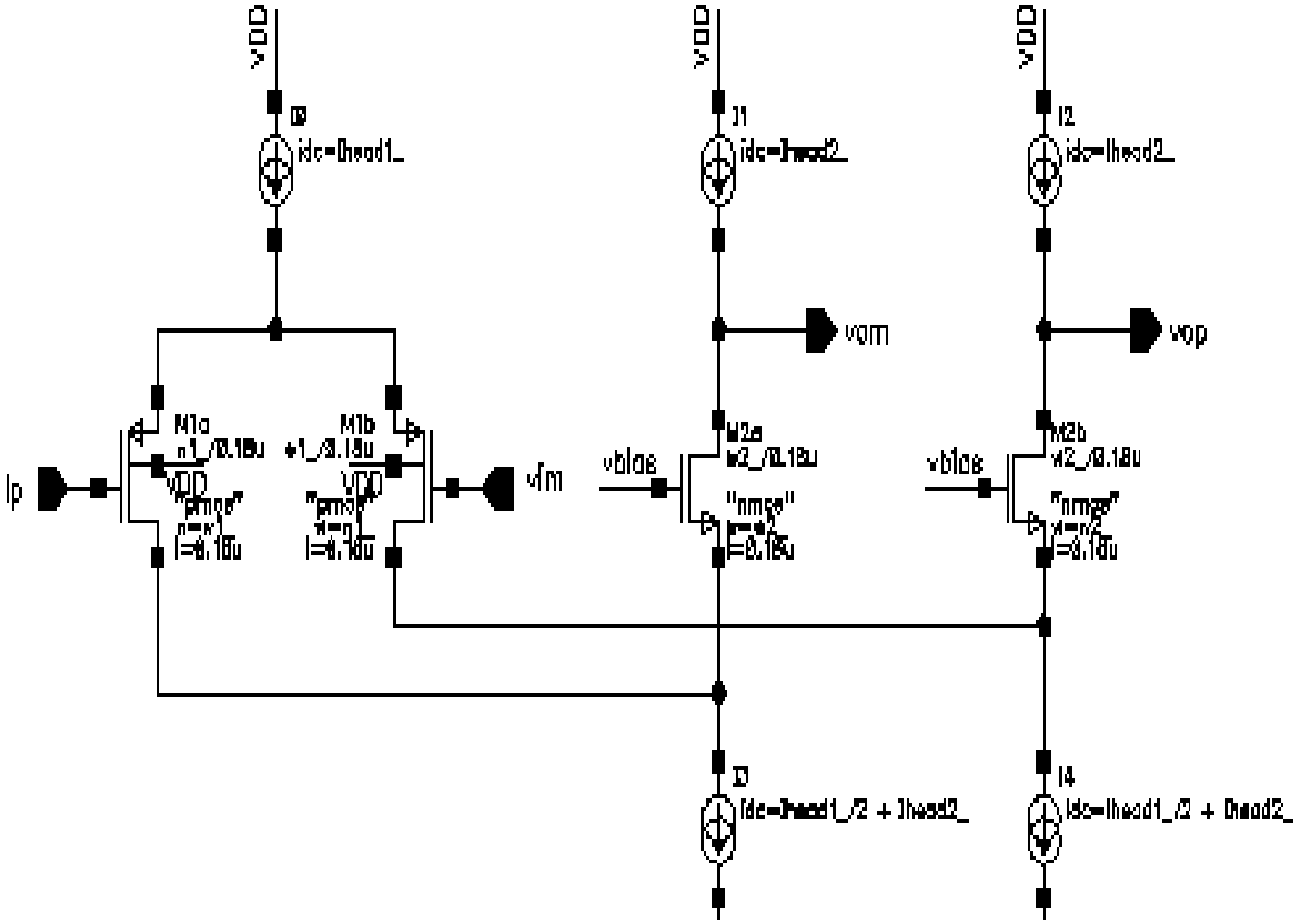


Fig A2.2 schematic of Fig 3.4



FigA2.3 schematic of Fig 4.1

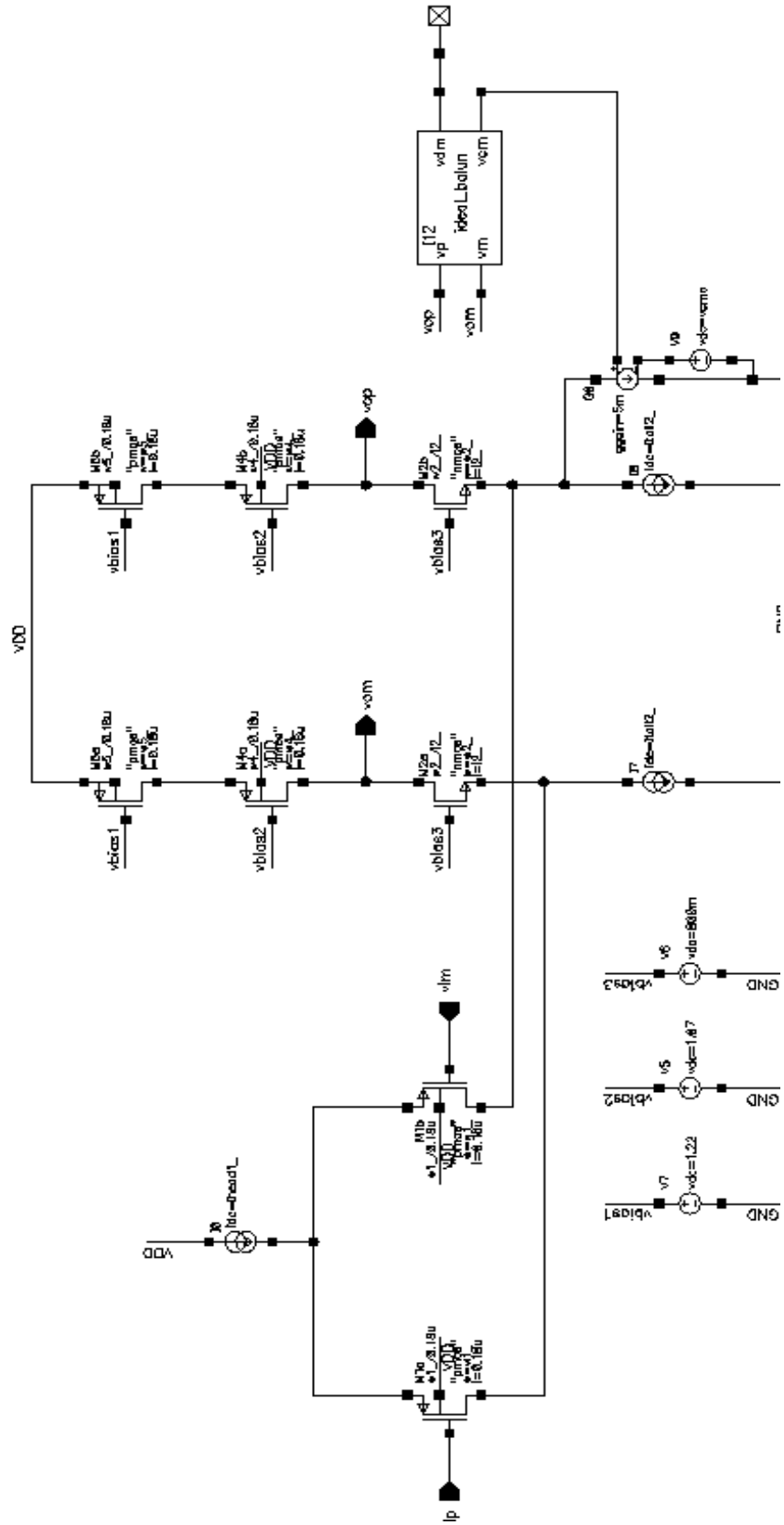


Fig A2.4 schematic of Fig 4.2

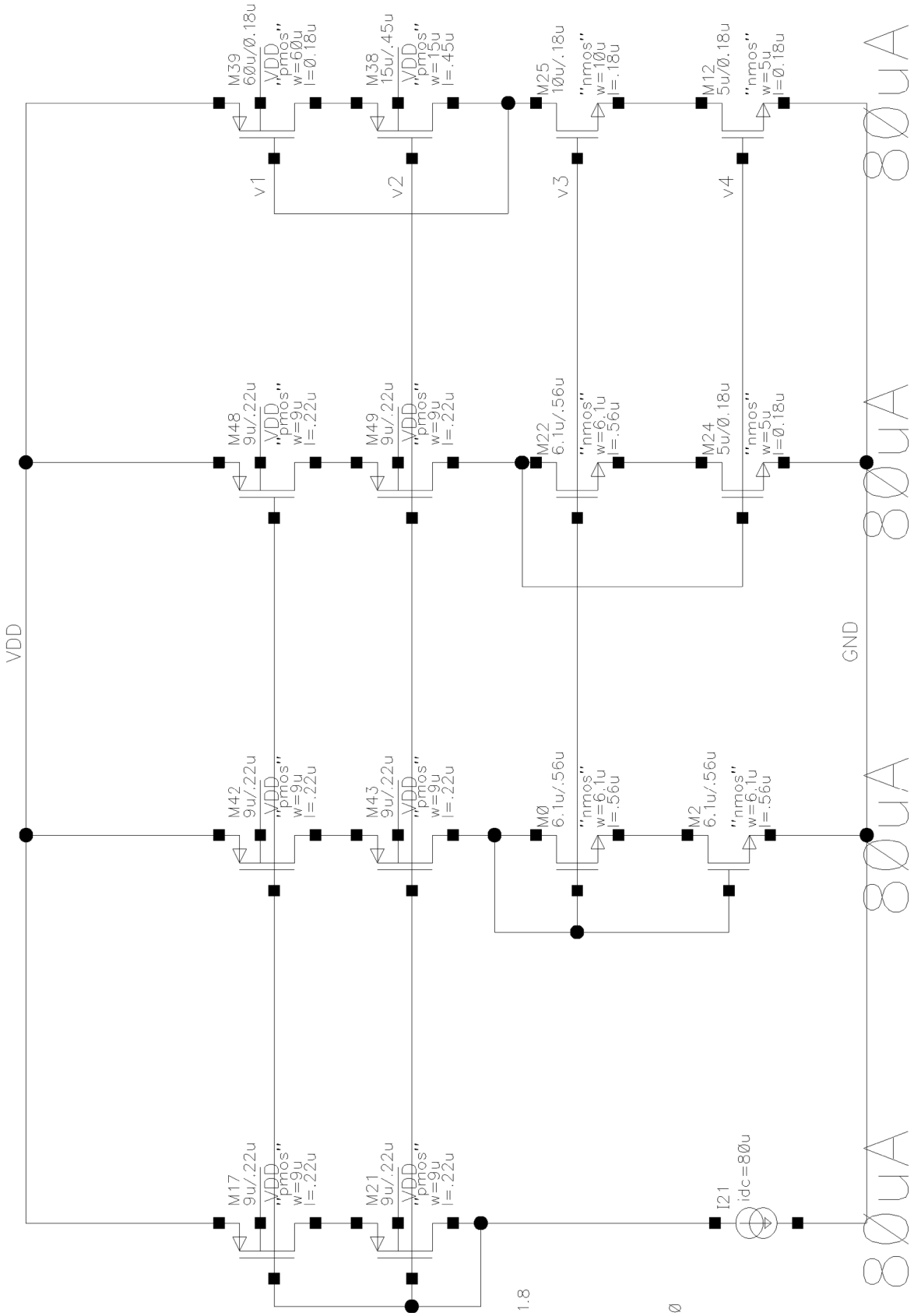


Fig A2.5 schematic of Fig 4.5

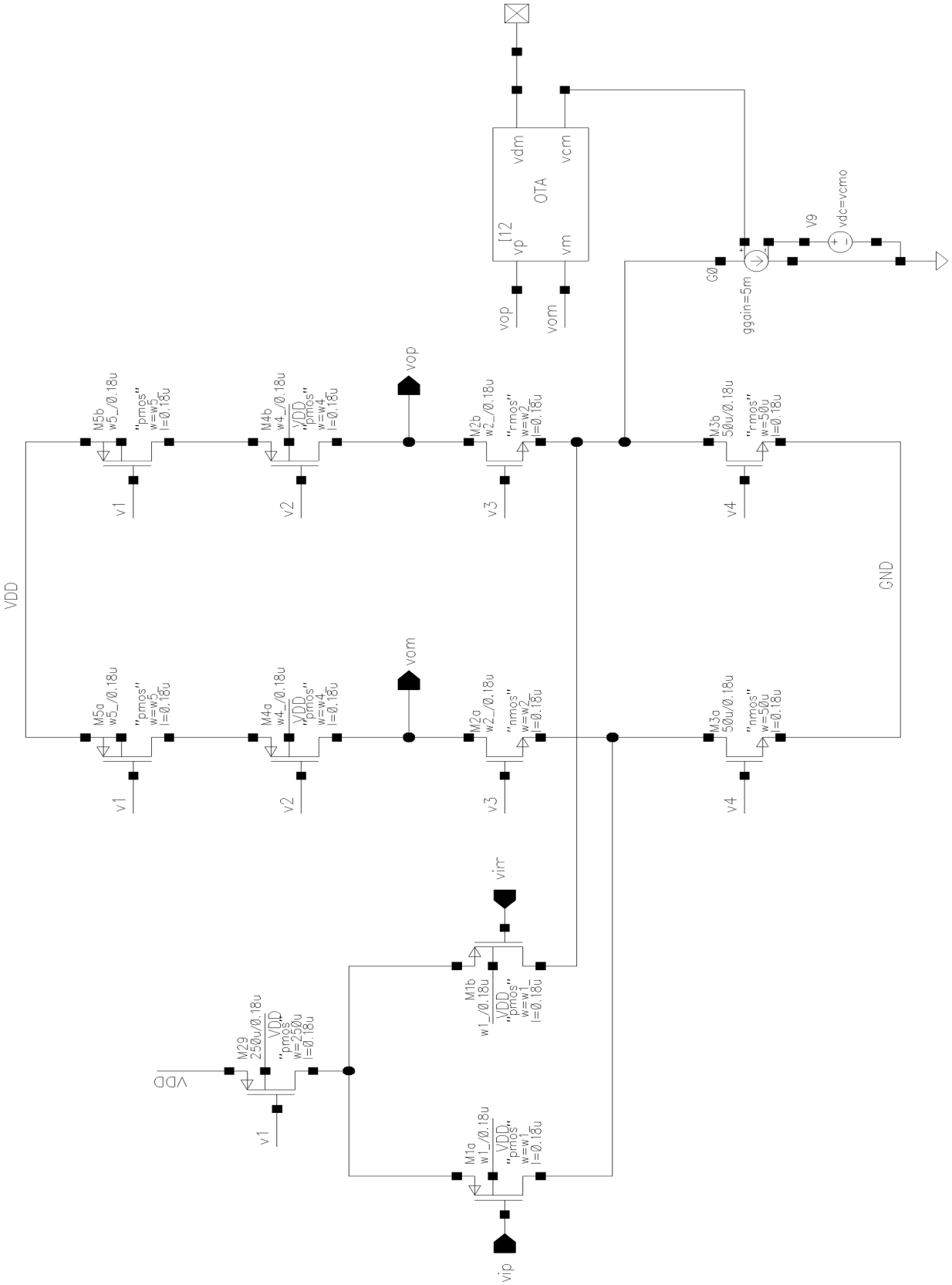


Fig A2.6 schematic of Fig 4.6

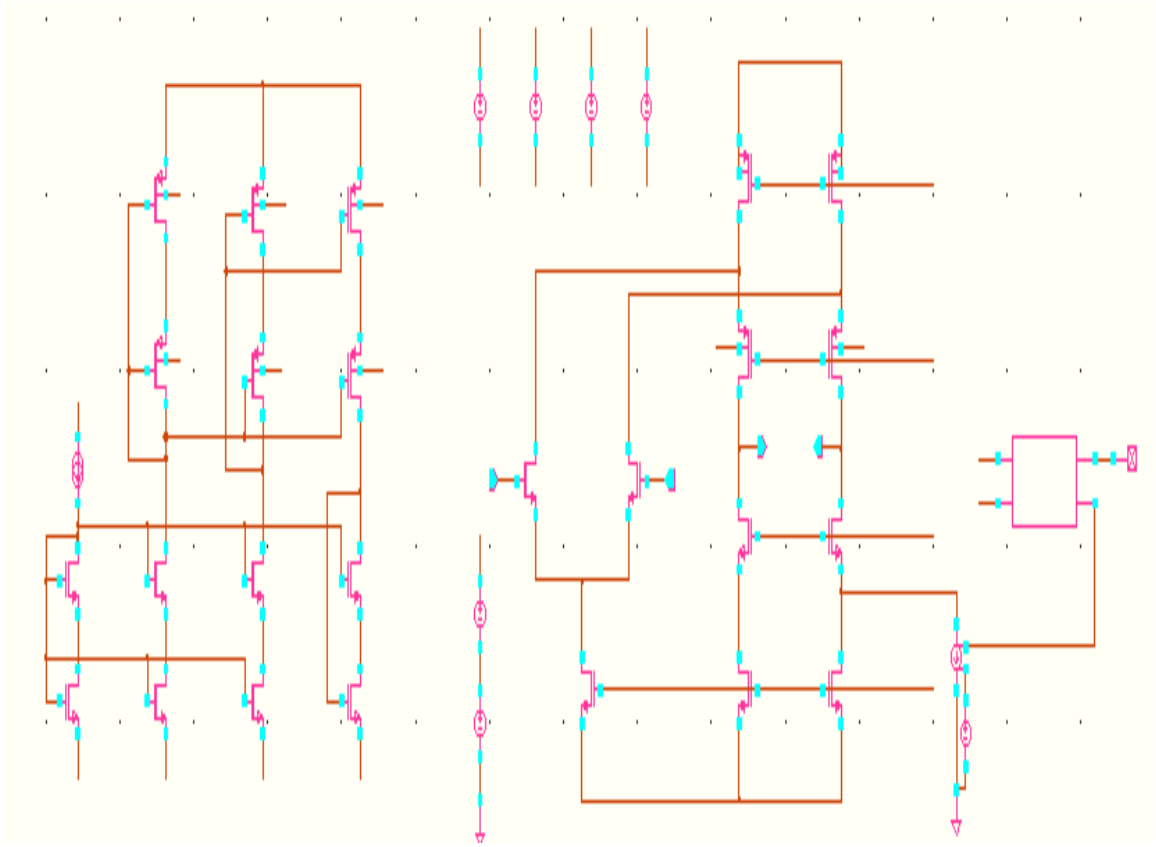


Fig A2.7 schematic of Fig 5.9

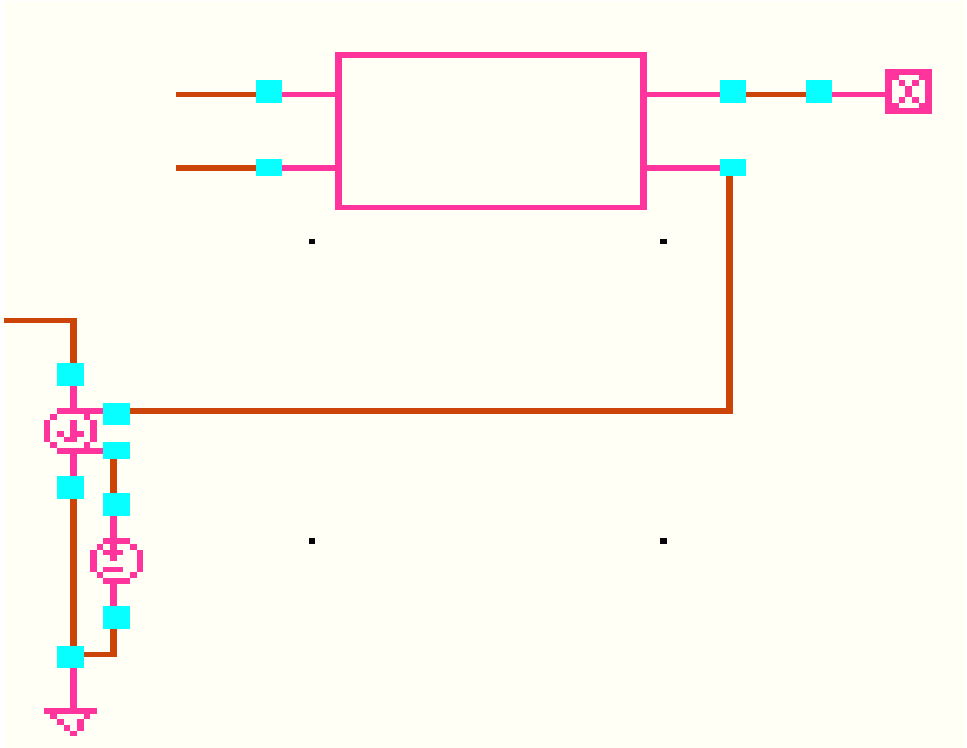
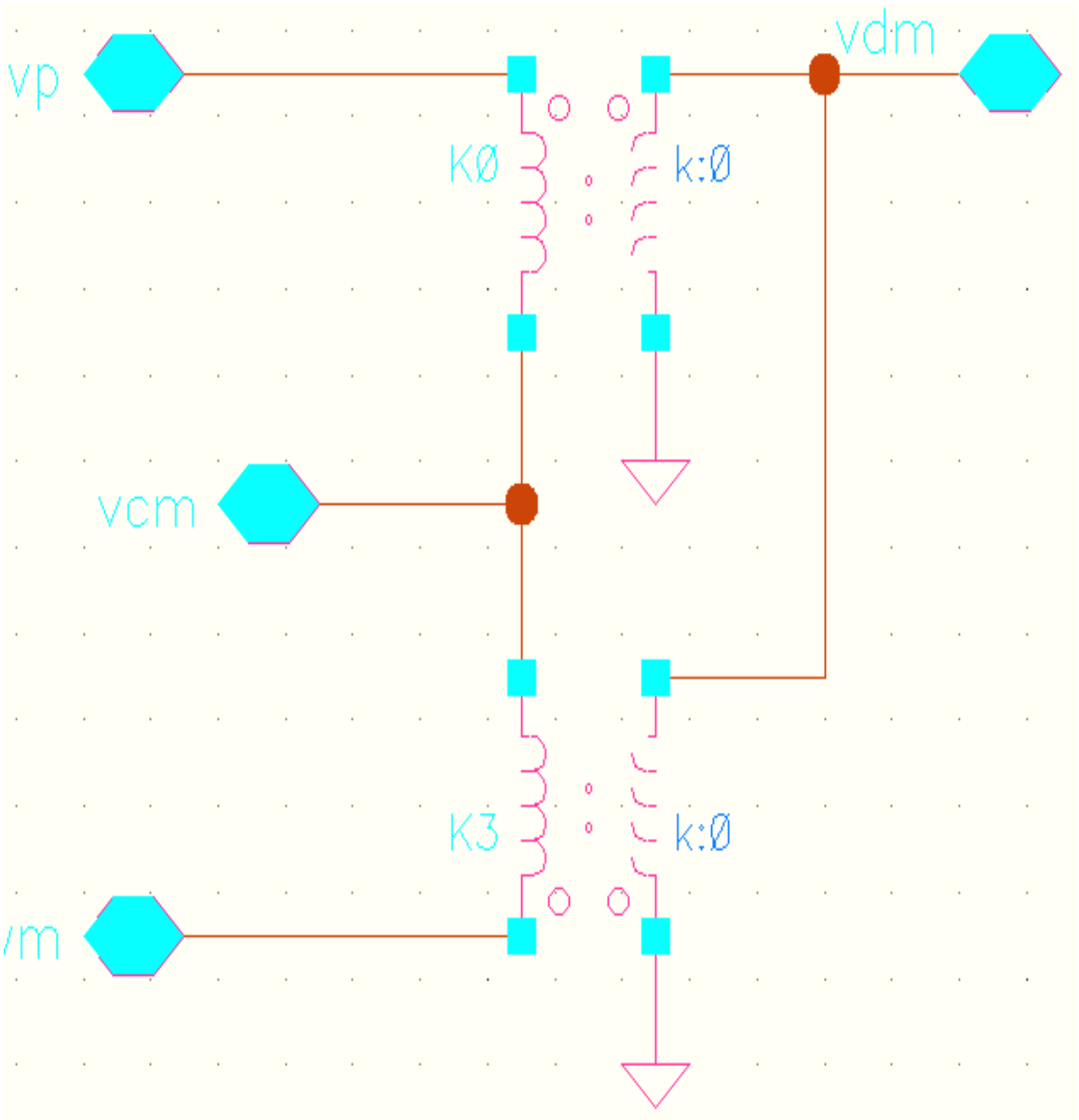


Fig A2.8 schematic of Fig 5.10



FigA2.9 schematic of Fig 5.11

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