Sensitivity Analysis of Critical Parameters in Board Test

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The authors analyze the main contributors to the quality and cost of complex boards. With manufacturing data from Hewlett-Packard boards, they use simulation models to derive the sensitivity of quality and cost to the solder defect rate, the functional defect rate, and test coverage. They also give a simple cost estimate of implementing IEEE 1149.1 boundary scan on ASICs. Their new yield model, which accounts for solder defect clustering, provides highly accurate yield predictions.

IN DESIGNING COMPLEX, high-performance boards, the designer must make several decisions: What surface-mount-technology (SMT) process should I use? What test escape rate is tolerable for custom ASICs (application-specific integrated circuits)? Is IEEE Std 1149.1 boundary scan necessary? What levels of board test coverage are best? If the designer fails to optimize these fundamental parameters of board manufacturing, test and repair costs will eat up the product's profits. On the other hand, if the designer minimizes incoming defect rates and carefully selects test coverage and isolation, test and repair costs decrease significantly.

To make these decisions, designers need quantitative data on how quality and cost vary with defect rates and test coverage for boards with different SMT complexities. To obtain such data, we have conducted an analysis of the sensitivity of manufacturing quality and cost to the solder defect rate, the component functional defect rate, and solder defect test coverage.

Board manufacturers typically measure quality in terms of first-pass yield (percentage of boards that pass their first test) for the various test steps. Accurate yield estimates facilitate prop-

er management of manufacturing cost, manufacturing-line capacity, materials procurement, and product delivery. Inaccurate yield predictions have adverse effects on both the manufacturing process and profit margins. An accurate yield model is particularly important during product design, when designers can still make trade-offs to improve manufacturability and testability.

Current board yield models are based on the Poisson distribution of defects.[1] This approach predicts yield accurately for simple assemblies. However, for complex SMT boards, in which the average number of defects per board can be greater than one, the Poisson model underestimates the yield due to the clustering of defects in the SMT production line. As a basis for our analysis, we introduce a new approach—a clustered yield model based on the negative binomial distribution.

Simulation methodology

For our analysis, we used the models implemented in the Manufacturing Test

Simulator,[2] a concurrent engineering tool for simulating test and repair aspects of boards and multichip modules from design concept through manufacturing release. The simulator helps designers select an assembly process, DFT features, test coverage, ASIC defect-level goals, and manufacturing quality and cost goals.

Defect mechanisms. Today's complex SMT boards contain through-hole, 50-, 25-, 20-, and 15-mil-pitch SMT packages. Many of their very high performance components are custom ASICs. The boards' operating frequency is on the order of 100 MHz. A typical board may have a 20-mil SMT joint next to a through-hole pin grid array or connector. In the manufacturing environment, boards are prone to two major classes of defects: SMT assembly and component functional. These defects cause multiple functional faults, which the test process must detect and isolate for repair.

Assembly defects originate during manufacturing. We categorize them as solder and workmanship defects. Solder defects are typically various forms of shorts and opens. SMT process developers characterize a solder joint's defect rate in ppm (parts per million).[3] Manufacturing facilities constantly monitor this rate. Workmanship defects are measured on a per-component basis. Examples are incorrect values, incorrect revision, reversed polarity, and misloads. Of the two categories of assembly defects, our analysis covers solder defects only.

ICs have a small but significant functional defect rate, which includes IC test escapes, chip-to-chip interactions, and some infant mortality. These defects typically cause delay and pattern-dependent faults. The functional defect rate of ASICs has been the target of much interest in the test community, and researchers are developing several new chip test techniques to reduce it.[4-6]

Fault probability model. Defect rates are a function of the assembly process and of individual components.[3,7] In our analysis, we considered the per-joint solder defect rate for each type of joint and the per-component functional defect rate.

The fault probability model we use computes the probability of at least one fault per component before test, assuming the binomial distribution of defects. It also bases the probability of at least one fault per component after test on the binomial distribution of defects. For solder defects, let Pfi be the probability of at least one fault per component before test, Pfo the probability of at least one fault per component after test, N the number of leads in the component, DR the per-joint solder defect rate for each type of joint, and TE the test efficiency. Then:

$$Pfi = 1 - [1 - DR]^N$$

$$Pfo = 1 - [1 - Pfi]^{(1 - TE)}$$

We use similar equations to obtain the functional fault probabilities.

Test methods. The test process usually targets a particular type of defect. For assembly defects, testing typically consists of in-circuit methods and IEEE 1149.1 boundary scan. For functional defects, testing usually takes the form of ROM-based self-test, system-level diagnostics, functional vectors, or board-level BIST (built-in self-test).

Our analysis assumes the two-step test process depicted in Figure 1. The assembly test step gives high solder defect coverage and isolation. The functional test gives very high fault coverage for both solder and functional defects, but defect isolation is difficult and usually technician intensive.

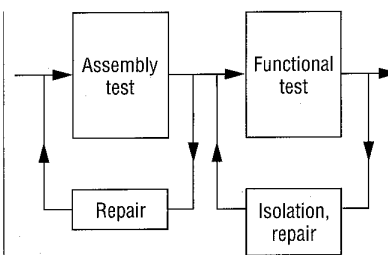**Cost models.** Each test step incurs costs for the operator, capital equipment, fault isolation, and repair. We estimate a rate in $/hour for each resource necessary for testing a board. The simulation then models the amount of time required to test and repair boards, thus obtaining the test cost.

Figure 1. Test process.

Yield models. In the manufacturing process of complex SMT assemblies, not all defects are independent of each other. Solder defects tend to be clustered, especially for finer pitch components. In contrast, we can model workmanship and functional defects adequately without considering clustering.

We calculate yields separately for clustered assembly defects, nonclustered assembly defects, and functional defects. The overall yield is the product of the individual yields:

$$Y = Ycl * Ync * Yfct$$

where Y is overall yield after test, Ycl is yield from clustered defects, Ync is yield from nonclustered defects, and $Yfct$ is yield from functional defects.

After characterizing the fault probability, we can estimate the average number of defects per board. However, we must include the test step's effectiveness if we are interested in yield after test. We compute the average number of defects per board, Do, after test for each type of defect, as follows:

$$Do = \sum Pf * TE$$

where the sum is over all components, and Pf is a component's incoming fault

Table 1. Board complexity.

Board	No. of solder joints
A	4,239
B	6,832
C	11,490

Table 2. Yield model results.

Board	Actual yield	Poisson yield	Clustered yield
A	a	50% of a	98% of a
B	b	44% of b	105% of b
C	c	10% of c	98% of c

probability.

The nonclustered yield, Ync, is based on the Poisson probability distribution function. We use this yield model for functional defects and nonsolder assembly defects:

$$Ync = e^{-Do}$$

Clustered yield model. We developed the clustered yield model on the premise that solder defects are clustered on complex SMT boards. We validated this premise by examining data from production boards at HP. We found that yield predictions based on the Poisson distribution were as much as 10 times under actual yield.

Researchers have done much work on the modeling of clustered phenomena. Stapper and others have used the negative binomial distribution to predict clustered yield of large integrated circuits.[8,9] However, their methods are not directly applicable to SMT assemblies because an SMT board's fault spectrum is not easy to model in terms of defect density.

Our original approach to the clustered yield model was to look at clustering for each type of solder joint and

also in a batch of boards. However, once we examined the data, we found that it is sufficient to model clustering for all solder joint types on a per-board basis. This simplifies the model significantly, since only one clustering factor must be determined. An earlier work details the derivation of this model.[10]

The following equation gives the clustered yield model, where α is the clustering factor:

$$Ycl = [1 + (Do/\alpha)]^{-\alpha}$$

Before we can apply this yield model, we must estimate parameter α, which determines the shape of the yield curve. We base the estimated value of α on the distribution of defects per board. For large values of α (>1), the negative binomial model will approximate the Poisson model; we use small values of α when clustering is severe. We would expect the clustering factor to remain constant for a particular SMT process as long as the boards have similar complexities, and our initial validation confirms this expectation. Our earlier article describes the estimation procedure.[10]

Boards used in validation. To validate our simulation methodology, we used data from three high-volume, complex SMT boards built at Hewlett-Packard. The three boards, listed in Table 1, have through-hole, 50-mil, 25-mil, and 20-mil SMT components. The boards contain several custom VLSI designs.

Clustered yield model validation. We used the clustered model to predict yield for the boards in Table 1. Table 2 gives the results. We present results as variables rather than specific yields because we are interested in the model's accuracy, not data from a particular SMT process. In Table 2, actual yield is the manufacturing line's measured yield for a four-month period. Poisson yield is the yield based on the nonclus-

tered Poisson model. Clustered yield is the yield we calculated with the new model. The clustered yield "98% of a" shown in the table means the value of the actual yield a minus 2% of a. Thus, for example, if board A's actual yield were 80%, the Poisson model would predict 40% and the clustered model would predict 78%.

We obtained the clustered yield values in Table 2 with $\alpha = 0.4$. In the average α range of 0.35 to 0.45, the clustered model predicts all yields correctly. Boards A, B, and C span the typical yield spectrum for the SMT process used because of the difference in their numbers of solder joints. However, they are similar in complexity and density. It is very encouraging that the clustering was predictable across this variety of board complexity. Board C is the largest board, with the largest average number of defects per board. As one would expect, the Poisson model significantly underestimates the yield, whereas the clustered model excels.

Sensitivity analysis

For the sensitivity analysis, we used the validated simulation models and varied the parameters of interest on the simulator.

Our analysis covers three main areas: 1) yield and test costs versus the solder defect rate, 2) yield and test costs versus the functional defect rate, and 3) test cost sensitivity to assembly test coverage, using IEEE 1149.1 techniques in the custom ASICs. We present results in relative terms to make them general rather than specific to HP's manufacturing line.

Solder defects. To analyze solder defects, we set the solder defect rate at an industry average of 50 ppm per joint and then scaled this rate by multiplying it by factors in the range 0 to 100. Figure 2a shows the relationship of assembly test yield to the scaled solder defect rate through the whole range for the three
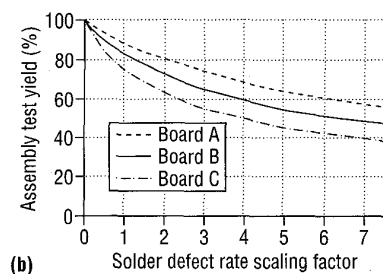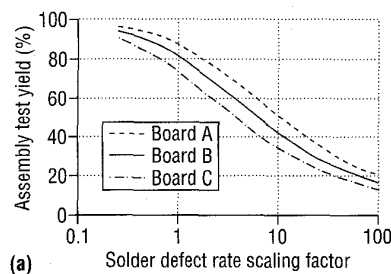
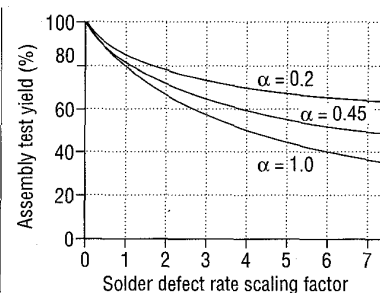**Figure 2.** Yield versus solder defect rate (a); detail (b).

Figure 3. Yield versus solder defect rate for board B with various clustering factors.

boards. Figure 2b expands the view in the low-defect-rate region.

Figure 2b shows that assembly test yield is very sensitive to the solder defect rate. For board B, doubling the solder defect rate from the nominal point implies a roughly 10% loss in yield.

Figure 3 also shows the low range of the solder defect rate, but only for board B, and plots the curves of different values of α. As the average number of defects per board grows, the clustered model accounts for the clustering and corrects the overpessimistic yield predictions. The yield is very sensitive to clustering, so good characterization of the SMT process is necessary to obtain the correct α.

Figure 4a depicts the relationship between the solder defect rate and test cost increase. Test cost is the total cost of testing and repairing the board, including isolation time. Figure 4b shows the low end of the defect rate.

An increase of solder defects implies that the number of solder defects not detected by the assembly test also increases. Covering these defects in the functional test step is very costly because isolating the defect is difficult and technician intensive. This explains the high sensitivity of cost to the solder defect rate.

Functional defects. Figure 5a shows the relationship of functional test yield to the scaled component functional de-
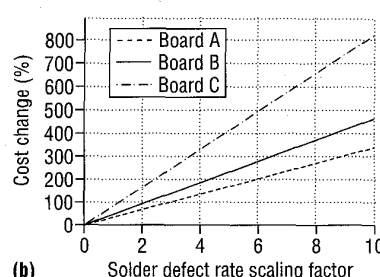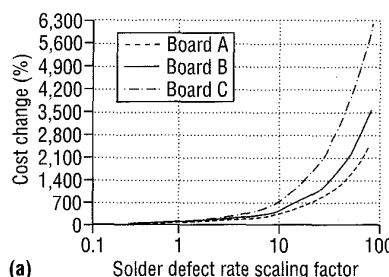

Figure 4. Cost versus solder defect rate (a); detail (b).
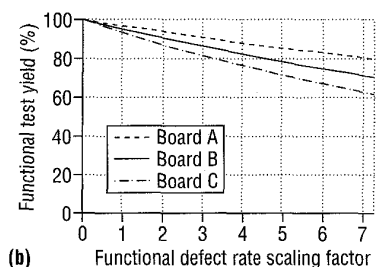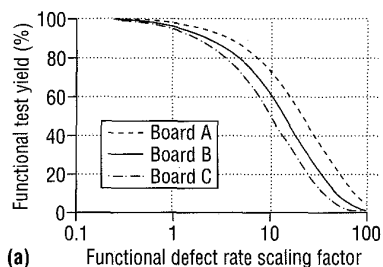

Figure 5. Yield versus functional defect rate (a); detail (b).

fect rate for the three boards. We set the component defect rate at an average value for each type of component at the running rates in the board's history.[7] We scaled this rate by multiplying by factors in the range 0 to 100. Figure 5b expands the low-defect-rate region.

The sensitivity of functional test yield to the component functional defect rate is not as high as to the solder defect rate, and surprisingly, the industry average

numbers contribute to a fairly small yield loss. This suggests that beyond an optimum point, there is a diminishing return on investment in chip-level testability and test coverage to reduce functional defect levels.

Figures 6a and 6b depict the relationship between the functional defect rate and the increase in total test cost. This increase reflects the fact that most functional fault isolation is technician
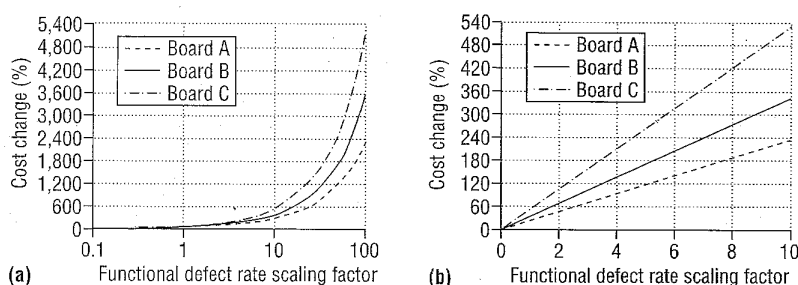
Figure 6. Cost versus functional defect rate (a); detail (b).
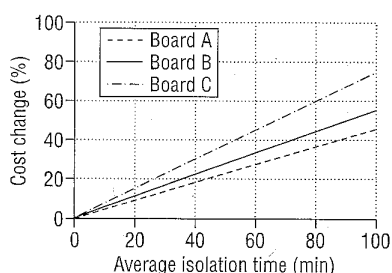

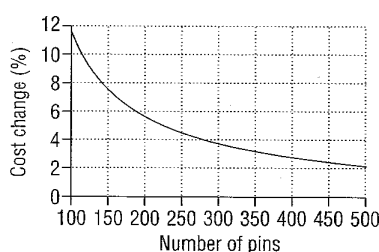Figure 7. Cost versus functional isolation time.

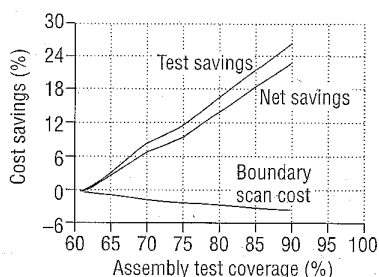Figure 8. Chip cost versus number of pins for IEEE 1149.1 implementation.

Figure 9. Test cost versus assembly defect coverage: board B.

Figure 10. Test cost versus assembly defect coverage with increased defect rate and decreased labor rate.

driven. We expect that BIST techniques with good isolation capabilities would significantly reduce costs.

Figure 7 shows the relationship between average technician-driven isolation time and changes in cost. This analysis assumes that the technician rate is the same as other test resource rates. Actually, technicians are more expensive, so we should expect an even greater cost increase. We conclude that
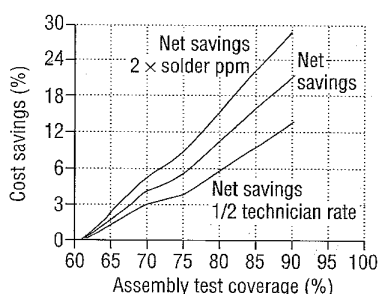
although functional test coverage is at acceptable levels, we still need to invest in automatic defect isolation techniques for faults detected at the functional test step.

Test coverage. The next parameter we considered was test coverage for solder defects. We chose solder defect test coverage because it has an incremental

development cost. In contrast, one can always obtain functional coverage by diagnostics, which are necessary anyway for system test and field test.

To make this analysis interesting, we assumed that all assembly test coverage in custom ASICs would be obtained via IEEE 1149.1 boundary scan. We also assumed that the cost of implementing the standard on chips is comparable to the cost of developing vectors, and thus they offset each other.[11] So the cost of implementing boundary scan is limited to the ASIC's increased area and pin count. We subtract this incremental chip cost from the test cost savings due to better solder defect coverage and isolation.

IEEE 1149.1 implementation cost. Some assumptions are necessary to estimate the added chip cost caused by IEEE 1149.1 implementation; results can vary and are open to debate.[10] Figure 8 graphs an ASIC's cost change due to IEEE 1149.1 implementation. Although the magnitude of change may vary from design to design, this data illustrates the cost trade-off analysis.

Assembly defect test coverage. To analyze the relation of total test cost to solder defect coverage, we selected board B. Board B contains nine custom ASICs that account for about 30% of the board's solder joints. Without testing any of these ASICs, we started at a coverage level of about 60%.

We then added IEEE 1149.1 boundary scan to the ASICs one at a time and simulated the net test cost savings. Figure 9 depicts the added boundary scan cost, the overall test cost savings, and the net cost savings. For this analysis we assumed that the technician labor rate is two times the rate for other resources such as test and repair operators. The slight knee in the curve is due to the variable coverage increment for different ASIC packages and their respective solder defect rates.

The net savings depends on both the

solder defect and the technician labor rates, since solder defects not covered in the assembly test will be detected by the functional test and must be isolated by a technician in most cases. Figure 10 shows the original net savings shown in Figure 9, along with the net savings when the solder defect rate is two times higher and when the technician labor rate is cut in half.

OUR SENSITIVITY ANALYSIS for the main quality parameters in dense, high-performance SMT boards shows that quality and cost are most sensitive to the solder defect rate. Therefore, selecting appropriate SMT processes and design techniques is critical to reducing costs and increasing quality.

Sensitivity to the component functional defect rate is not as strong as we expected, showing that contrary to intuition, there is an optimum point beyond which the return from improving chip-level test coverage diminishes. However, board manufacturing cost is not the only factor to consider in deciding when to stop investing in reduced ASIC defect rates. We must also consider the cost incurred by faults that escape board test and go on to system test and beyond.

Assembly defect test coverage, as we expected, greatly influences overall cost, primarily due to the superior isolation methods of boundary scan compared to functional test. Our analysis of assembly test coverage versus overall test cost (Figure 9) demonstrated a large ROI from using IEEE 1149.1 boundary scan techniques. Automatic defect isolation techniques for faults detected at the functional test stage will also give a significant payback in product profit margins.

Our clustered yield model predicts yield after test, accurately modeling the clustering of solder defects. Validation with HP manufacturing data shows that the model's yield predictions are excellent. If SMT assemblies are not very com-

plex, Poisson yield modeling is sufficient, but for complex boards clustering is a dominant factor. Thus, we encourage further research in this area. ◁D&T▷

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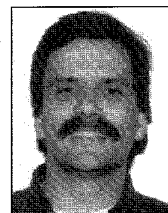
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