

THESIS

DESIGN, FABRICATION, AND TESTING OF A DATA ACQUISITION AND CONTROL
SYSTEM FOR AN INTERNALLY-CALIBRATED WIDE-BAND MICROWAVE AIRBORNE
RADIOMETER

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ABSTRACT

DESIGN, FABRICATION, AND TESTING OF A DATA ACQUISITION AND CONTROL SYSTEM FOR AN INTERNALLY-CALIBRATED WIDE-BAND MICROWAVE AIRBORNE RADIOMETER

The National Aeronautics and Space Administration (NASA)'s Earth Science Technology Office (ESTO) administers the Instrument Incubator Program (IIP), providing periodic opportunities for the development of ground-based and airborne instruments to reduce the risk, cost and schedule to accomplish future Earth Science satellite missions. The IIP-10 project proposed in 2010 and led by PI S. Reising at Colorado State University focuses on the development of an internally-calibrated, wide-band airborne radiometer to reduce risks associated with wet-path delay correction for the Surface Water and Ocean Topography (SWOT) mission. This airborne radiometer includes microwave channels at 18.7, 23.8, and 34.0 GHz at both H and V polarizations; millimeter-wave window channels at 90.0, 130.0, 168.0 GHz; and temperature and water vapor sounding channels adjacent to the 118 and 183 GHz absorption lines, respectively. The microwave, millimeter-wave window and millimeter-wave sounding channels consist of 6, 3 and 16 channels, respectively, for a total of 25 channels in the airborne radiometer. Since this instrument is a prototype for space flight, a great deal of effort has been devoted to minimizing the mass, size and power consumption of the radiometer's front-end.

Similar design goals have been implemented to minimize the mass, size and power consumption of the radiometer back-end, which performs the data acquisition and control functions for the entire instrument. The signals output from all 25 radiometer channels are conditioned, integrated and digitized on the analog back-end boards. The radiometer system is controlled by a Field Programmable Gate Array (FPGA) and a buffer board. Each analog back-end board can condition and simultaneously sample four signals, thereby performing analog-to-digital conversion. The digital back-end consists of the buffer board and FPGA, which control and accept data from all seven analog back-end boards required to sample all 25 radiometer channels. The digital back-end also controls the radiometer front-end calibration (also called “Dicke”) switching and the motor used to perform cross-track scanning and black body target calibration of the airborne radiometer instrument.

The design, fabrication, and test results of the data acquisition and control system are discussed in depth. First, a system analysis determines general requirements for the airborne radiometer back-end. In the context of these requirements, the design and function of each component are described, as well as its relationship to the other components in the radiometer back-end. The hardware and software developed as part of this radiometer back-end are described. Finally, the back-end testing is described, and the results of these tests are discussed.

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1. Introduction

The purpose of this thesis is to document the design, fabrication and testing of a data acquisition and control system for an internally-calibrated wide-band microwave radiometer as part of the NASA IIP-10 Airborne Radiometer Project led by Prof. Steven C. Reising at Colorado State University (CSU) in collaboration with Caltech's Jet Propulsion Laboratory (JPL). In this chapter, this IIP-10 Airborne Radiometer Project is introduced. The scientific motivation of the project is discussed, and a brief overview of the principles of microwave radiometers is given. Finally, an overview of the data acquisition and control system is presented, and the organization of this thesis is provided.

1.1 IIP-10 Airborne Radiometer Project at Colorado State University and Jet Propulsion Laboratory

The objective of the NASA IIP-10 Airborne Radiometer Project at CSU and JPL is to develop and produce an internally-calibrated, wide-band airborne radiometer to reduce risks associated with wet-path delay correction for the Surface Water and Ocean Topography (SWOT) mission. The specific goals of the project are to assess variability of the wet-tropospheric path delay on 10-km and smaller scales, demonstrate high-frequency millimeter-wave radiometry to improve coastal and enable over-land retrievals of wet path delay, and provide a calibration and validation instrument in support of the SWOT mission.

The approach to meeting this objective is as follows:

- Develop science requirements and flow them down to radiometer instrument design.
- Design and fabricate internally-calibrated, wide-band microwave, millimeter-wave window and millimeter-wave temperature and humidity sounding radiometer channels.

- Integrate channels into airborne radiometer instrument.
- Perform remote sensing test flight campaigns.
- Measure fine-scale water vapor using an integrated airborne radiometer over oceans, coastal areas and land.

The principal investigator for the IIP-10 is Professor Steven C. Reising, Director of the Microwave Systems Laboratory (MSL) at CSU. The Co-Investigators are Dr. Pekka Kangaslahti, Dr. Shannon Brown, Dr. Alan Tanner, Dr. Sharmila Padmanabhan, Mr. Douglas Dawson, Dr. Todd Gaier, and Mr. Steve DiNardo, all of JPL, and Professor Behzad Razavi of the University of California Los Angeles (UCLA) [1].

1.2 Scientific Motivation

Radar altimeter missions include nadir-viewing 18-37 GHz microwave radiometers to measure brightness temperatures, from which wet-tropospheric path delay is retrieved. However, these radiometers, including SWOT and the planned Jason Continuity of Service (Jason-CS) missions, cannot provide measurements sufficient for wet-path delay retrievals in coastal areas or over land, since the error due to land incursion at these frequencies is unacceptable at distances less than 40 km from the coastlines. Additional high-frequency window channels at 90, 130, and 168 GHz are optimum to improve performance in coastal areas, as schematically illustrated in Figure 1-1: Comparison of footprint sizes at high (millimeter-wave) and low (microwave) frequencies [1].

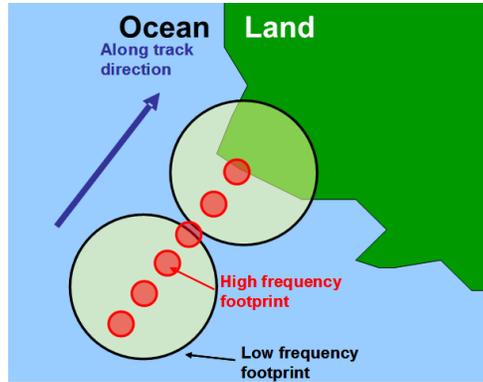


Figure 1-1: Comparison of footprint sizes at high (millimeter-wave) and low (microwave) frequencies [1].

The additional high-frequency channels provide brightness temperature measurements closer to the coast without land contamination, which in turn provide lower root mean square (RMS) error in wet-path delay retrieval. A hybrid Bayesian retrieval algorithm was used to retrieve wet-path delay from simulated brightness temperatures at both microwave and millimeter-wave window frequencies. The addition of millimeter-wave frequencies yielded a wet path delay retrieval error of less than 8 mm to within a few km of the coasts, as shown in Figure 1-2 [1].

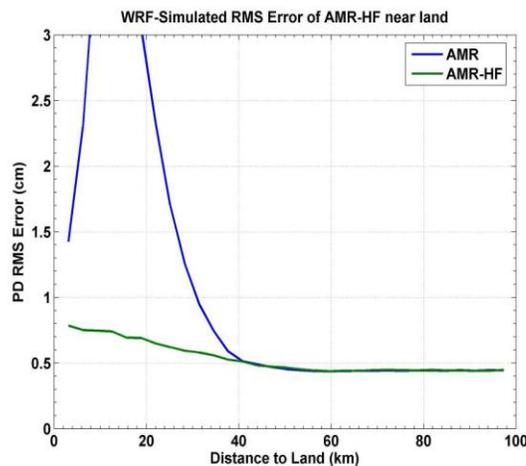


Figure 1-2: Root-mean-square errors in wet-path delay using microwave channels only (in blue) vs. both microwave and millimeter-wave window channels (in green) [1]

1.3 Frequencies used by the IIP-10 Airborne Radiometer

The IIP-10 airborne radiometer contains microwave channels, millimeter-wave window channels and millimeter-wave sounding channels. The microwave radiometers are adapted from the Advanced Microwave Radiometer (AMR) systems produced at JPL to fly on-board the JASON-1, JASON-2 (OSTP) and JASON-3 missions [2]. The millimeter-wave window channels are adapted from technology developments at CSU and JPL as part of an Advanced Component Technology 2008 (ACT-08) grant from NASA ESTO, also led by Professor Steven C. Reising as PI [3]. The temperature sounding channels are based on an application-specific integrated circuit (ASIC) developed as a subaward of the IIP-10 project to Professor Behzad Razavi, Director of the Communication Circuits Laboratory (CCL) at UCLA [4]. Table 1-1 lists the center frequencies of the channels used by the IIP-10 airborne radiometer.

Table 1-1: Frequency channels used by the IIP-10 Airborne Radiometer

Microwave Frequencies (GHz) (H & V polarizations)	Millimeter-wave Window Channel Frequencies (GHz)	Millimeter-Wave Temperature and Humidity Sounding Frequencies (GHz) (8 channels adjacent to each frequency)
18.7	90.0	118.0
23.8	130.0	183.0
34.0	168.0	

1.4 Introduction to Microwave Radiometer Systems

This section provides a brief overview of microwave radiometer theory and systems.

1.4.1 Introduction to Microwave Radiometer Theory

Radiometers measure the energy emitted by a given body at microwave and millimeter wavelengths. Radiometers are used to measure emission from terrestrial and atmospheric sources in Earth remote sensing and radio astronomy. In thermodynamic equilibrium, a black body, which is an ideal body that absorbs and re-emits all incident energy, radiates energy according to Planck's law uniformly in all directions with a spectral brightness density $B_f(T)$, in units of $W/(m^2SrHz)$, as given by [5]:

$$B_f(T) = \frac{2hf^3}{c^2} \frac{1}{e^{hf/kT} - 1} \quad (1-1)$$

where:

- h is Planck's constant ($6.6 \times 10^{-34} Js$)
- k is Boltzmann's constant ($1.38 \times 10^{-23} J/K$)
- c is the speed of light in vacuum ($2.99 \times 10^8 m/s$)
- f is frequency (Hz)

Furthermore, Planck's Law can be simplified up to 300 GHz to Rayleigh-Jeans' Law derived from the first order Taylor polynomial expansion of Planck's Law, where $B_f(T)$ is again given in units of $W/(m^2SrHz)$ as [5].

$$B_f(T) \approx \frac{2f^2 kT}{c^2} = \frac{2kT}{\lambda^2} \quad (1-2)$$

where λ is the wavelength of the frequency defined as $\lambda = c/f$. The power received by a lossless antenna with normalized radiation pattern $|F_n(\theta, \phi)|^2$, where θ and ϕ are the zenith and azimuth angles, respectively, over a bandwidth B_w centered at a center frequency f , kept at a constant physical temperature T , is described by:

$$P = \frac{kT}{\lambda^2} A_{eff} B_w \iint_{4\pi} |F_n(\theta, \phi)|^2 d\Omega \quad (1-3)$$

where A_{eff} is the effective area of the antenna, which is given by $A_{eff} = D\lambda^2/4\pi$, where D is the antenna directivity. When integrating the normalized antenna radiation pattern over the entire angular domain, Equation 1-3 simplifies to:

$$P = k B_w T \quad (1-4)$$

For a non-ideal black body, Equation 1-4 still holds true when using the concept of brightness temperature. Brightness temperature is defined as the equivalent temperature of a body when measuring a given power equal to that radiated by an ideal black body at the same physical temperature as the brightness temperature. The brightness temperature is always less than or equal to the physical temperature of the body.

Since measured radiometric power is proportional to physical temperature (Equation 1-4), one usually refers to antenna temperature as the value measured directly by a radiometer and brightness temperature as the power emitted by the body. Antenna temperature and brightness temperature are related but are not the same. The measured antenna temperature includes the

effects of the antenna pattern, as well as attenuation of the scene brightness temperature by the atmosphere and radiation from other sources, such as atmospheric emission and radiation coming from the antenna's secondary lobes [5].

Functionally, a radiometer relates antenna temperature to the brightness temperature, or power, emitted by a scene or object of interest. This concept is illustrated in Figure 1-3, where T is the brightness temperature of a scene at a given frequency, f , and, P is the power detected by the radiometer [6].

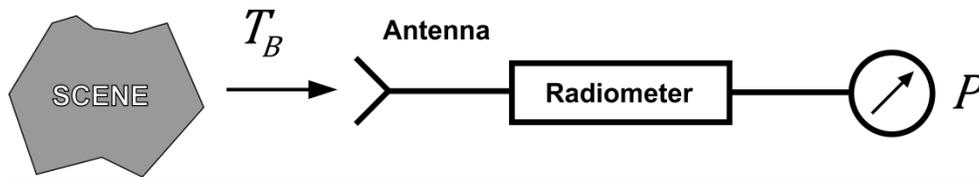


Figure 1-3: Illustration of a radiometer measuring a scene brightness temperature T and detecting power P [6]

However, realistic radiometers, like most electrical and electronic circuits and systems, generate thermal noise, which has to be taken into account. Also, realistic radiometers need to accomplish filtering to measure the power over a certain bandwidth around a desired center frequency and amplify the power to at least the range of tenths of millivolts. A more realistic illustration of a radiometer is shown in Figure 1-4 [6].

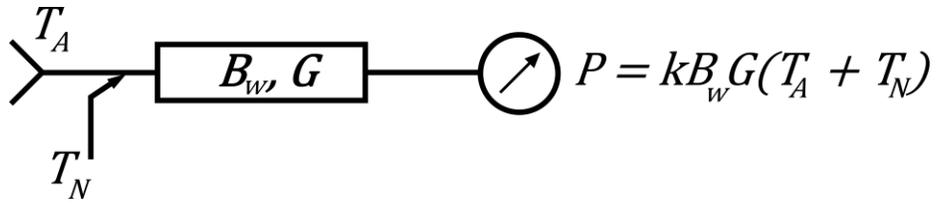


Figure 1-4: Illustration of radiometer with a receiver noise temperature T_N , antenna temperature T_A , bandwidth B , and gain G [6].

The power detected in Watts from the radiometer in Figure 1-4 is represented by Equation 1-5 [6].

$$P = kB_w G(T_A + T_N) \quad (1-5)$$

where:

- k is Boltzmann's constant ($1.38 \times 10^{-23} \text{ J/K}$)
- B_w is the bandwidth (Hz)
- G is the power gain
- T_A is the antenna temperature (K)
- T_N is the receiver noise temperature (K)

In addition, an important characteristic of any radiometer is the radiometric sensitivity, which is defined as the minimum change in brightness temperature that a radiometer can detect. Radiometric sensitivity of a total-power radiometer is shown in Equation 1-4, where τ is the integration time [6].

$$\Delta T = \frac{(T_A + T_N)}{\sqrt{B_w \tau}} \quad (1-6)$$

1.4.2 Introduction to Microwave Radiometer System Architecture

The microwave and the millimeter-wave window channel receivers in the IIP-10 Airborne Radiometer have a direct-detection Dicke architecture. Direct detection means that the signal is power detected without downconverting, and a Dicke architecture means that the radiometer has a switch before the first low-noise amplifier which alternates the input to the receiver between a scene and a reference to reduce the impact of gain fluctuations.

Since the radiometers are direct detection and do not require the use of local oscillators for heterodyne down conversion, the mass, volume, and power consumption of each radiometer are reduced. Direct-detection architecture is enabled by the use of high-frequency low-noise amplifiers, band definition filters and power detectors. The basic architecture of the microwave and millimeter-wave window channel radiometers in the IIP-10 Airborne Radiometer Project is shown in Figure 1-5 [3].

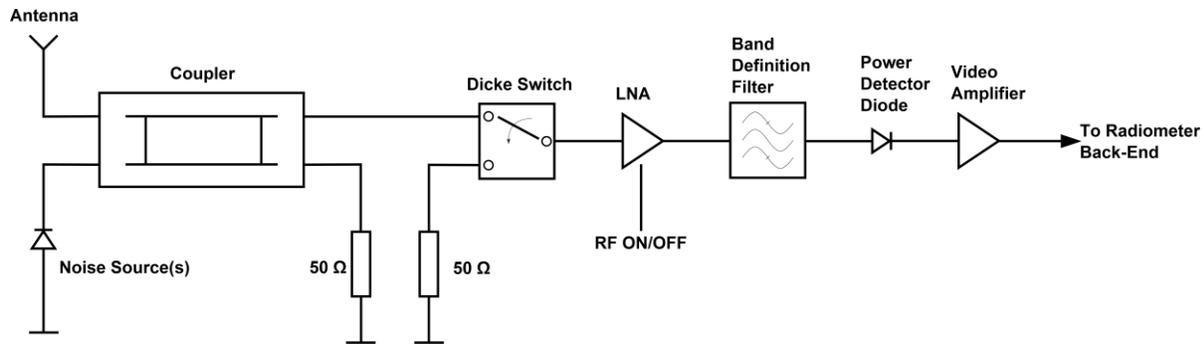


Figure 1-5: Simplified block diagram of the IIP-10 Airborne Radiometer microwave and millimeter-wave window channels [3]

The 10-dB directional couplers are used to couple the power from the noise diodes into the radiometer front-end with an attenuation of 10 dB, while simultaneously sending the signal from the antenna through to the radiometer front-end with only 10% attenuation. The microwave radiometers have three noise sources, while each of the millimeter-wave window-channel radiometers have two noise sources. The purpose of the noise sources is to inject noise into the system for calibration. The next component in the radiometer system is the Dicke switch, which switches the input of the radiometer between the output of the coupler (signal from the antenna) and the reference load. Dicke switching is performed so that the radiometer can measure the difference between the antenna temperature and the matched load as the second reference to measure gain fluctuations, as:

$$P_{Dicke} = kB(T_A - T_{REF}) \quad (1-7)$$

After the Dicke switch, the signal is amplified with a low-noise amplifier (LNA), and the bandwidth is defined using a band-pass filter. The last two components are the power detector and the video amplifier. The power detector diode squares the input signal so that the output

voltage is proportional to the input power. The video amplifier amplifies the signal so that the output signal level is large enough to achieve a sufficient signal-to-noise ratio on the coaxial cable connecting the output of the radiometer front-end to the radiometer back-end.

1.5 Introduction to Data Acquisition System

The purpose of this thesis work is to analyze, design, fabricate, and test the control and acquisition subsystem to meet design specifications. The output of the radiometer front-end is connected via a coaxial cable to the radiometer back-end for digitization. A top-level block diagram of the overall radiometer system is shown in Figure 1-6.

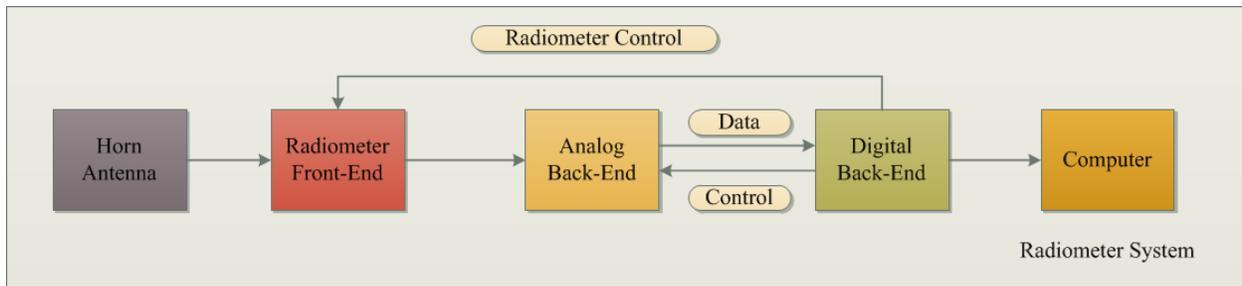


Figure 1-6: Top-level block diagram of radiometer system

The output signal from the video amplifier, i.e. the last element in each radiometer channel's front-end, is input to the analog back-end using a coaxial cable. The analog back-end board amplifies, filters, integrates, and digitizes the signal coming from the radiometer front-end. The digitized signal is then input to the digital back-end and it is then stored in a single-board computer housed inside of the IIP-10 Airborne Radiometer. The digital back-end consists of a buffer board and a field programmable gate array (FPGA). The buffer board buffers, level

converts, and interfaces with all signals from the FPGA. The FPGA outputs all signals used for radiometer control and the analog back-end, as well as reads in all sampled data from the analog back-end. These boards will be described in detail in later chapters.

1.6 Thesis Organizational Structure

After the introduction, in Chapter 2 this thesis discusses the control and data acquisition subsystem as well as the design specifications and how each specification was derived, including the offset paraboloid roughness, airborne platforms, radiometric footprints, sampling times, data throughput, and filtering architecture. Next, Chapter 3 provides a series of block diagrams showing the basic functions of all subsystems of the radiometer as well as the interfaces among the subsystems. A short explanation of each block diagram is provided. Chapter 3 is intended to provide a conceptual overview of the subsystems to aid the reader's understanding. Detailed explanations of the block diagrams are provided in Chapters 4 and 5. The analog and digital back-end boards are discussed in detail in Chapters 4 and 5, providing design strategies, fabrication processes, and test results. Finally, Chapter 6 presents a summary and conclusions of the thesis.

2. Acquisition Subsystem Design Specifications

The goal of this chapter is to analyze and identify the design requirements of the radiometer system so that the system can be designed to meet these specifications. Specifically, an analysis of the general system requirements of parabolic roughness, antenna footprint, integration time, and the number of bits required for digitization are given. A systems analysis of acquisition subsystems was conducted, and corresponding requirements were derived.

2.1 Impact of Paraboloid Roughness

To measure the brightness temperature emitted by the scene of interest, the power coming from the scene is first collected from a rotating flat reflector and then directed to a paraboloid where it is then focused to the feed horn antennas. The feed horn antennas receive the signals for radiometers, which amplify, filter, power detect, and digitize them. These subsystems are illustrated in Figure 2-1.

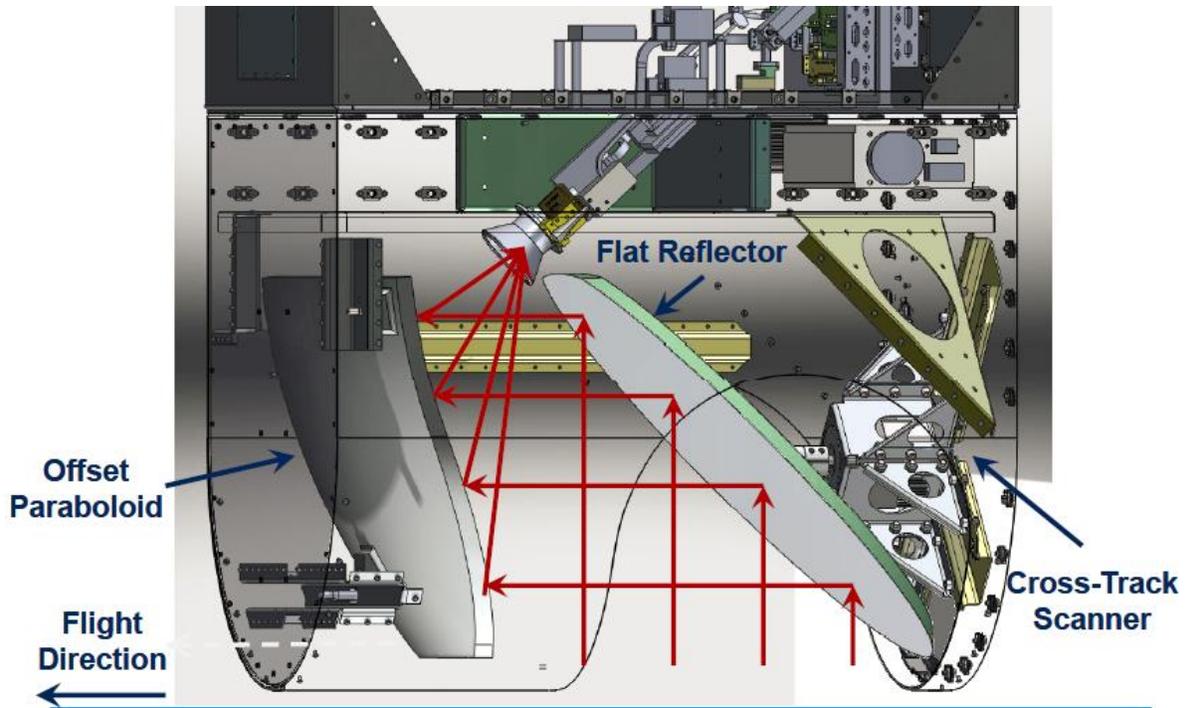


Figure 2-1: Flat reflector, parabolic reflector and cross-track scanner

To direct the power from the scene to the focal planes of the feed horn antennas, an offset paraboloid is used. An offset paraboloid is a section of a complete paraboloid and is useful in the aircraft platform because it does not block the antenna feed horn. Using an offset paraboloid has the additional benefit of having less volume and mass than that of a complete paraboloid. The difference between a paraboloid and an offset paraboloid is illustrated in Figure 2-2 (a) and (b), respectively.

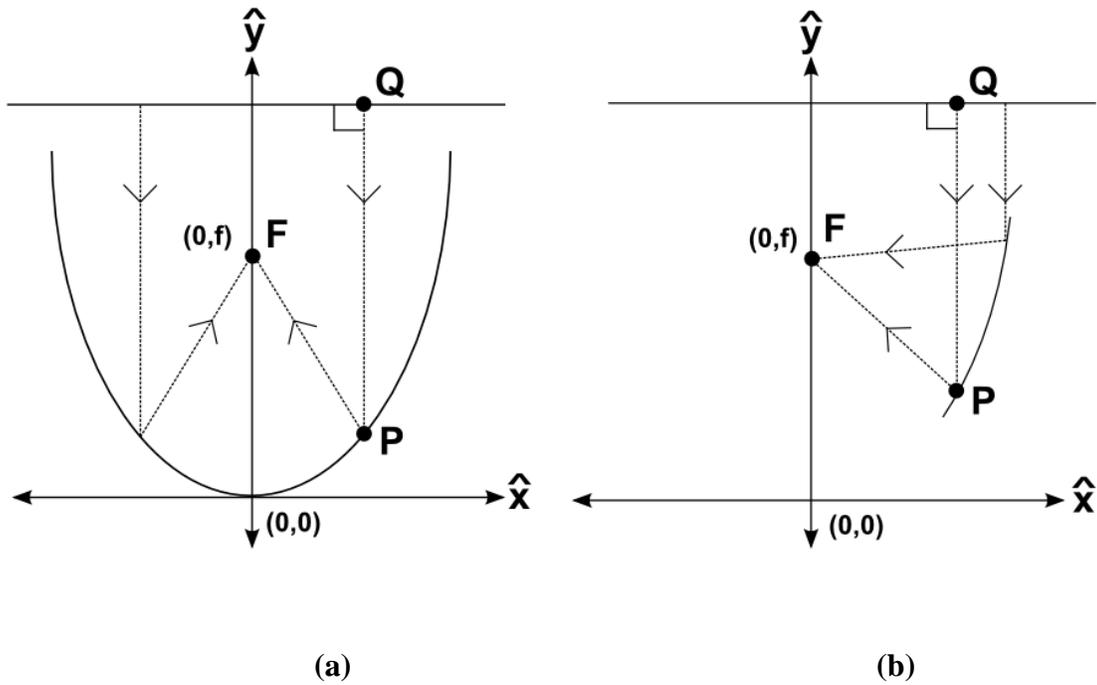


Figure 2-2: Geometry of paraboloid (a) and offset paraboloid (b)

For both paraboloids and offset paraboloids the relationship between the focal point, F , the point of reflection, P , and the position of incoming rays, Q , is given as [7]

$$|FP| = |QP| \quad (2-1)$$

Surface roughness of the paraboloid will affect the main beam efficiency, defined as the ratio of the power collected from the main beam of the observed scene to the total power collected. The main concern with the efficiency analysis is what happens when some power from the scene is lost. The power is re-radiated and the power collected by the feed horn has a significant component that is not coming from the scene. Furthermore, the magnitude and direction of this power that is not from the scene can be modulated by the scanning of the flat reflector.

The paraboloid roughness was simulated to determine the impact on antenna efficiency. The antenna roughness efficiency was calculated as [8]

$$\eta_{Distortion} = e^{-(4\pi K \frac{\sigma}{\lambda})^2} \quad (2-2)$$

where:

- $\frac{\sigma}{\lambda}$ denotes the surface Root Mean Square (RMS) distortion normalized to wavelength (λ),
and
- $K = 4F/D \sqrt{\log(1 + 1/(4F/D)^2)}$, and F/D is the ratio between the focal length and the aperture diameter.

Figure 2-3 shows the effect of the surface roughness on the antenna efficiency at a variety of F/D ratios. To obtain antenna efficiency close to one, the maximum roughness allowed is approximately $\lambda/100$.

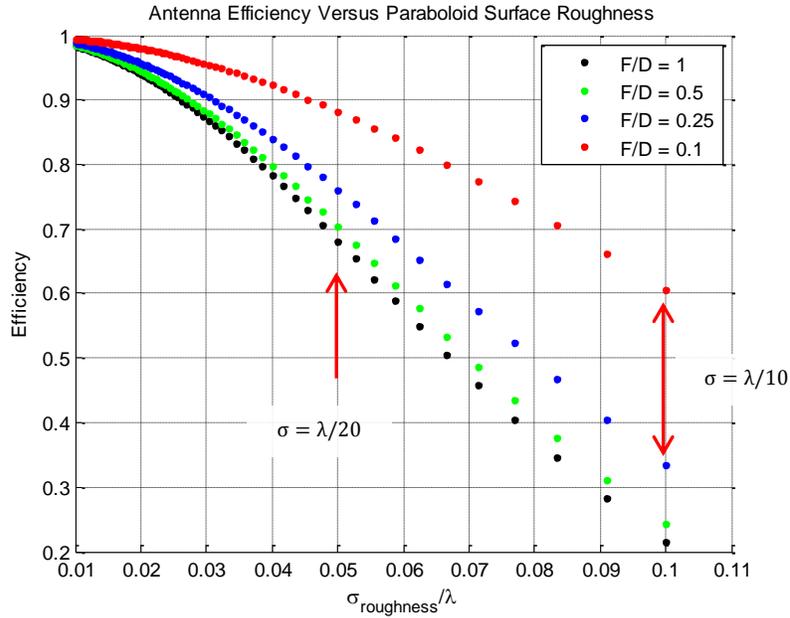


Figure 2-3: Surface roughness of the paraboloid impact on the antenna overall efficiency for several values of F/D

To significantly reduce the effect of surface roughness on antenna efficiency, Figure 2-3 shows that F/D has to be reduced to near 0.1. When $F/D = 0.1$ and $\sigma = \lambda/10$, the resulting efficiency is about 0.6, and for $\sigma = \lambda/20$, the resulting efficiency is about 0.88.

Based on this analysis, a paraboloid with a maximum surface roughness of 2 mils, equal to 0.002” or 51 microns, was chosen. At 180 GHz, this surface roughness in terms of wavelength is $\sigma = \lambda/32$, which corresponds to an efficiency of about 0.95. The paraboloid reflector was manufactured at the National Center for Atmospheric Research (NCAR) Earth Observing Laboratory’s Design and Fabrication Services. An image of the paraboloid reflector is shown in Figure 2-4.

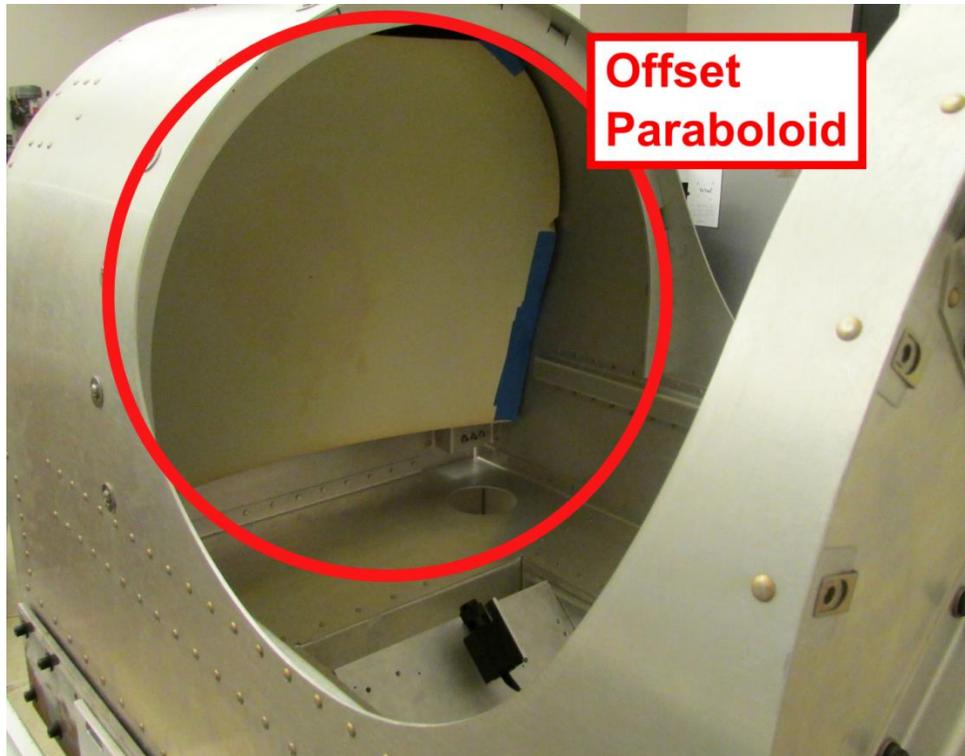


Figure 2-4: Offset paraboloid reflector mounted in the chassis

2.2 Airborne Platforms

The airborne platform constrains the design in several ways, the most important being the dimensions and total weight of the radiometer system. Furthermore, the nominal ground speed and flight altitude along with the half power beam width of each antenna will determine the footprint size, the spin rate of the scanning motor, and the radiometric resolution of each footprint. Finally, from these constraints the footprint sampling period and number of samples per footprint can be determined. The footprints of three aircraft and the corresponding radiometric resolutions were considered. These aircraft are the Twin Otter, King Air, and Global Hawk. A brief description of each aircraft is given in the following subsections.

2.2.1: Twin Otter

Shown in Figure 2-5, the Twin Otter is a short takeoff and land (STOL) utility aircraft with a high rate of climb that has a nominal velocity of 33 m/s and nominal cruising altitude of 3 km. The low nominal velocity and cruising altitude of Twin Otter makes it ideal for testing and prototyping scientific instruments [9].



Figure 2-5: Twin Otter [10]

2.2.2 King Air

Shown in Figure 2-6, the King Air is a twin turbo-prop utility aircraft with a nominal ground velocity of 140 m/s and a nominal cruising altitude of 9.1 km [11]



Figure 2-6: King Air [12]

2.2.3 Global Hawk

Shown in Figure 2-7, the Global Hawk is an unmanned aerial vehicle surveillance aircraft used as a high-altitude platform with a nominal velocity of 172 m/s and a nominal cruising altitude of 19.8 km. The key feature of the Global Hawk for scientific usefulness is its long flight duration of up to 30 hours. [13]



Figure 2-7: NASA Global Hawk [14]

Though all three aircraft were considered, the radiometer is being designed to accommodate only the Twin Otter and Global Hawk due to size constraints imposed by the King Air.

2.2.4 Radiometer Footprint from Various Airborne Platforms

The instrument will scan the scene of interest in the across track direction to increase the total swath of the scan. The scene of interest is scanned using a rotating flat reflector, as illustrated in Figure 2-8.

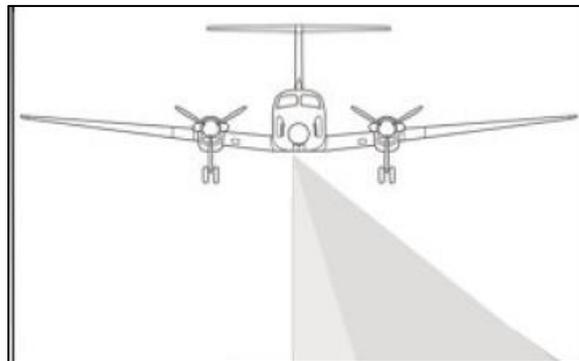


Figure 2-8: Cross track scanning diagram [1]

To determine the required rotation speed of the flat reflector, a MATLAB[®] script was written to analyze the antenna footprint dimensions and the radiometric resolution so that the effects of aircraft velocity and altitude as well as reflector spin rate and incidence angle on the ground could be taken into account and plotted. The assumption was made that each aircraft flies at a constant velocity, i.e. in a straight trajectory at a constant speed.

Furthermore, the three attitude angles, pitch, roll and yaw, were assumed to be constant. While the instrument is in flight testing, an on-board Inertial Measurement Unit (IMU) will measure and record pitch, roll, and yaw which affect the actual footprint position and size. Figure 2-9 is a

diagram illustrating the pitch, roll, and yaw angles. The MATLAB[®] script for these footprints is available in appendix *MATLAB Script for Footprint Analysis*.

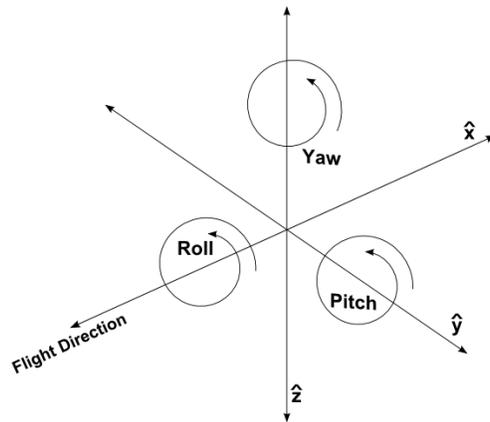


Figure 2-9: Illustration of pitch, roll and yaw angles

2.2.5 Theory of Footprint Analysis

Figure 2-10 shows the geometry of the footprint being scanned, where θ_{HPBW} is the angle of incidence of the scanning flat reflector and θ_{HPBW} is the half-power beam width of the antenna.

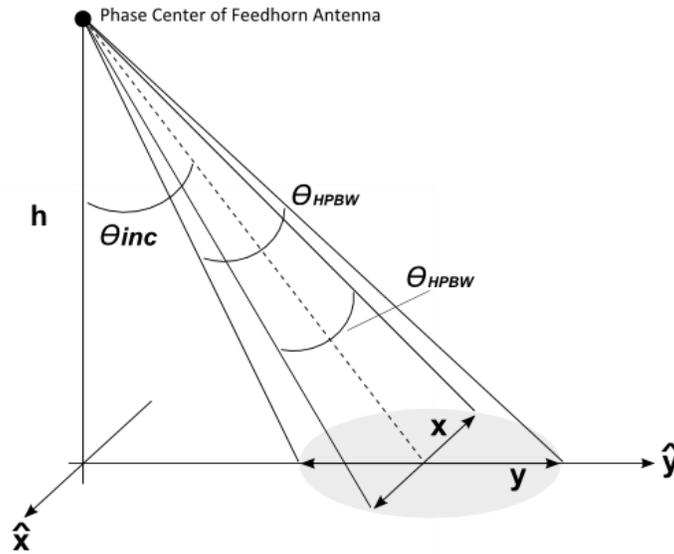


Figure 2-10: Geometry of the incidence angle (θ_{inc}) and half-power beam width (θ_{HPBW})

Equations 2-3 and 2-4 show the relationships among the parameters, including the aircraft altitude h and the half-power beam width θ_{HPBW} , after reflection from the primary parabolic reflector and the secondary scanning flat-plate reflector. The incidence angle of the radiometer measurement at the surface is θ_{inc} .

- Along-track dimension of footprint

$$y = 2h \sec(\theta_{inc}) \tan(\theta_{HPBW}/2) \quad (2-3)$$

- Cross-track dimension of footprint

$$x = h(\tan(\theta_{inc} + \theta_{HPBW}/2) - \tan(\theta_{inc} - \theta_{HPBW}/2)) \quad (2-4)$$

The half power beam width is defined as the angle between the half-power (-3 dB) points of the main lobe of the antenna pattern and is illustrated in Figure 2-11.

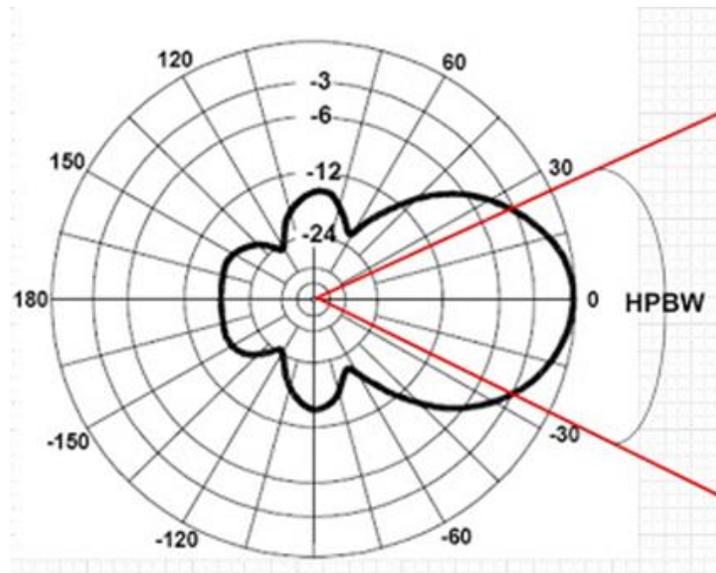


Figure 2-11: Polar coordinate diagram of half power beam width example [15]

Each radiometer channel has a specific half-power beam width which will also affect individual footprint position and size. This will be taken into account when analyzing the in-flight data.

Table 2-1 shows each frequency channel and its corresponding half-power beam width [16].

Table 2-1: Half-Power Beam Width of radiometer channels [16]

Channel Frequency (GHz)	Beam Width (Degrees)
18.7	3.46
23.8	3.06
34.0	2.14
90.0	1.36
130.0	0.44
168.0	0.34
118.8	0.95
183.3	0.67

2.2.6 Simulation of Footprints

For given values of aircraft altitude, ground speed, and reflector spin rate in revolutions per minute (rpm), scanning was simulated from nadir to a 60° incidence angle on either side of the aircraft. The scan was simulated only to 60° because larger angles produce footprints which are too distorted in the cross-track direction. Figures Figure 2-12, Figure 2-13 and Figure 2-14 show instantaneous fields of view for four rotations of the flat reflector for the Twin Otter, King Air and Global Hawk aircraft, respectively. Reflector spin rates were chosen so that each footprint has no overlap and no gap between adjacent footprints. These figures were made using the antenna beam width of $\theta_{HPBW} = 0.67^\circ$. Table 2-2 shows the corresponding parameters associated with each aircraft footprint.

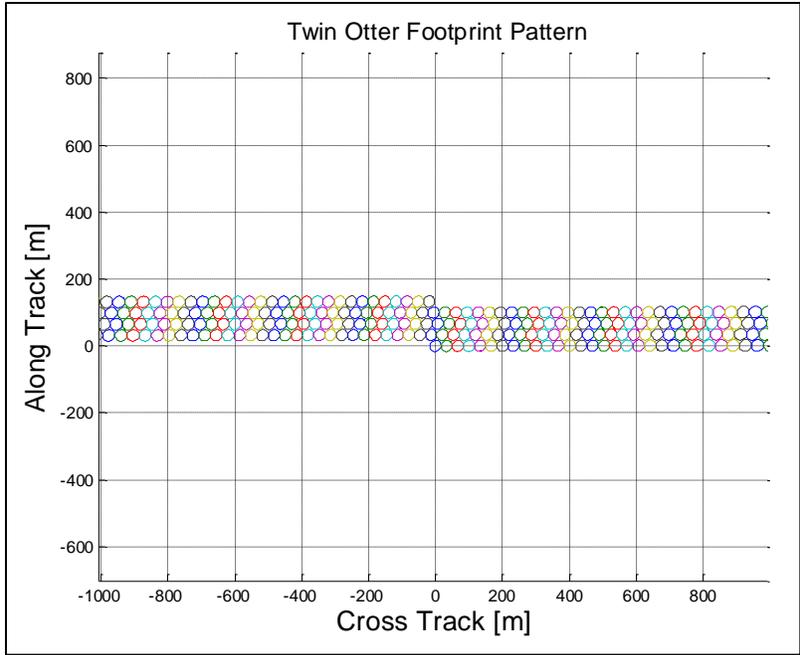


Figure 2-12: Twin Otter footprint pattern

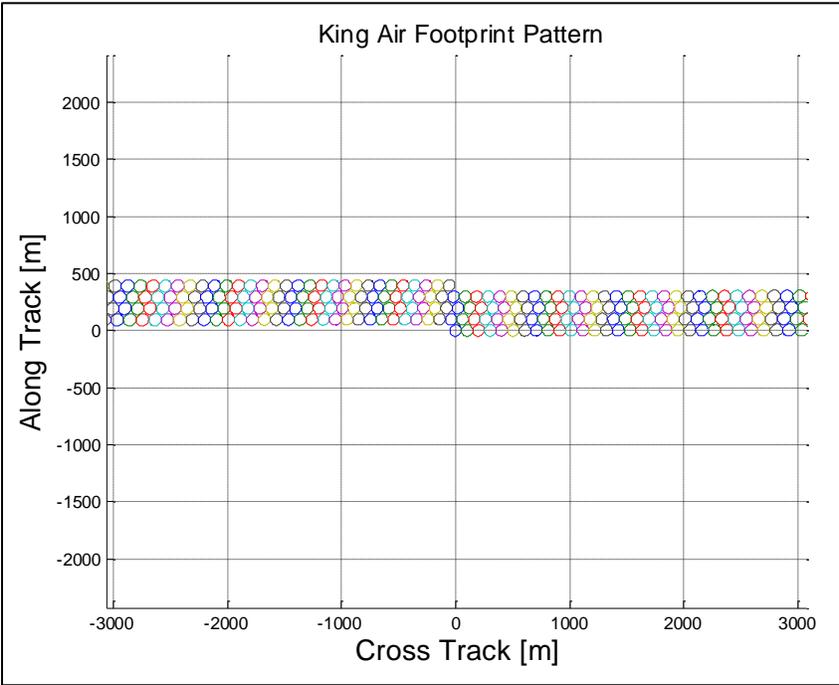


Figure 2-13: King Air footprint pattern

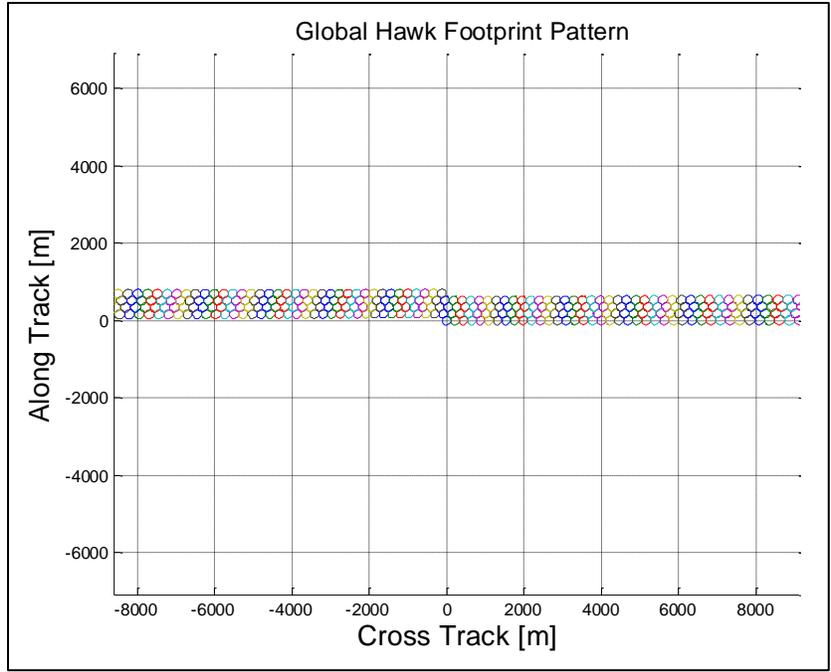


Figure 2-14: Global Hawk footprint pattern

Table 2-2 lists the nominal altitude and ground speed of all three aircraft with the corresponding reflector spin rates, swath widths, cross-track dimensions, and along-track dimensions. Minimum track cross-track dimensions occur when θ_{inc} is 0° while maximum cross-track dimension occurs when θ_{inc} is 60° .

Table 2-2: Twin Otter, King Air and Global Hawk footprint parameters

Parameter	Twin Otter	King Air	Global Hawk
Altitude	3 km	9.1 km	19.8 km
Ground Speed	33 m/s	140 m/s	172 m/s
Reflector Spin Rate	60 rpm	85 rpm	48 rpm
Footprint Time	1.9 ms	1.3 ms	2.4 ms
Swath Width	10.5 km	31.8 km	69.2 km
Minimum Cross-Track Dimension of Footprint	33.28 m	100.95 m	219.65 m
Maximum Cross-Track Dimension of Footprint	133.13 m	403.76 m	878.51 m
Minimum Along-Track Dimension of Footprint	33.28 m	100.95 m	219.65 m
Maximum Along-Track Dimension of Footprint	66.55 m	201.88 m	439.25 m

2.2.7 Impact of Radiometric Resolution on Footprint Size

As defined in Equation 1-3, the calculated radiometric resolution, *NEAT*, of each radiometer channel for each aircraft configuration is shown in Table 2-3. The expected value of the system noise temperature is given for each channel using an assumed antenna temperature of 200 K. The antenna temperature will change for each scene and frequency, but this is just a starting point to estimate radiometric resolution.

Table 2-3: Radiometric Resolution (*NEAT*) for Microwave Channels and Millimeter-wave Window Channels

Frequency (GHz)	T_{sys} (K) (Expected)	Twin Otter <i>NEAT</i> (K)	King Air <i>NEAT</i> (K)	Global Hawk <i>NEAT</i> (K)
18.7	800	1.30	1.55	1.16
23.8	925	1.06	1.27	0.95
34.0	1050	0.99	1.17	0.88
90.0	1600	0.37	0.44	0.33
130.0	1700	0.39	0.47	0.35
166.0	1800	0.41	0.49	0.37

2.2.8 Summary of Footprint Analysis

Footprints were shown for the Twin Otter, King Air, and Global Hawk, and their along-track and cross-track dimensions were calculated. Radiometric resolutions were calculated for both microwave channels and millimeter-wave window channels. Assuming a specific range of incidence angles, antenna beam width, aircraft altitude, and ground speed, the only remaining variable is the reflector spin rate. Integration times were chosen so that adjacent footprints touch but do not overlap. Reflector spin rates were chosen to ensure no footprint overlap as well as no along-track gap between footprints.

2.3 Sampling and Data Throughput

Each radiometer channel is digitized at 14-bit resolution, as will be shown in Section 2.4, for each integration time. The assumption is made that data from these radiometer channels need to be collected even when the antenna is pointing to the inside of the aircraft. The “data packet” for each channel has the following components.

- Header: 24 bits
- Radiometric data: 14 bits from the analog to digital converter (ADC) (with 2 additional filler bits) multiplied by the number of channels
- Info data: 24 bits for motor control and switch position control

Thus the total number of bits per channel can be found using Equation 2-5.

$$Bits_{Total} = Bits_{Header} + (Bits_{ADC} + Bits_{Filler})(\# \text{ of channels}) + Bits_{Housekeeping} \quad (2-5)$$

The data transfer rate can be determined using Equation 2-6.

$$Transfer \text{ Rate} = (Bits_{Total})(Sampling \text{ Period}) \quad (2-6)$$

The sampling period is defined by Equation 2-7.

$$Sampling \text{ Period} = \frac{Time \text{ per Footprint}}{Samples \text{ per Footprint}} \quad (2-7)$$

The nominal estimate of the sampling period for each radiometer along with each corresponding time per footprint and samples per footprint are shown in Table 2-4.

Table 2-4: Footprint time, samples per footprint, and sampling period for each radiometer type

Radiometer Type	Nominal Footprint Time (ms)	Nominal Samples per Footprint	Sampling Period (ms)
Microwave	10	50	0.2
Millimeter-wave Window Channels	2	20	0.1
Millimeter-wave Sounding Channels	3	5	0.6

The data transfer rates for all three radiometers are shown in Table 2-5 in both kilobits per second (kbps) and in kilobytes per second (kBps). The microwave frequencies have 6 channels which are digitized using two analog back-end boards. The millimeter-wave window frequencies have 3 channels plus one additional unused channel on an analog back-end board, for a total of 4 channels. The millimeter-wave sounding frequencies have 16 channels, which will be digitized using four analog back-end boards.

Table 2-5: Data throughput rates for IIP-10 radiometer channels

Radiometer Type	Header [bits]	Radiometric Data [bits]	Info Data [bits]	Total bits to send	Sampling Period (ms)	Rate (kbps)	Rate (kBps)
Microwave	24	128	24	176	0.2	880	110
Millimeter Wave Window Channels	24	64	24	112	0.1	1120	140
Millimeter Wave Sounding Channels	24	256	24	304	0.6	304	38

Adding the data throughput rates for each channel in Table 2-5, the total data throughput for the entire system is 2304 kbps, or 288 kBps.

2.4 Bit Requirement Analysis

To ensure that the quantization error from digitization is much less than the uncertainty inherent in each radiometer, the following analysis was conducted. The quantization error of an analog to digital converter is given by Equation 2-8 [17]

$$Error_{Quantization} = \frac{V_{Total}}{2^{Number\ of\ Bits}} \quad (2-8)$$

The radiometric uncertainty is given by Equation 2-9 [6].

$$\Delta T = \frac{T_{sys}}{\sqrt{(BW)(\tau)}} \quad (2-9)$$

To ensure sufficient number of bits for the ADC, the quantization error must be much less than the radiometric uncertainty. Equations 2-8 and 2-9 can be used to form the requirement given in Equation 2-10.

$$\frac{V_{Total}}{2^{Number\ of\ Bits}} \ll \frac{T_{sys}}{\sqrt{(BW)(\tau)}} \quad (2-10)$$

Assuming that total system temperature, T_{sys} , is equal to the total input voltage, V_{Total} , Equation 2-11 is derived.

$$\frac{1}{2^{Number\ of\ Bits}} \ll \frac{1}{\sqrt{(BW)(\tau)}} \quad (2-11)$$

The quantization error for digitizing with 8 to 20 bit resolution is shown as a function of radiometric resolution for all three radiometers, is shown in Figure 2-15. A MatLab script for this plot is available in Appendix I, entitled *Analog to Digital Converter Bit Number Analysis*.

$$\frac{1}{2^{Number\ of\ Bits}} \ll \frac{1}{\sqrt{(BW)(\tau)}}$$

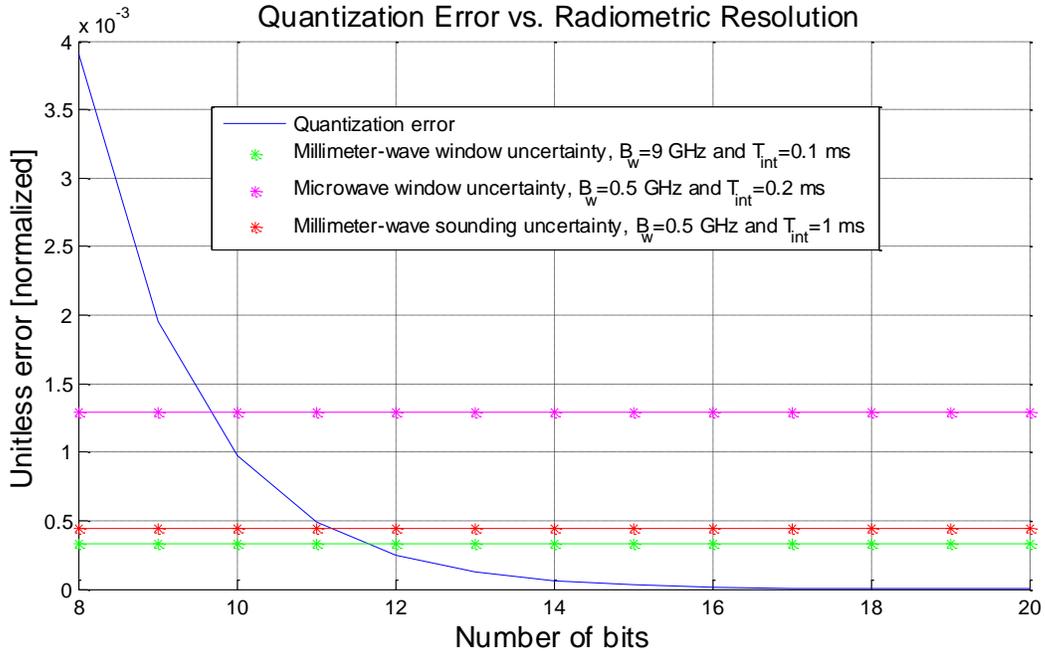


Figure 2-15: Quantization error and radiometer uncertainty

Figure 2-15 shows that the minimum number of bits needed to ensure that the quantization error from the analog-to-digital converter is sufficiently lower than the radiometer resolution of all three radiometers is 14 bits.

2.4 Low-Pass Filter versus Integrator

The signal from the radiometer needs to be either filtered or integrated before digitization to reduce the measurement uncertainty. A low pass filter is the simpler design from a signal management point of view; however, it may add sample-to-sample leakage. A switched capacitor integrator does not have nearly as much sample leakage but is more complex to control. The sample leakage error produced by a low-pass filter was compared to that of an integrator to determine which one is preferred before digitization of the radiometric signal. The filter is a second order analog Butterworth low-pass filter, and the integrator is an “integrate-and-dump

integrator. These comparisons are performed at sampling frequencies of 1 kHz, 20 kHz, and 100 kHz.

The filter cut-off frequency is half of each sampling frequency. The data for each sample number shows the low-pass filter error designated by an “o” in comparison to the integrator error designated by a dot. These comparisons are shown in Figures Figure 2-16, Figure 2-17 and Figure 2-18. The Matlab script for this analysis is available in Appendix II entitled *MatLab Script of Low-Pass Filter versus Integrator*.

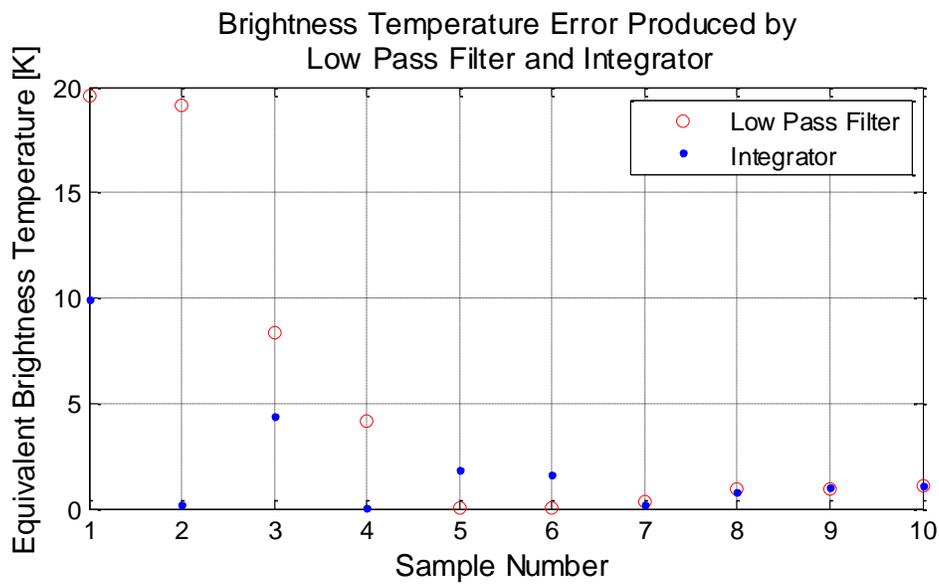


Figure 2-16: Low-pass filter and integrator comparison at $f_s = 1$ kHz

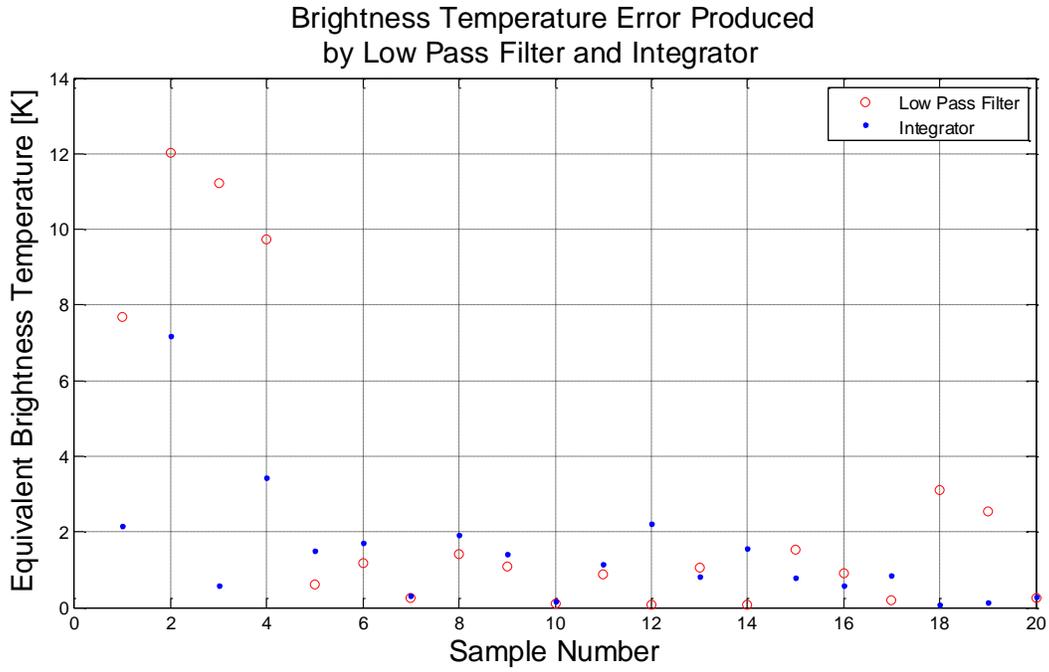


Figure 2-17: Low-pass filter and integrator comparison at $f_s = 20$ KHz

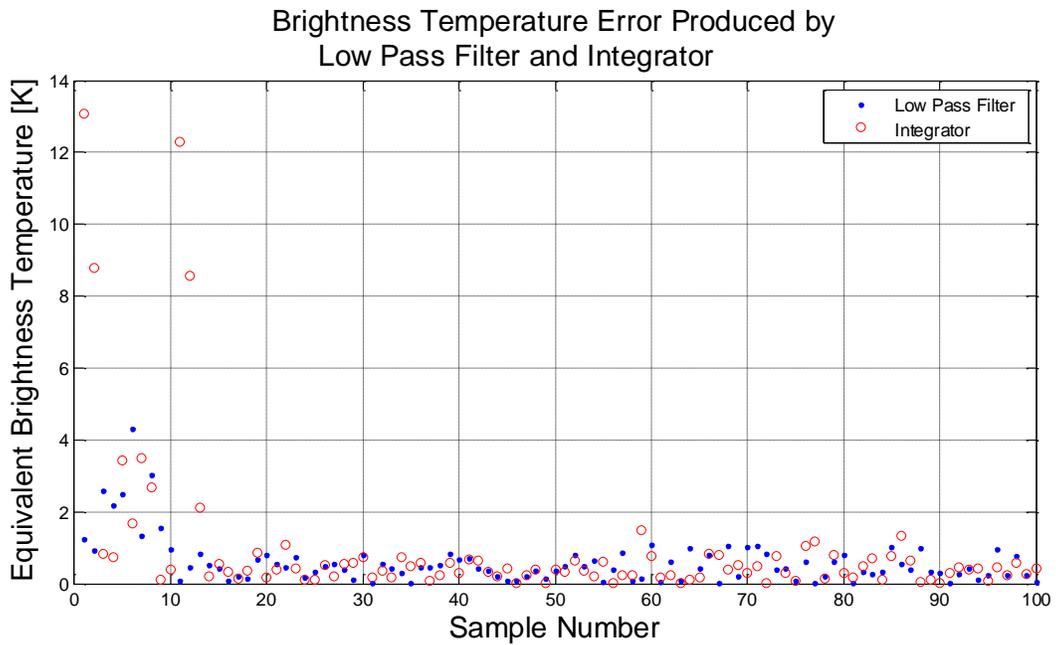


Figure 2-18: Low-pass filter and integrator comparison at $f_s = 100$ kHz

An analysis of the low-pass filter error at this range of frequencies shows that increasing the sampling frequency decreases the error. Moreover, if an average error of about 1 K is desired for the noise diode and Dicke switching, a minimum sampling rate of 40 kHz is needed. For all of these sampling rates, to determine the antenna temperature of the scene, approximately the first 10-15% of the samples should be ignored in post-processing because they correspond to samples from the noise diode and matched load. However, after averaging the rest of the samples, the error from the integrator is less than that of a low-pass filter at all sampling frequencies lower than 40 kHz. Since keeping the data rates low is a concern, an “integrate-and-dump” integrator is preferred over a low-pass filter even though this integrator adds complexity to the design of the back-end board.

2.5 Acquisition Subsystem Analysis Summary

From the acquisition subsystem analysis design, specifications were determined for the paraboloid surface roughness, airborne platforms and corresponding footprints, data throughput, the number of bits required for digitation, and filtering technique. The paraboloid surface roughness should be a maximum of 0.002 inches (51 microns). Three aircraft were analyzed; however, only the Twin Otter and Global Hawk will be able to hold the instrument. The footprint and scanning spin rate of these aircraft are given in Table 2-2. The data throughput of all three radiometer types is given in Table 2-4. Each radiometer channel will be digitized with a 14 bit analog to digital converter. Finally an “integrate and dump” integrator will be used to filter each of the radiometers’ signals.

3. System Block Diagrams

This chapter presents and explains the block diagrams for the entire acquisition system, including the analog back-end, and the Field Programmable Gate Array (FPGA) and buffer board. These block diagrams are also presented in later chapters but are shown here to provide a high-level description of the acquisition and control systems used in the IIP-10 airborne radiometer.

3.1 Entire Acquisition System Block Diagram

The radiometer front end, the analog back-end, and the flat reflector motor are all controlled by the digital back-end consisting of the BeMicro (Standard Development Kit) SDK FPGA and buffer board [18]. The FPGA is controlled by and sends data to an onboard computer. Data from the Global Positioning System (GPS) and Inertial Measurement System (IMU) as well as data from the thermistor acquisition system are also read-in by this computer. Figure 3-1 is the block diagram of the entire acquisition system.

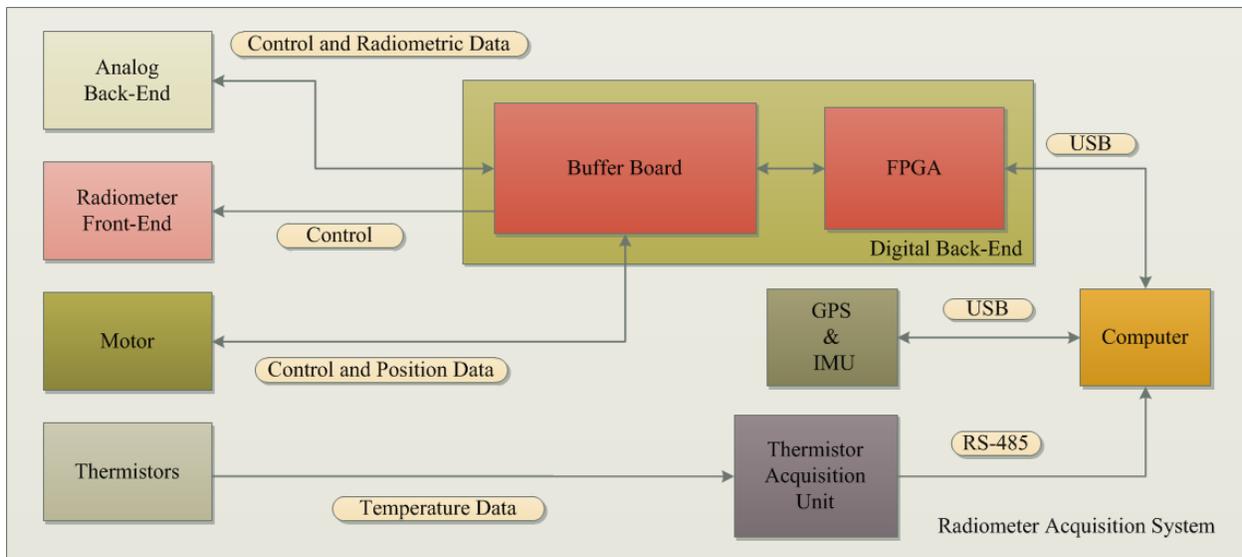


Figure 3-1: Radiometer acquisition system block diagram

3.2 Radiometer Acquisition System Block Diagram

Radiation from the scene of interest is detected with the feed-horn and radiometer front-end which outputs a signal from a power detector diode that is then video-amplified. The signal from the video amplifier is sent to the analog back-end via a coaxial cable with a Subminiature-A (SMA) connector. Once digitized, the signal is sent via a 9 Pin D-Subminiature (DE-9) connector and cable to the digital back-end. The integrator and ADC are also controlled by the digital back-end through the same connector. All data from the FPGA is sent to an on-board computer using a Universal Serial Bus (USB) connection. The FPGA and buffer board also control the Dicke switching, noise source, and radiometer on/off switch (RF switch) for the radiometer front-end. The digital back-end also reads in the data from the analog back-end. The radiometer system simplified block diagram is shown in Figure 3-2.

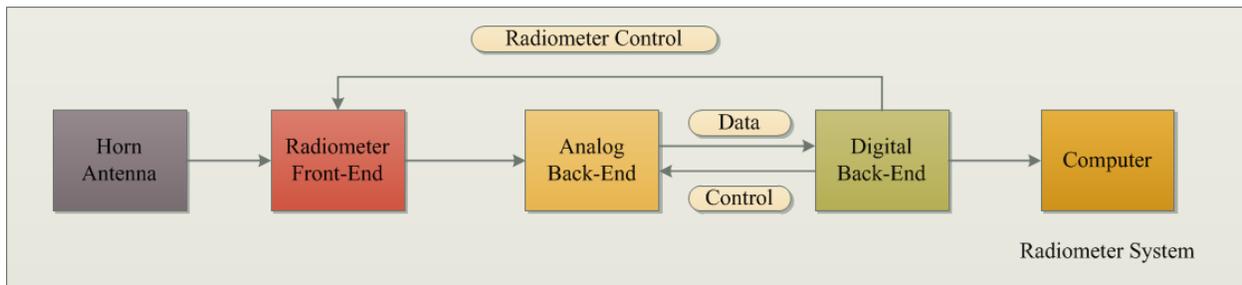


Figure 3-2: Radiometer system simplified block diagram

3.3 Analog and Digital Back-End System Block Diagram

Each analog back-end board has four SMA inputs, and each channel has a gain and filtering stage, integration stage, differential driver stage, and digitization stage. The entire system

includes seven analog back-end boards, all of which are interfaced to and controlled by the FPGA through the buffer board to accommodate all channels used in the IIP-10. Figure 3-3 shows an in-depth block diagram of the analog back-end and the digital back-end.

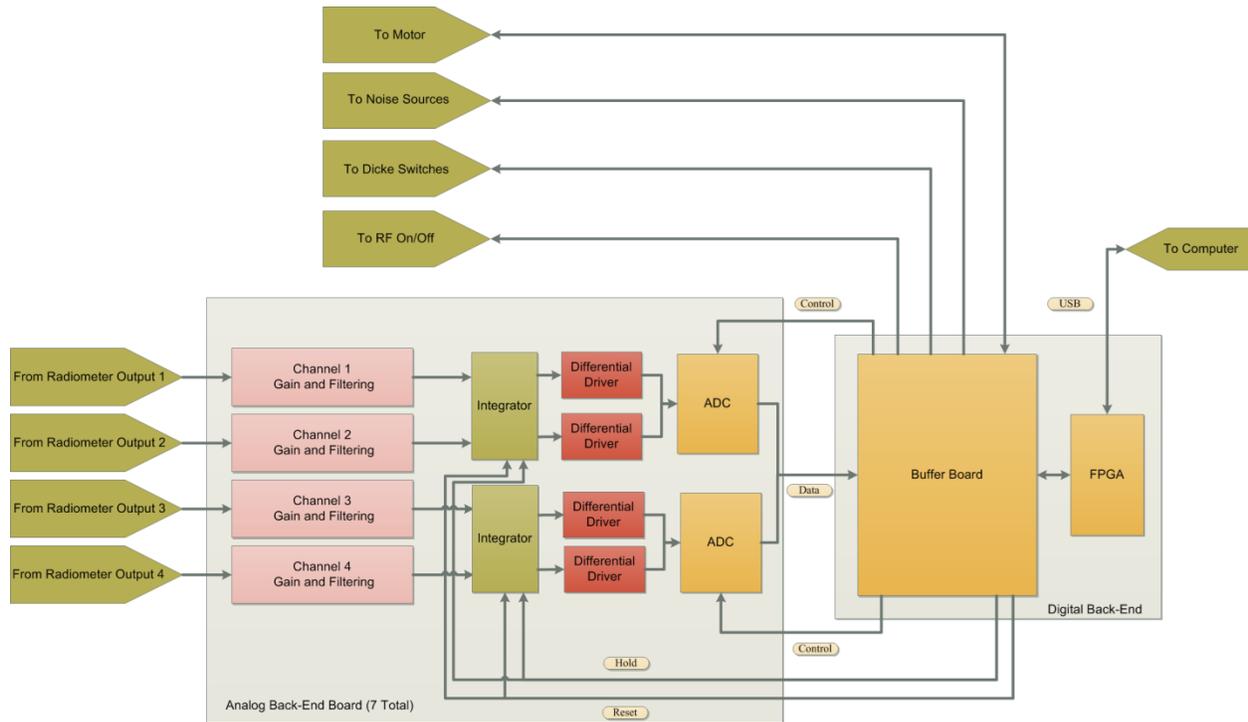


Figure 3-3: Analog and digital back-end block diagram

3.4 Buffer Board Block Diagram

To buffer and route all signals coming to and from the FPGA, a buffer board was created. The board buffers all radiometer control signals and drives them at the appropriate voltages. Also, all analog back-end board control signals are buffered through this board, and all analog back-end board data is sent to the buffer board. The motor control signals are also buffered through this board. Figure 3-4 shows the block diagram of the buffer board.

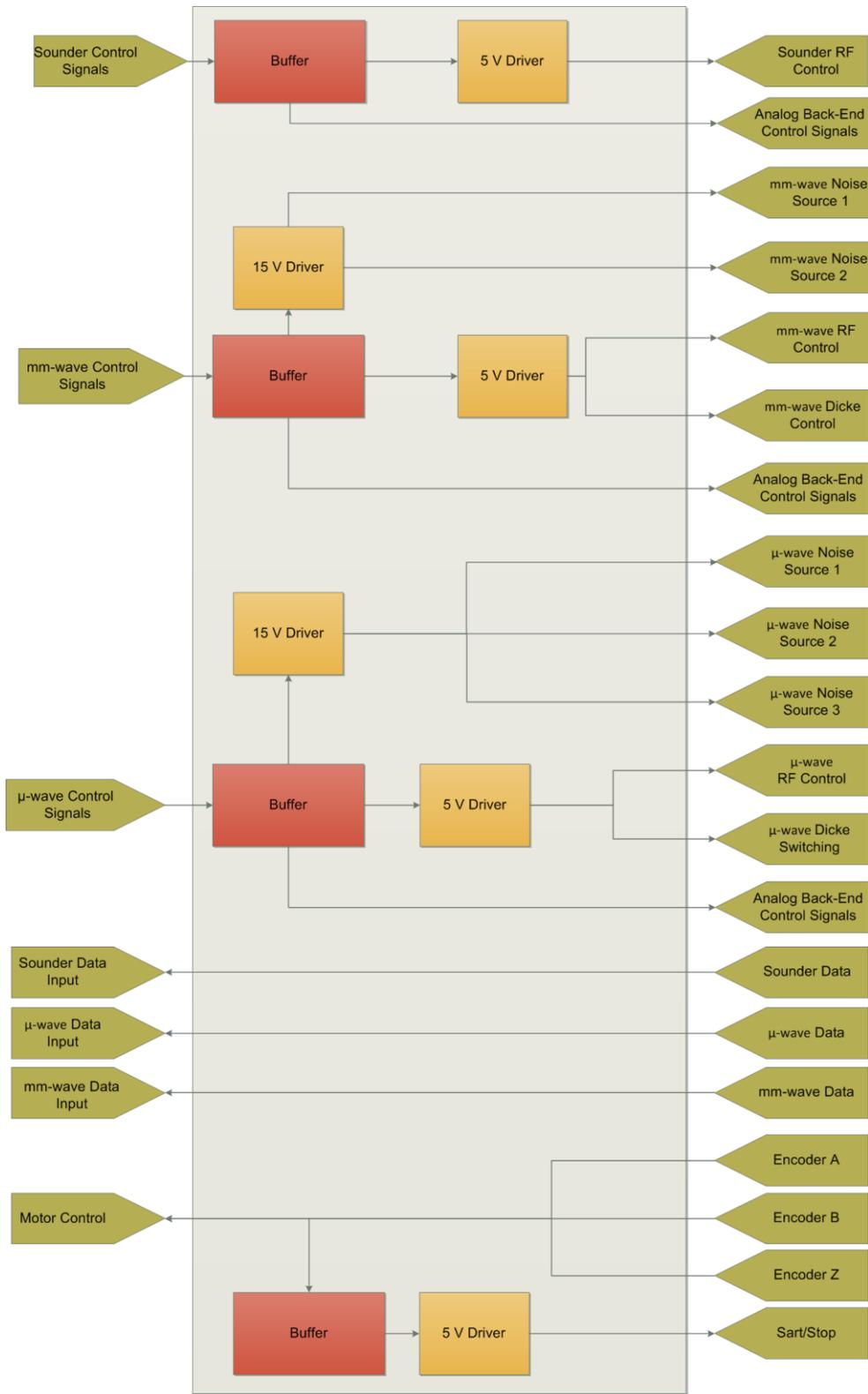


Figure 3-4: Buffer board block diagram

3.5 FPGA Block Diagram

Figure 3-5 shows a block diagram of the BeMicro SDK FPGA. The BeMicro SDK is configured via an Ethernet cable using the onboard NIOS2 Microprocessor [19]. This configures the calibration sequence generators, which provide the radiometer and analog back-end control signals, as well as the chip select (CS) signal for the Serial Protocol Interface (SPI). The CS signal controls when the ADC is actually sampling, and the SPI signal provides all analog back-end SPI clocks and also reads in the data from the analog back-end boards. This data is sent through a double buffer and an SPI-to-USB Converter and then sent to a computer for storage.

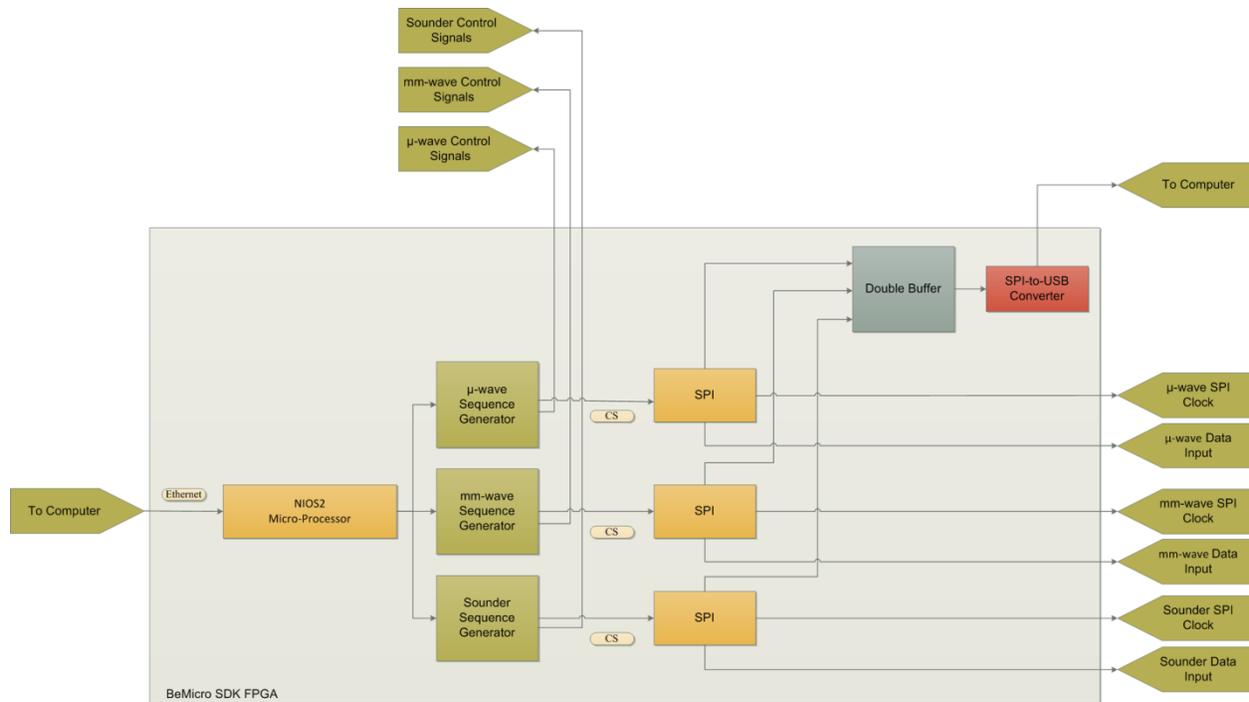


Figure 3-5: BeMicro SDK FPGA block diagram

4. Analog Back-End Board Design and Test Results

This chapter will discuss the design and test results of the analog back-end board in depth. The IIP-10 instrument will have 6 microwave channels at 18.7, 23.8 and 34.0 GHz at H and V polarizations, 3 millimeter-wave window channels at 90, 130, and 166 GHz, and 16 millimeter-wave sounding channels in 8 bands near 118 and 183 GHz. All of these 25 channels are digitized using a total of 7 analog back-end boards. Each board is approximately three inches by six inches and can digitize up to four channels. In total, one board is used for each of the H and V polarizations of the microwave channels, one board is used for the millimeter-wave window channels, and 4 boards are used for the millimeter-wave sounding channels. Figure 4-1 is an image of the analog back-end board.

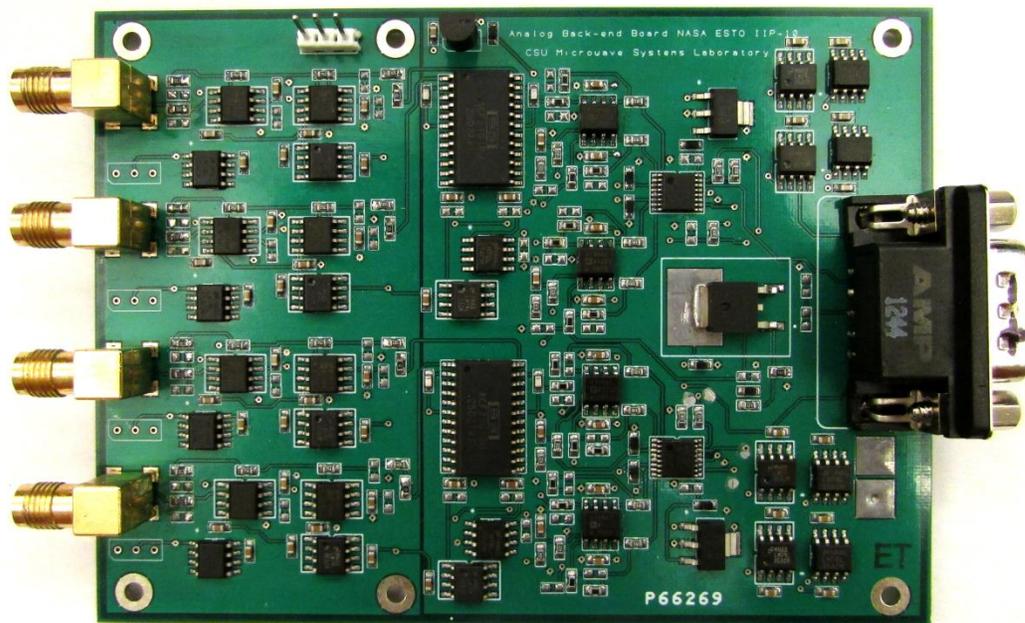


Figure 4-1: Analog back-end board

The analog back-end board was designed using DesignSpark Schematic Capture and Printed Circuit Board (PCB) Software [20]. The complete schematic is shown in Appendix III, entitled *Analog Back-End Board Schematic*. The PCB layout and three-dimensional model are shown in Figure 4-2 (a) and (b), respectively.

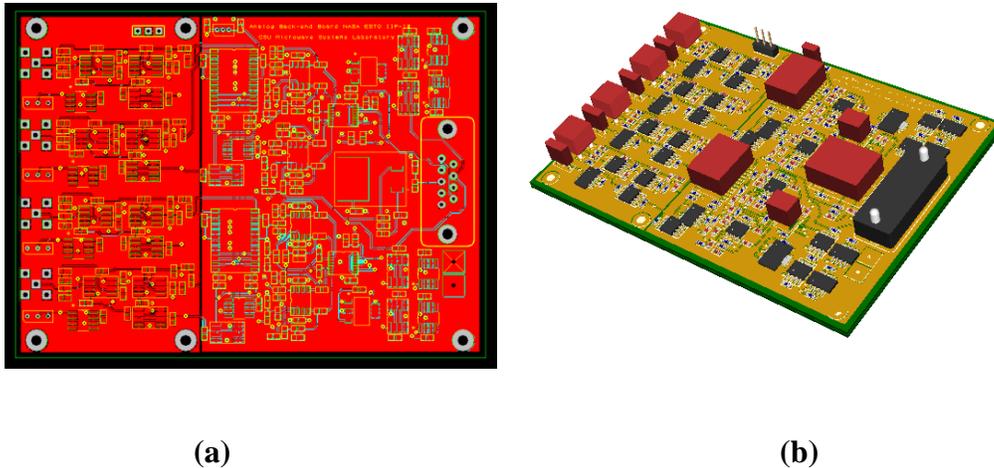


Figure 4-2: Analog back-end board (a) PCB layout and (b) three-dimensional model from DesignSpark

4.1 Analog Back-End Board Functional Components

The analog back-end board was designed to perform signal conditioning and digitization of the output of the radiometer front-end. This output is the power detector signal which has been amplified using the video amplifier of the radiometer. Each analog back-end board has four input channels with gain and filtering stages for each input. Next, the signals are integrated with a two-channel integrator. Afterward, each signal is converted from a single-ended signal to a differential signal using a single-channel differential driver. Finally, the signal is digitized using

a two-channel ADC. The following is an in-depth explanation of all stages. Figure 4-3 is a block diagram of the analog back-end board interfaced with the digital back-end.

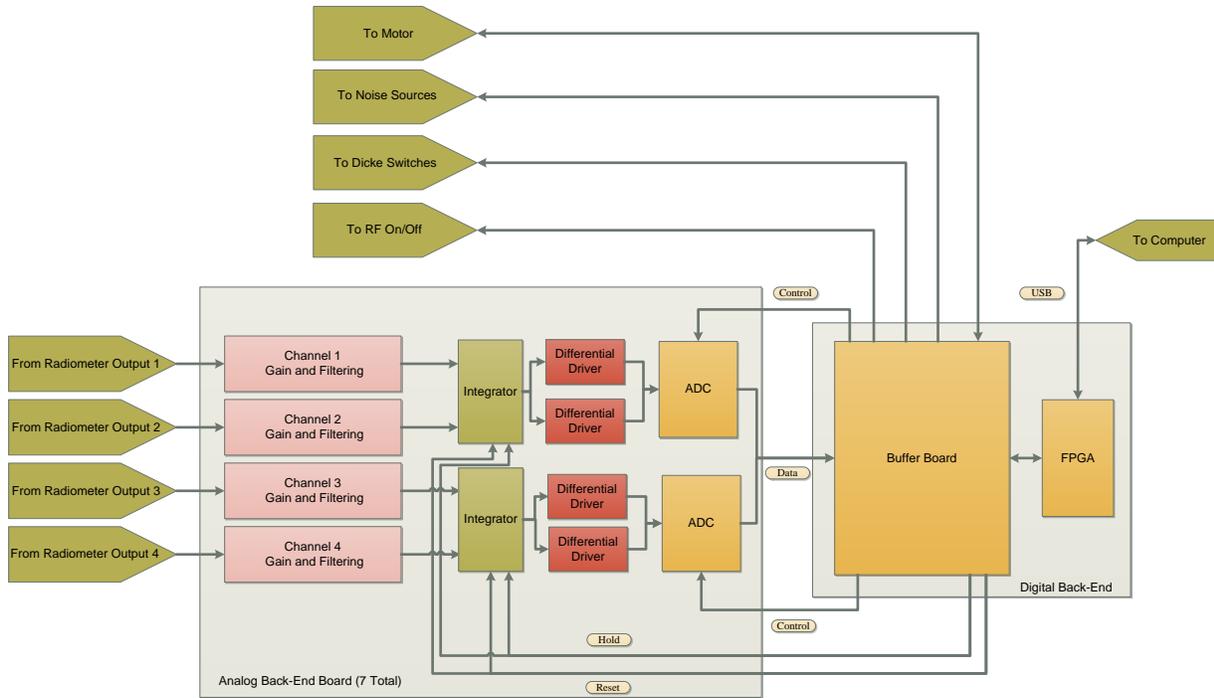


Figure 4-3: Block diagram of the analog back-end board

The analog back-end is controlled by the digital back-end, which consists of a BeMicro SDK FPGA by Altera and the buffer board, both of which are discussed in depth in Chapter 5 [18]. The FPGA controls, through the buffer board, the “Hold” and “Reset” signals of the integrator as well as the control signals for the ADC. All analog back-end control signals are timed with the radiometer control signals, noise source switches, Dicke switches, and Radio Frequency (RF) On/Off switches to ensure the synchronization of the entire radiometer system.

4.2 Input Connections

The analog back-end has surface-mount female Sub-Miniature A (SMA) jacks for input connections. These SMA connections were chosen to match the coaxial cable outputs of the Radiometer Front-End. The specific jacks being used are the 50 Ω PCB 5-1814400-1 SMA Jack from TE Connectivity [21]. These jacks are zinc alloy with gold plating and operate up to 3 GHz. An image of the analog back-end board with all four SMA jack inputs circled in red is shown in Figure 4-4.

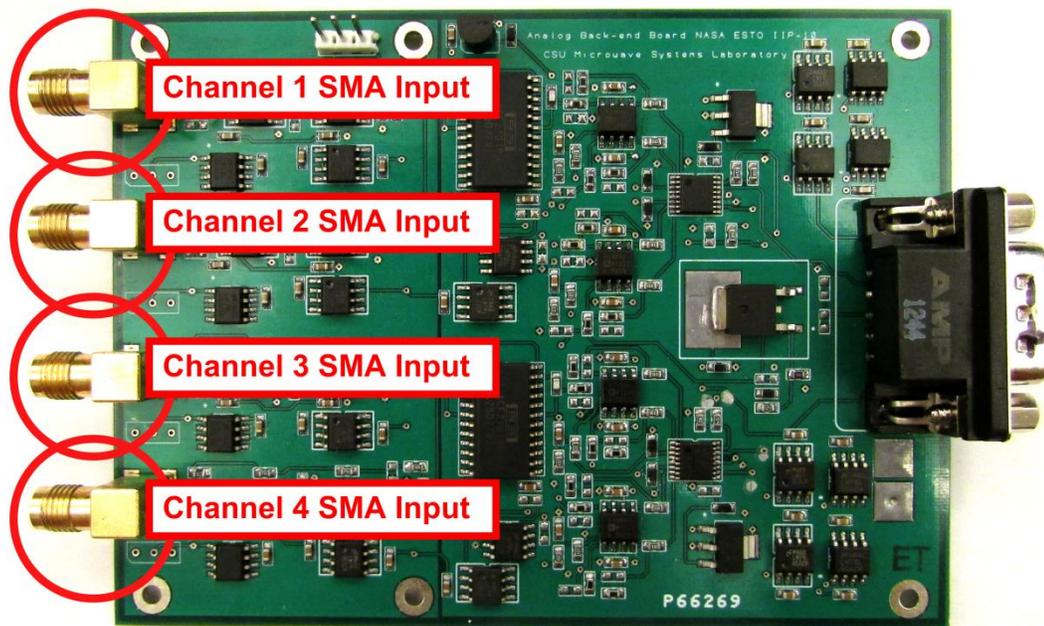


Figure 4-4: Analog back-end board with SMA jacks circled in red

4.3 Gain Stage

The gain stage is divided between two operational amplifiers and includes both passive and active filtering. A schematic of these stages is shown in Figure 4-5. First, the gain stages are

discussed, then the operational amplifier selection is explained, and finally the filtering options are analyzed. Note that Resistors R5 and R6 were included on the PCB for debugging reasons and are not used in the final design. Also the capacitors C1 and C2 are for filtering, as discussed in Section 4.3.3.

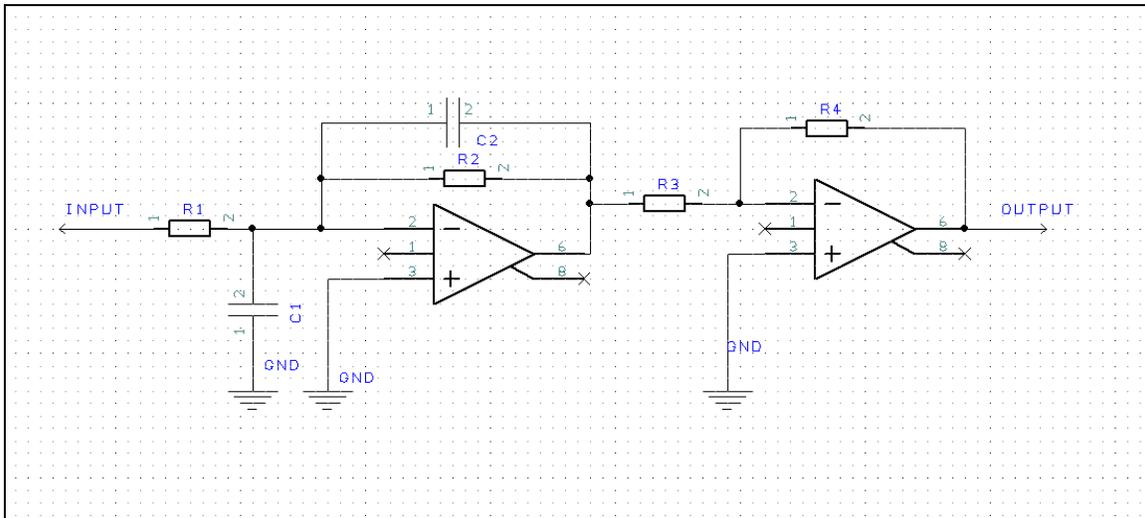


Figure 4-5: Single-channel gain stage schematic of the analog back-end board

The gain stage of the analog back-end board consists of two inverting amplifiers. Figure 4-6 is a general schematic of an inverting amplifier based on an operational amplifier.

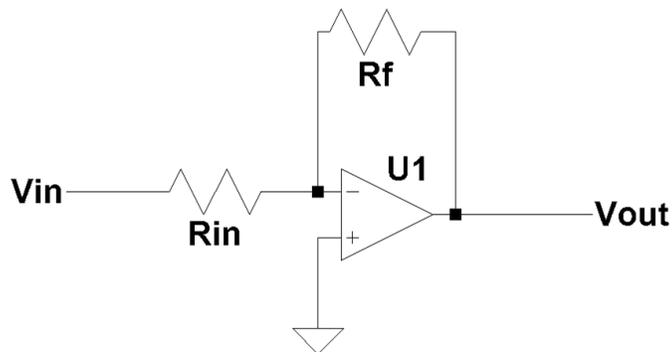


Figure 4-6: Nominal inverting amplifier schematic

The gain equation for an inverting amplifier is given in Equation 4-1 [22].

$$V_{out} = -V_{in} \left(\frac{R_f}{R_{in}} \right) \quad (4-1)$$

4.3.1 Gain Selection

Originally a gain of 4000 was estimated to be the maximum gain needed, so the gain was divided into two stages. The actual gain required for digitization has now been determined to be much lower than 4000. However, the analog back-end boards have maintained this high-gain capability. As explained more in depth in the following sections, the integrator also amplifies the signal, and the ADC requires a peak-to-peak input of 4.096 V to fully utilize its dynamic range. The gain of the integrator is given in Equation 4-2 [23].

$$V_{out} = -\frac{I_{in}\Delta t}{C_{int}} \quad (4-2)$$

Where:

- V_{out} is the maximum output voltage (V)
- C_{int} is the integration capacitance (F)
- I_{in} is the input current (A)
- Δt is the integration time (s)

Therefore, the resistor values of the gain stages, R1, R2, R3, and R4, from Figure 4-6 should be chosen to fit Equation 4-3, where the two gain stages and the integrator gain are taken into account. Note that integrator gain loses a negative sign since the signal is inverted with a differential driver after the integrator, as explained in Section 4.6.

$$4.096 V = -V_{in} \left(\frac{R_2}{R_1} \right) \left(\frac{-R_4}{R_3} \right) \left(\frac{I_{in} \Delta t}{C_{int}} \right) \quad (4-3)$$

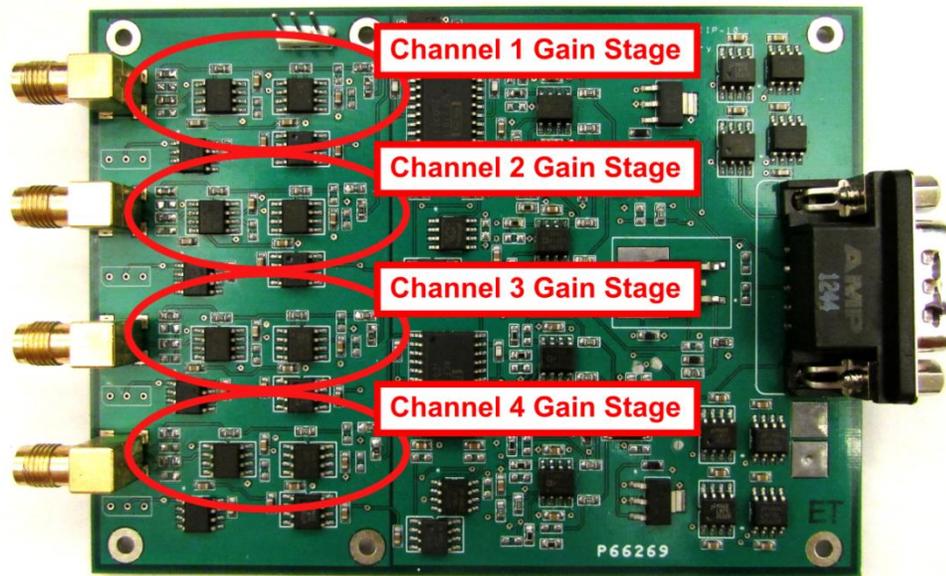
The resistances should be kept in the 1 k Ω to 20 k Ω range to keep current through the operational amplifiers at a reasonable level.

4.3.2 Op-Amp Selection

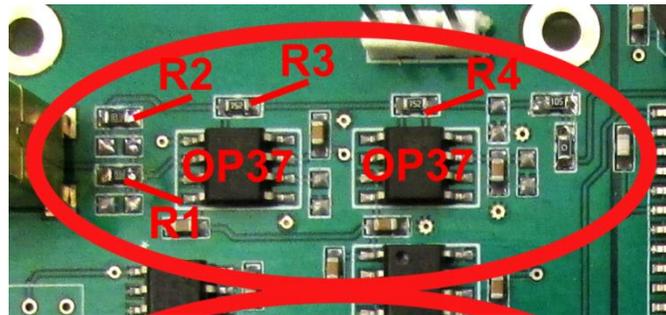
The operational amplifier used in the gain stage was chosen based on the heritage of the JPL High Altitude Monolithic Microwave Integrated Circuit (MMIC) Sounding Radiometer (HAMSR). HAMSR used OP27 [24] operational amplifiers from Analog Devices in the design. However, for the analog back-end board the operational amplifier was updated to the OP37 [25] because it has a higher gain-bandwidth product. The performance characteristics of the OP37 are as follows:

- Low noise, 80 nV peak-peak (0.1 Hz to 10 Hz) 3nV
- Low drift, 0.2 $\mu\text{V}/^\circ\text{C}$
- High speed, 17 V/ μs slew rate 63 MHz gain bandwidth
- Low input offset voltage, 10 μV
- Excellent common mode rejection ratio, 126 dB (common-voltage @ 11V)
- High open-loop gain, 1.8 million

The OP37 is available in as a 8-pin Small-Outline Integrated Circuit (SOIC8) footprint which is the package used in the analog back-end board design. The SOIC8 OP37 packages and gain stages of all four channels are circled in red in Figure 4-7 (a) while a single-channel gain stage is labeled in Figure 4-7 (b).



(a)



(b)

Figure 4-7: Analog back-end board (a) gain stages of all four channels circled in red and (b) labeled single-channel gain stage

4.3.3 Filtering Capabilities

The first gain stage includes the option for both a passive and an active low-pass filter to remove any noise in the bandwidth of interest that may get coupled in to the coaxial cable that connects

the front-end to the analog back-end board in the instrument. Figure 4-8 shows a schematic of the filter stage.

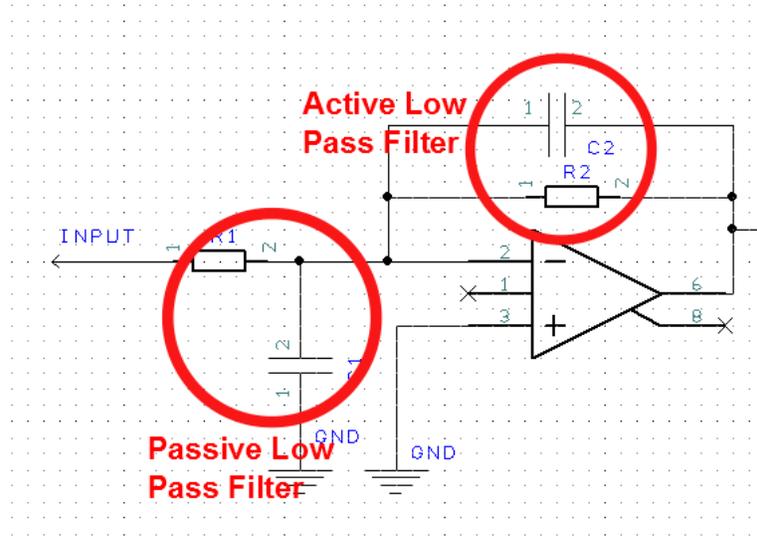


Figure 4-8: Schematic of both passive and active low-pass filters of a single-gain stage on the analog back-end board

The passive filter cutoff frequency is given by Equation 4-4 [22].

$$f_{c1} = \frac{1}{2\pi R_1 C_1} \quad (4-4)$$

The while the active filter cutoff frequency is given by Equation 4-5 [22].

$$f_{c2} = \frac{1}{2\pi R_2 C_2} \quad (4-5)$$

These filters are optional and can be used to filter out noise from the entire instrument, aircraft, and radio signals that may be introduced during test flights. This noise is not present in laboratory settings, so the filters were not included while testing the functionality of each board.

4.4 Integrator

As discussed in Section 2.4, a switched capacitor integrator was needed in the analog back-end board. A switched capacitor integrator converts input current to output voltage through integration using an integration capacitor. This capacitor holds a charge until it is reset by triggering a switch that dumps the charge on the capacitor to ground [23]. Figure 4-9 shows the integrators circled in red.

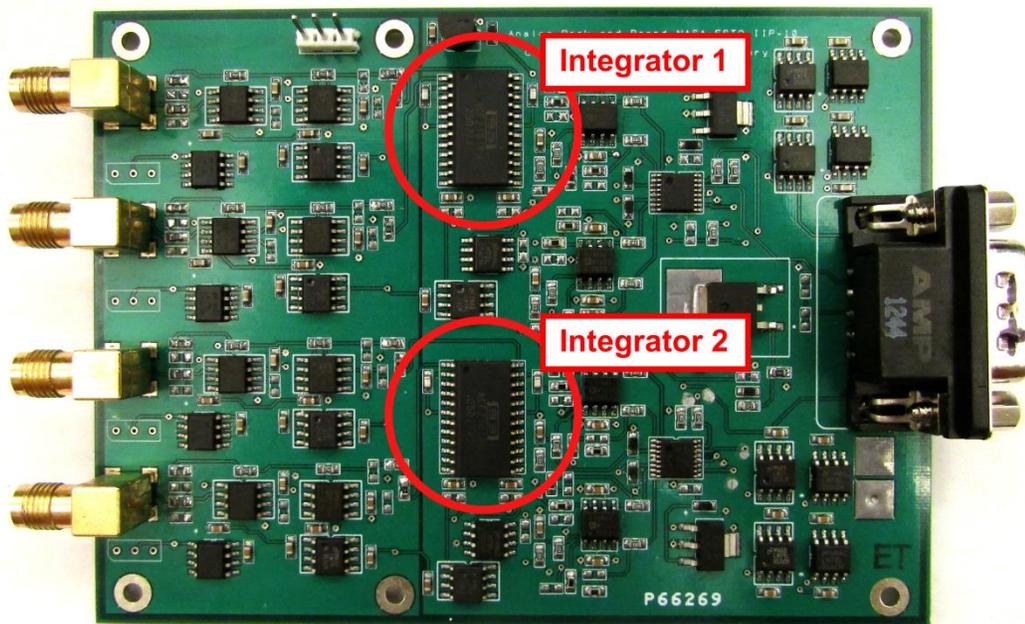


Figure 4-9: Integrators on the analog back-end board circled in red

4.4.1 Integrator Control and Layout

For integration the Burr-Brown ACF2101 Low Noise Dual Switched Integrator [23] was used because it is the only switched capacitor integrator available packaged as an integrated circuit. A schematic image of the integrator is shown in Figure 4-10.

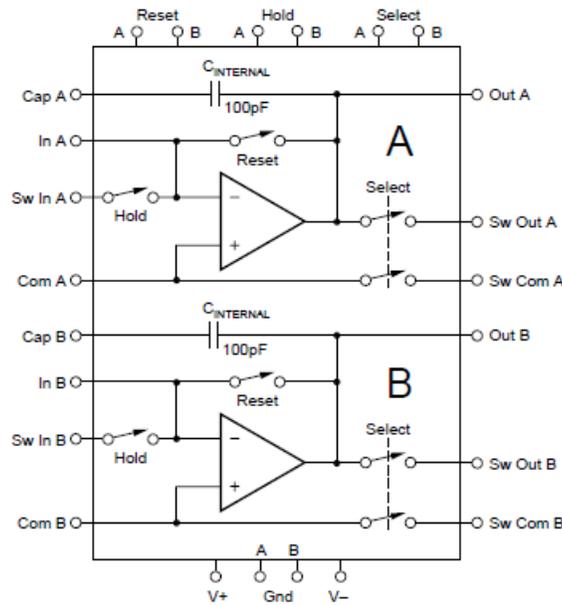


Figure 4-10: Schematic of Burr-Brown ACF2101 low noise dual switched integrator [23]

The ACF2101 has three control signals: “Reset”, “Hold”, and “Select”. The “Reset” switch is used to discharge the integration capacitor before the next integration period. The “Hold” switch disconnects the input current and holds the output at a fixed level. The “Select” switch is used to turn on and off the outputs of the integrator. The “Select” signal was set to logic one or 3.3 V while the “Reset” and “Hold” signals were timed based on the following timing diagram. Figure 4-11 shows the timing diagram recommended on the ACF20201 datasheet.

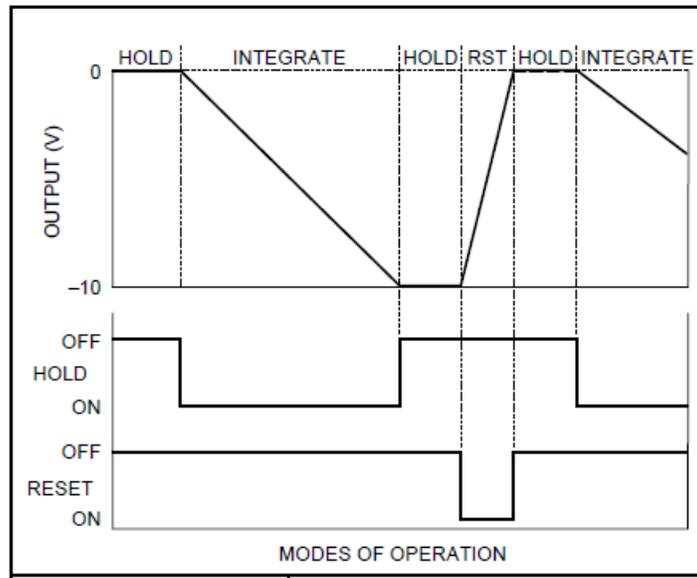


Figure 4-11: Suggested timing diagram for AC2101 [23]

For the analog back-end board, a “Reset” time of 8 μ s seconds and a “Hold” time of 4 μ s were used. Figure 4-12 is diagram of the actual timing used for the analog back-end board.

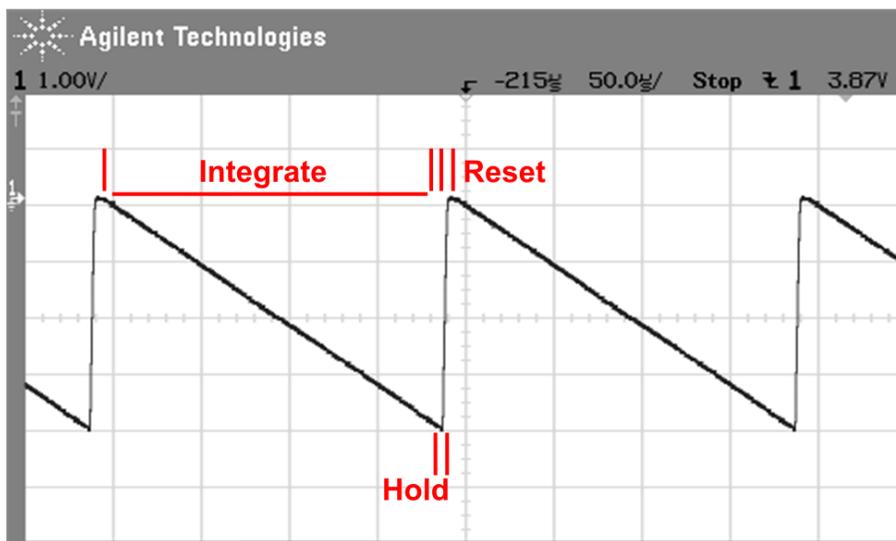


Figure 4-12: Oscilloscope measurement of output of the AC2101 switch capacitor integrator with integrate, hold, and reset signals labeled

An integration capacitor was chosen to match a “Reset” time of 8 μs . Figure 4-13 shows a comparison of recommended integration capacitor value versus “Reset” time from the ACF2101 datasheet [23]. With a “Reset” time of 8 μs , the integration capacitor should have a value of approximately 200 pF.

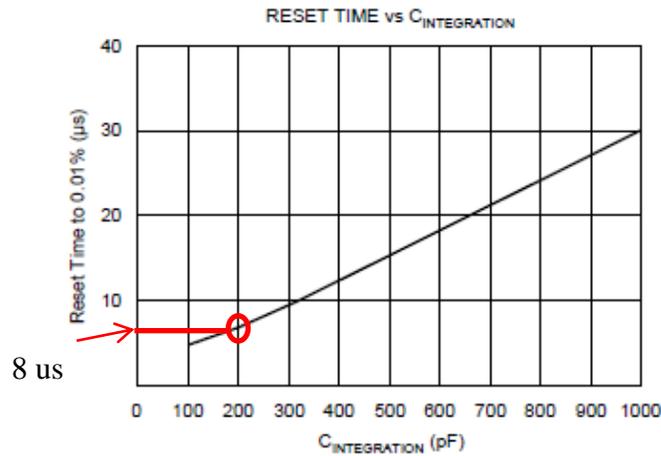


Figure 4-13: Reset time vs. integration capacitance for the ACF2101 [23]

The internal integration capacitance of ACF2101 is only 100 pF, so the external integration capacitance configuration was used per the ACF2101 datasheet. Figure 4-14 shows the schematic of this configuration.

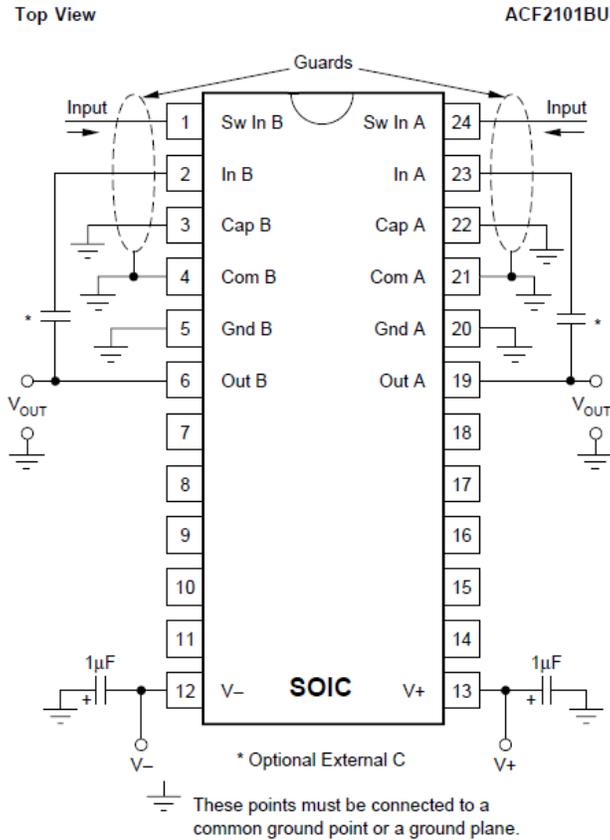


Figure 4-14: ACF2101 schematic for external integration capacitors [23]

As stated in Section 4-3, the gain of the integrator is given by Equation 4-5 [23].

$$V_{out} = -\frac{I_{in}\Delta t}{C_{int}} \quad (4-5)$$

Where:

- V_{out} is the maximum output voltage (V)
- C_{int} is the integration capacitance (F)
- I_{in} is the input current (A)
- Δt is the integration time (s)

To fully utilize the dynamic range of the ADC, which is discussed later, a V_{out} of 4.096 V is needed. Knowing that the minimum integration time, Δt , is 0.1 ms and using the integration capacitance and Equation 4-5, the input current I_{in} needed is approximately 8 μA . This can be achieved by using an input resistance of approximately 1 M Ω . This resistance value was determined empirically through trial and error.

4.5 Analog-to-Digital Converter

After the integration stage of the analog back-end board, the signal is digitized. An analog-to-digital converter was chosen, and a differential driver was chosen to be suitable for this particular ADC and added. Figure 4-15 shows the ADCs on the analog back-end board circled in red.

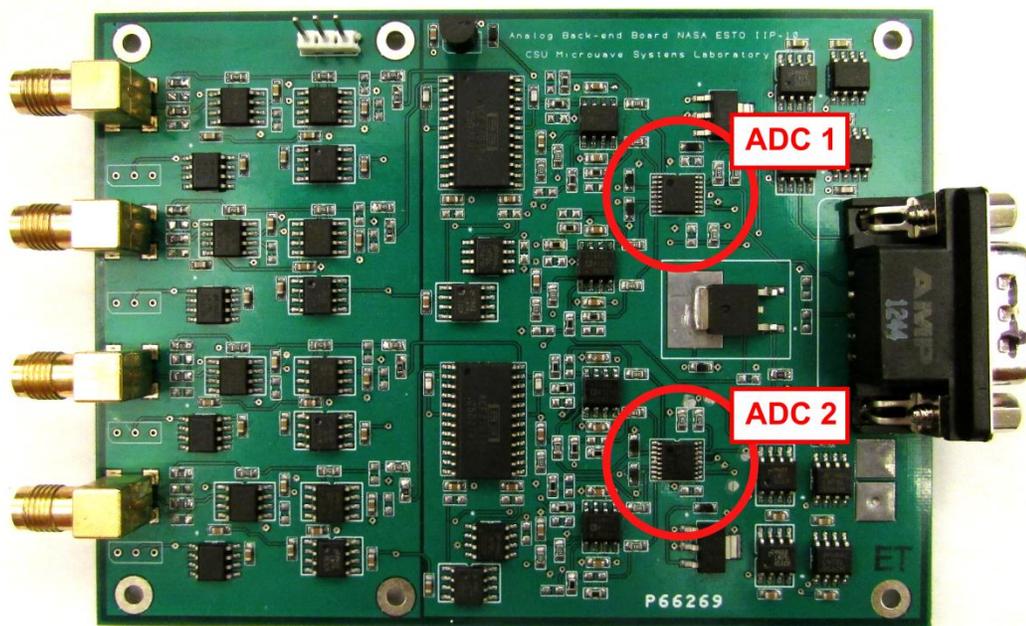


Figure 4-15: Analog-to-digital converters on the analog back-end board circled in red

4.5.1 Analog-to-Digital Converter Selection

The ADC was chosen according to the following criteria:

- Required simultaneous sampling
- Required ADC resolution of greater than or equal to 14 bits
- Minimum amount of control, power, and data signals
- Straight-forward Serial Protocol Interface (SPI) for easy data access

The requirement of simultaneous sampling was based on the science requirements of this airborne radiometer. The requirement of a single DE-9 requirement was assumed, based on the fact that eight of these boards will be used, so a simple “plug-and-play” design was preferable.

Based on the criteria given above, the AD7357 Differential Input, Dual, Simultaneous Sampling, 4.2 Mega-Samples per Second (MSPS), 14-bit, Successive Approximation Register (SAR) Analog-to-Digital Converter from Analog Devices was chosen [26]. Two AD7357 are used per Analog back-end board. Figure 4-16 shows a functional block diagram of the AD7357.

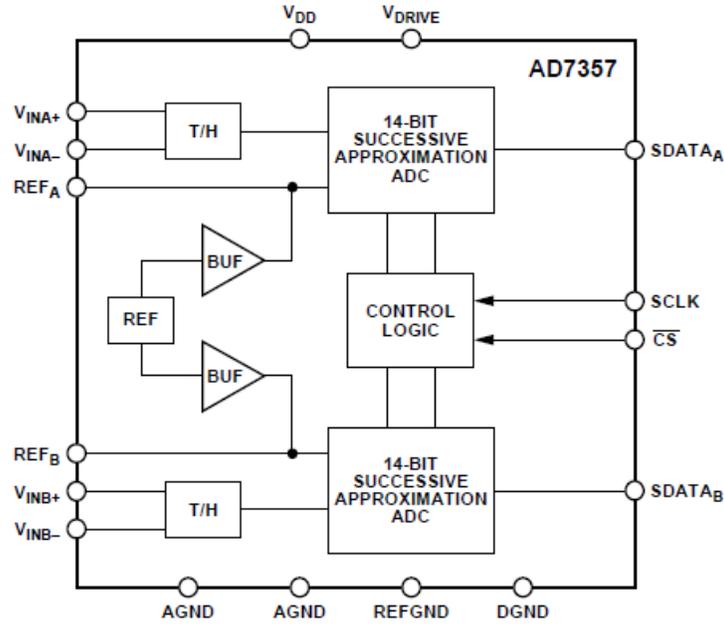


Figure 4-16: Functional block diagram of the AD7357 [26]

4.5.2 Analog-to-Digital Converter Operation

The ADC is operated in what the AD7357 datasheet refers to as “Normal Mode” where both data outputs are on the same trace. Figure 4-17 shows the timing diagram of this “Normal Mode.” The Chip Select (CS) selects when the ADC is actually sampling, and Serial Protocol Interface Clock (SCLK) provides timing for the serial output of the ADC.

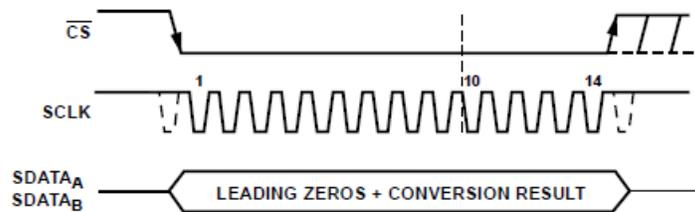
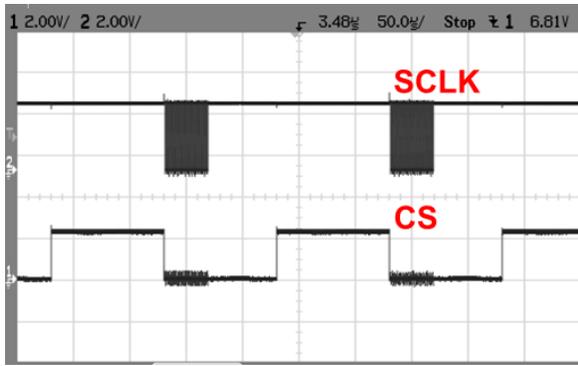
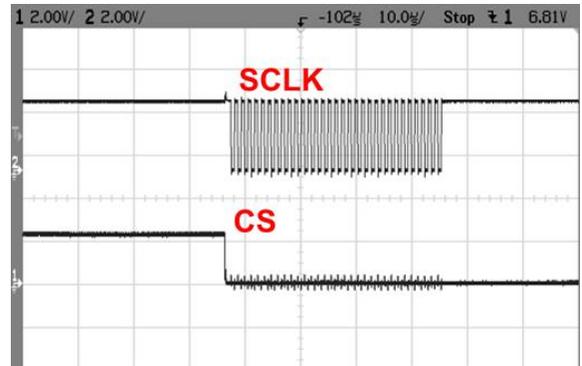


Figure 4-17: “Normal Mode” of Operation of AD7357 [26]

Figure 4-18 (a) and (b) are the oscilloscope output of the times of CS and SCLK transition at 50 μ s per division and 10 μ s per division time scales, respectively.



(a)



(b)

Figure 4-18: Oscilloscope outputs of (a) SCLK and CS at 50 μ s per division and (b) 10 μ s per division

4.6 Differential Driver

According to the datasheet of the AD7357, the AD8138 [27] differential driver from Analog Devices is recommended to convert the single-ended signals to differential signals for the AD7357. In Figure 4-19 the differential drivers on the analog back-end board are circled in red.

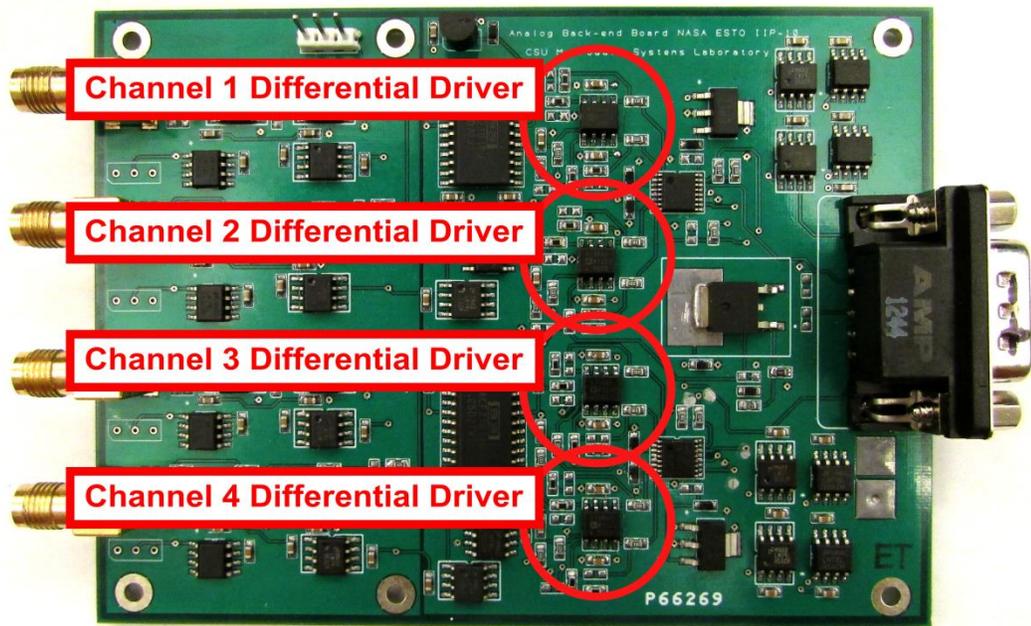


Figure 4-19: Differential drivers of analog back-end board circled in red

Figure 4-20 is a typical application circuit for the AD8138 driving the AD7357. However, this application circuit was modified to accommodate the output of the integrator, which has a maximum output range of 0 to -4.096 V rather than the nominal output of -2.048 V to +2.048 V.

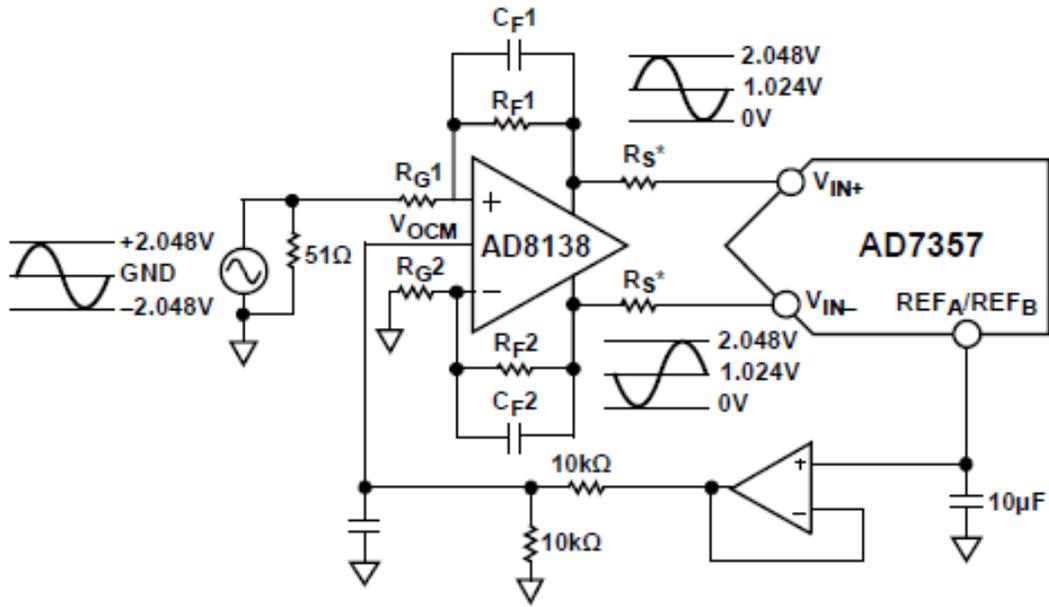


Figure 4-20: Suggestion application circuit for the AD7357 and AD8138 [27]

To use the maximum range of the ADC with an 0 to -4.096 V input into the differential driver, the design was modified by tying the ground node connected to R_{G2} to -2 V. Also, the unity gain buffer used for back current protection purposes was removed due to space constraints. The schematic of the modified circuit used is shown in Figure 4-21.

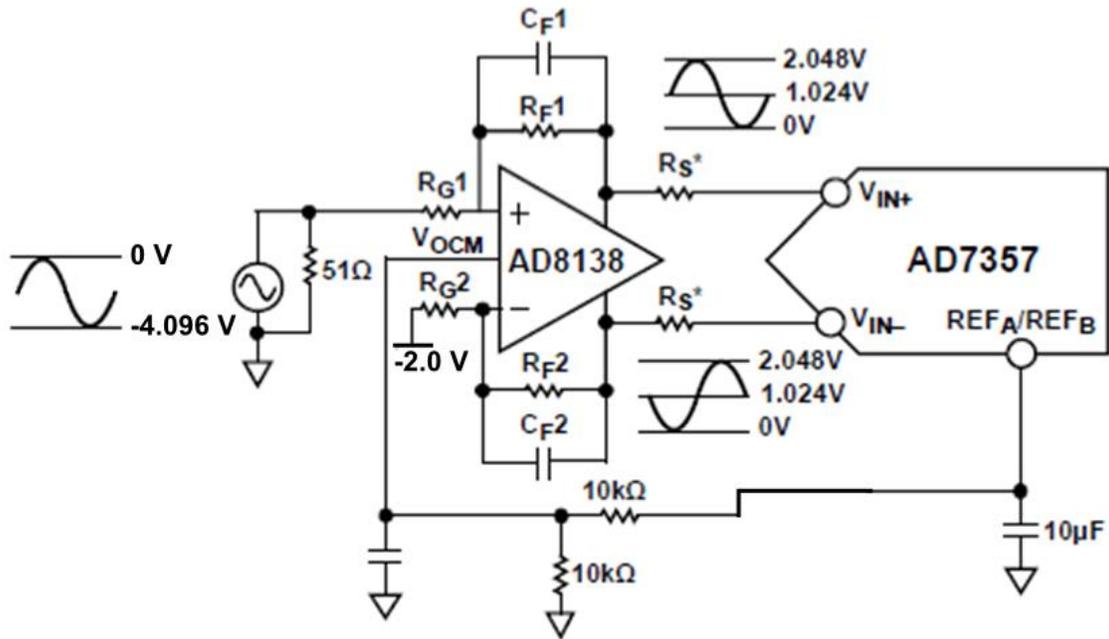


Figure 4-21: Modified AD7357 and AD8138 schematic [27]

A series of simulations, shown below, were used to understand the phenomenon associated with different inputs into and different offsets on a differential driver. These simulations were conducted using Linear Technologies Simulation Program with Integrated Circuit Emphasis (LTspice) [28]. The input for all simulations was a 1 kHz sine wave. Figure 4-22 shows the LTspice model used for the simulation.

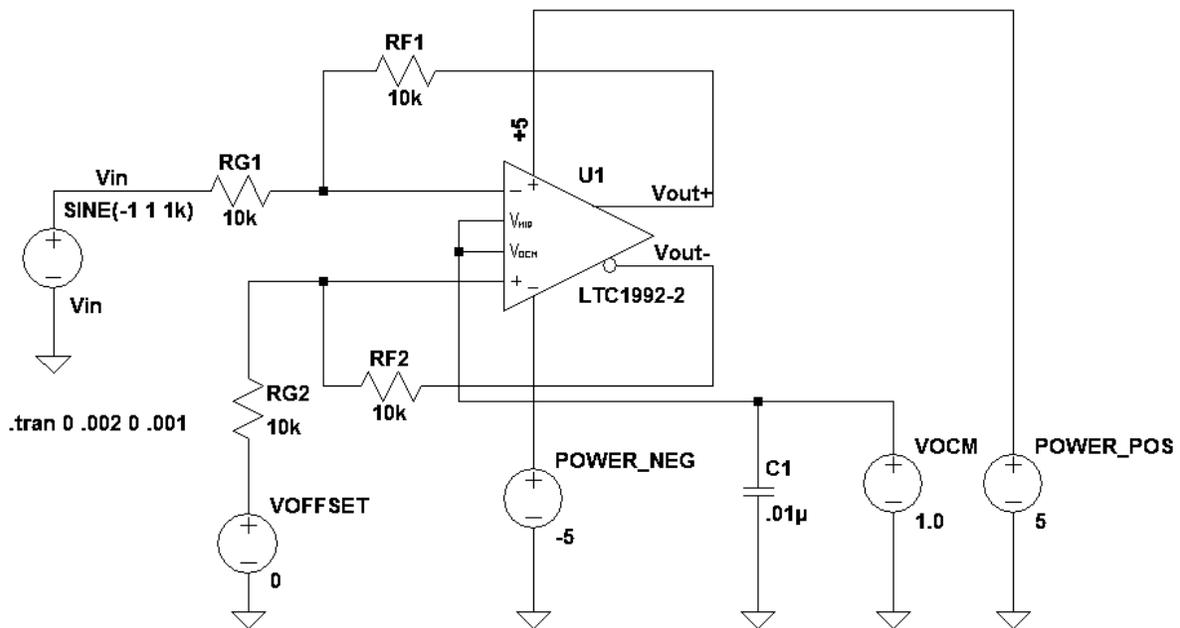


Figure 4-22: Schematic used in LTspice Simulation

First, a nominal scenario, suggested in the AD7357 datasheet and shown in Figure 4-21, was modeled. Figures Figure 4-23 and Figure 4-24 show the simulation results with inputs of 2 V and 4 V peak-to-peak with no offset and the corresponding offsets, respectively.

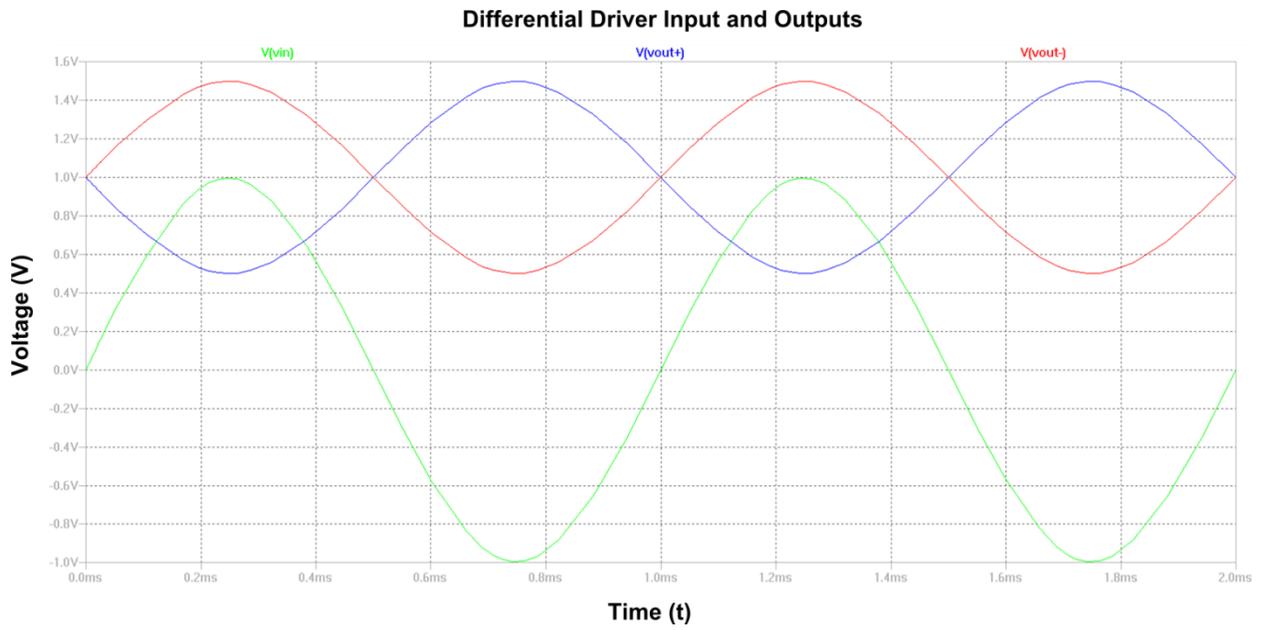


Figure 4-23: Differential driver response with 2 V peak-to-peak input and zero offset input

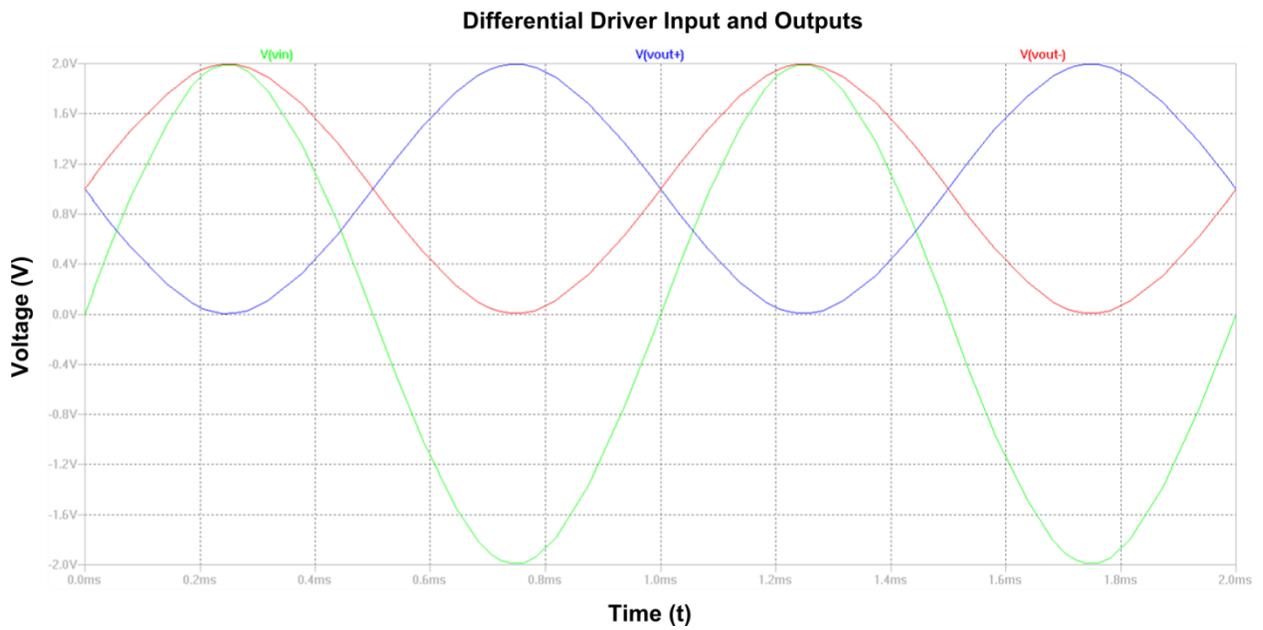


Figure 4-24: Differential driver response with 4 V peak-to-peak input and zero offset input

The magnitudes of the outputs are half the magnitude of the input and have an offset of 1 V. This allows a 4.096 V single-ended peak-to-peak input to have a 2.048 V differential peak-to-peak output that can utilize the maximum range of the AD7357 of 2.048 V.

Next, an input to the differential driver with similar voltages to the output of the integrator is simulated. Figures Figure 4-25 and Figure 4-26 show the simulation results of 0 to -2 V and 0 to -4 V inputs and their corresponding outputs, respectively.

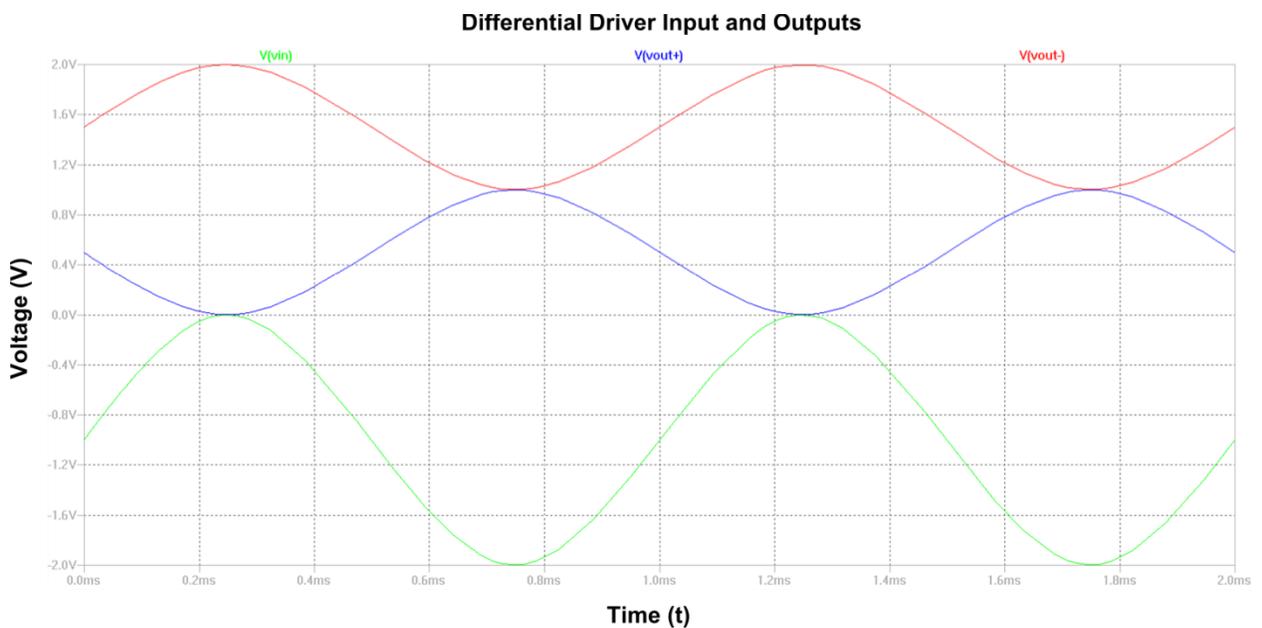


Figure 4-25: Differential driver response with 0 to -2 V input

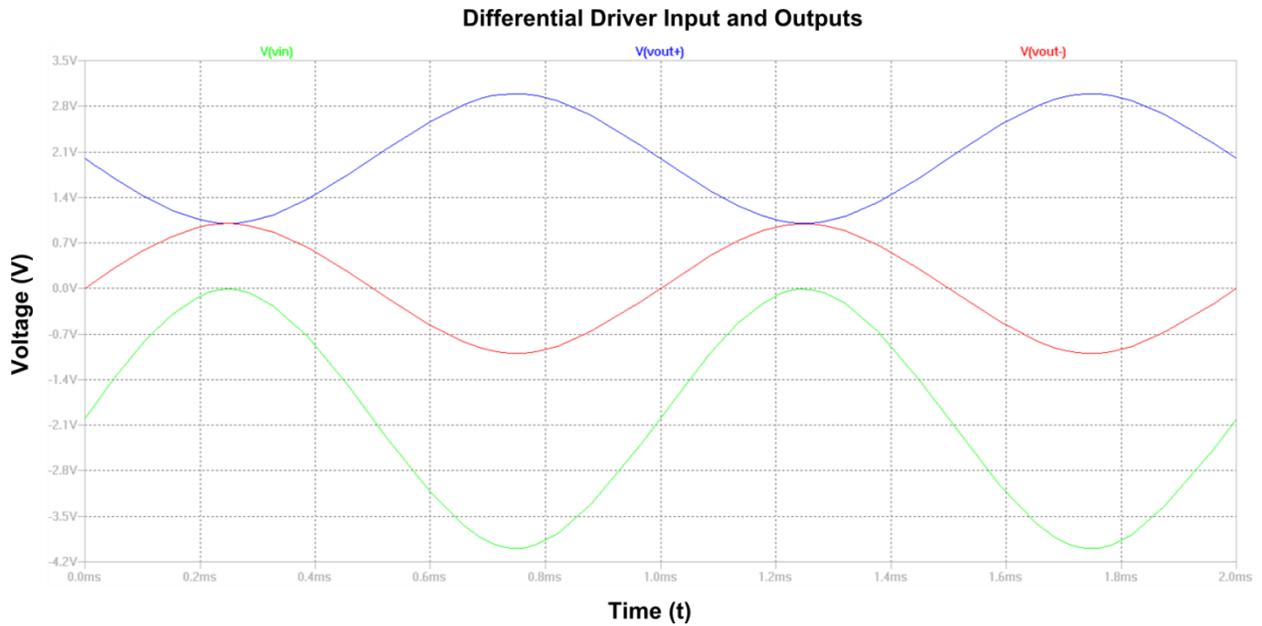


Figure 4-26: Differential driver response with 0 to -4 V input

With the 0 to -2 V input, the differential outputs are still less than the maximum input range of the AD7357. However, with the 0 to -4 V input, the differential outputs are no longer in the maximum input range of the AD7357.

Now the 0 to -2 V and 0 to -4 V inputs are used again, but the differential driver has a (note the negative) -2 V offset applied to R_4 (R_{G2} in the AD7357 schematic). Figures Figure 4-27 and Figure 4-28 show the simulation results of 0 to -2 V and 0 to -4 V inputs with the -2 V offset applied to the differential driver and corresponding outputs, respectively.

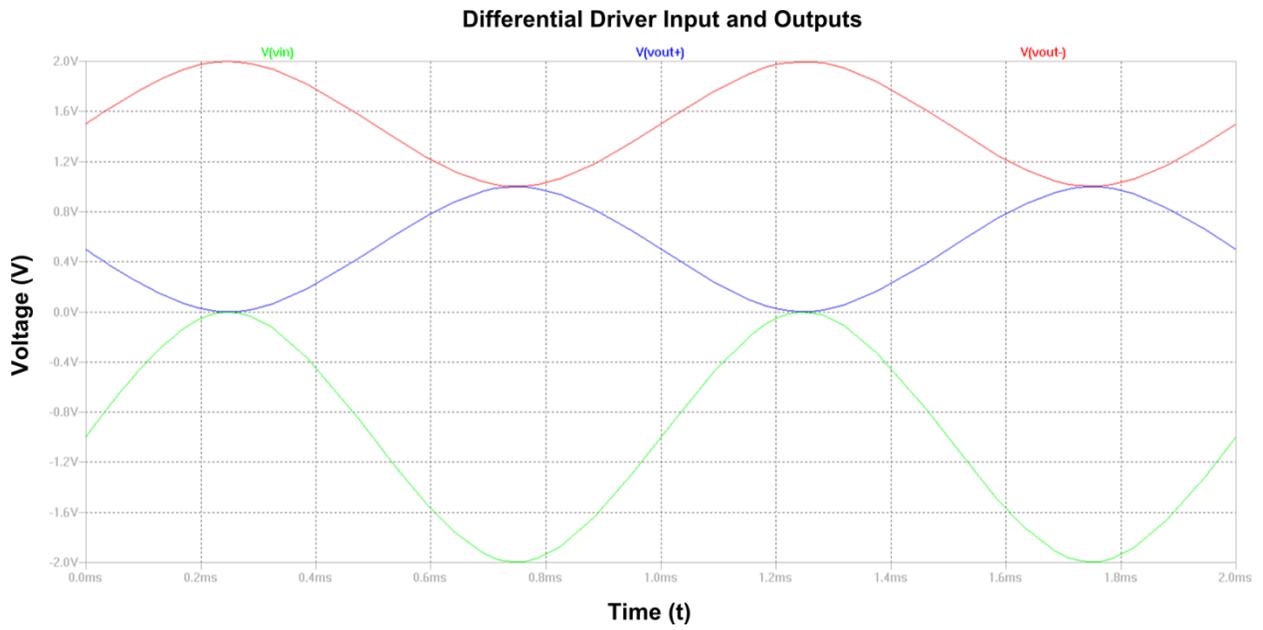


Figure 4-27: Differential driver response with 0 to -2 V input and -2 V offset applied to R_{G2}

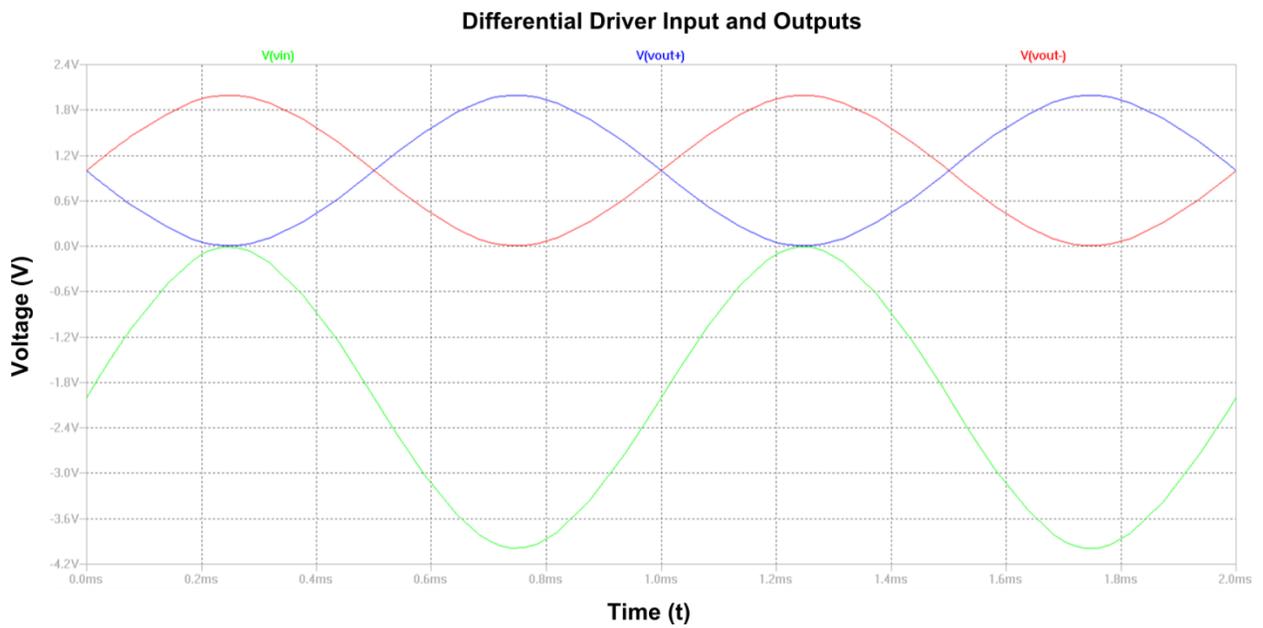


Figure 4-28: Differential driver response with 0 to -4 V Input and -2 V offset applied to R_{G2}

With this -2 V offset, the differential outputs are within the maximum range of the AD7357 when the inputs are at both 0 to -2 V and 0 to -4 V. Although this meets the dynamic range requirements of the AD7357, this output scenario differs slightly from the scenarios in the suggested schematics in Figures 4-23 and 4-24. The suggested schematic produces outputs centered on a 1 V offset, while the modified schematic produces a negative differential output anchored at 2 V and a positive differential output anchored at 0 V, so the AD7357 will give a negative output of the input signal. Figures Figure 4-29 and Figure 4-30 show the oscilloscope readings of the differential driver output with both a 0 to -2 V input and a 0 to -4 V input.

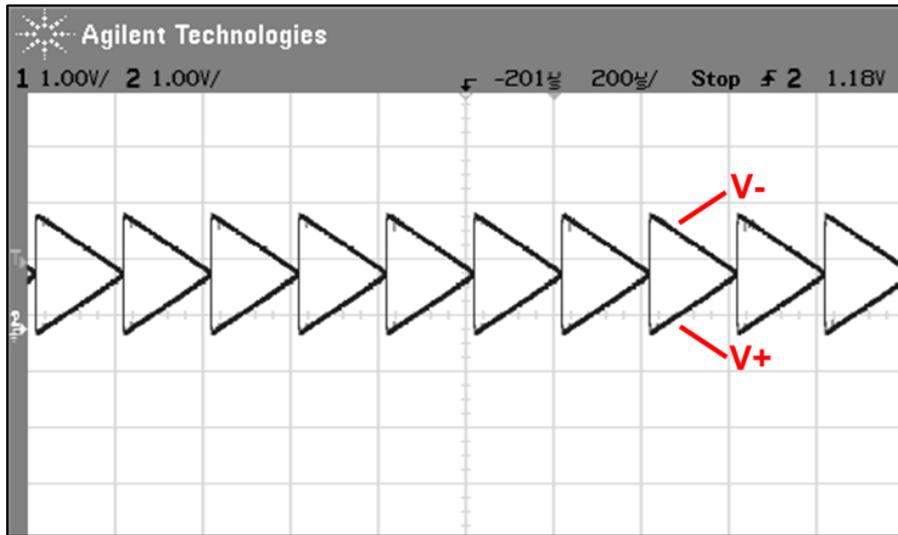


Figure 4-29: Differential driver response with 0 to -2 V input and -2 V offset applied to R_{G2}

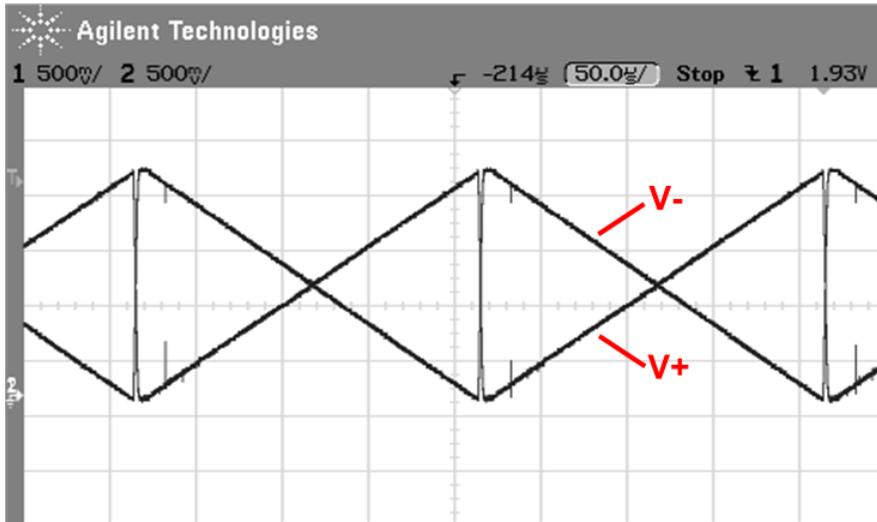


Figure 4-30: Differential driver output response with 0 to -4 V input and -2 V offset applied to R_{G2}

4.7 FPGA Control and Interface

Each analog back-end board is controlled by a BeMicro SDK FPGA [18] which is interfaced through the buffer board. Both the FPGA and the buffer board will be discussed in depth later. The interface connection with the FPGA controls is a DE-9 Connector which is shown circled in red in Figure 4-31.

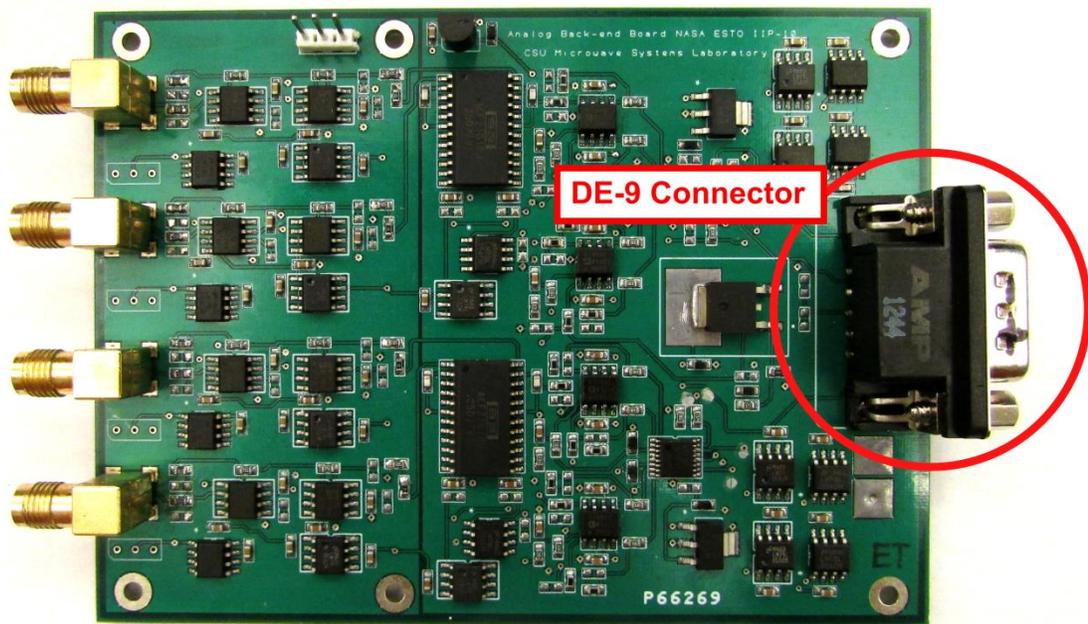


Figure 4-31: DE-9 connector on the analog back-end board circled in red

Also, each analog back-end board is supplied power and outputs data through the DE-9 connector. The layout of the DE-9 connector is shown in Figure 4-32.

DATA A	5	9	SPI
CS	4	8	POWER NEG
DIG GND	3	7	POWER POS
RESET	2	6	DATA B
HOLD	1		

Figure 4-32: DE-9 output connections from analog back-end board

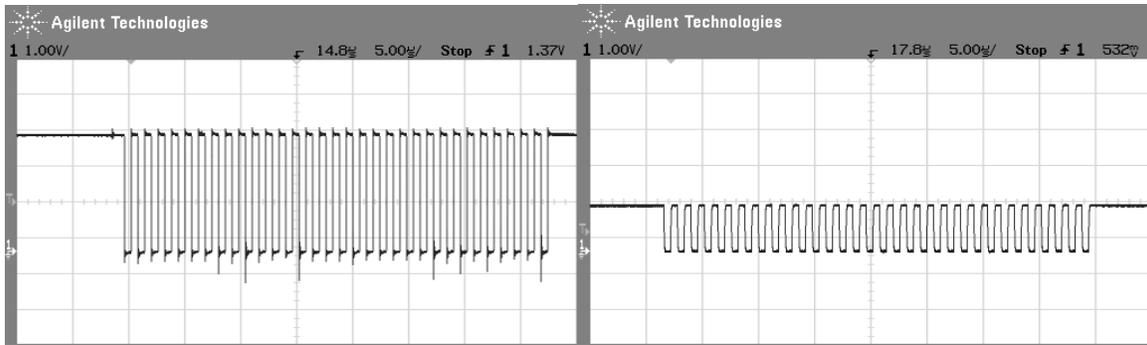
4.7.1 SPI Clock Interface

Originally a 33 Ω resistor was placed in series with the SPI Clock (SCLK) signal to minimize reflections from the high-speed signal [29]. However, communication issues still existed even with the 33 Ω resistor in series. This is because the SCLK signal from the FPGA has a maximum output voltage of 3.3 V, while the AD7357 has a maximum SPI clock input voltage of 2.4 V. To adjust the voltage level of the SCLK signal, a voltage divider was also added before the input to the ADC. Figure 4-33 is a schematic of the voltage divider. Note that voltage divider overrides the 33 Ω impedance.



Figure 4-33: SCLK voltage divider schematic

Figure 4-34 is an image of the SCLK signal measured with an oscilloscope before (a) and (b) after the voltage divider.



(a)

(b)

Figure 4-34: Oscilloscope reading of the SCLK output (a) before and (b) after the voltage divider circuit

4.7.2 Integrator Control Signals

The integrator is controlled by a 3.3 V logic level signals from the digital back-end. Figure 4-35 shows the “Hold” (Top) and “Reset” (Bottom) signals controlling the integrator.

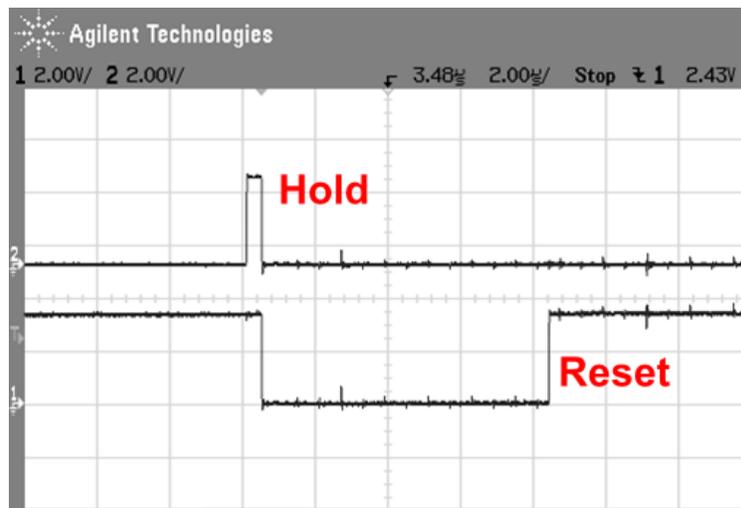


Figure 4-35: “Hold” (top) and “Reset” (bottom) control signals for the analog back-end board

The signal is sampled while the integrator “Hold” signal is triggered. Figure 4-36 shows the timing of the integrator output with the “Hold” signal at (a) 100 μ s per division and (b) 2 μ s per division.

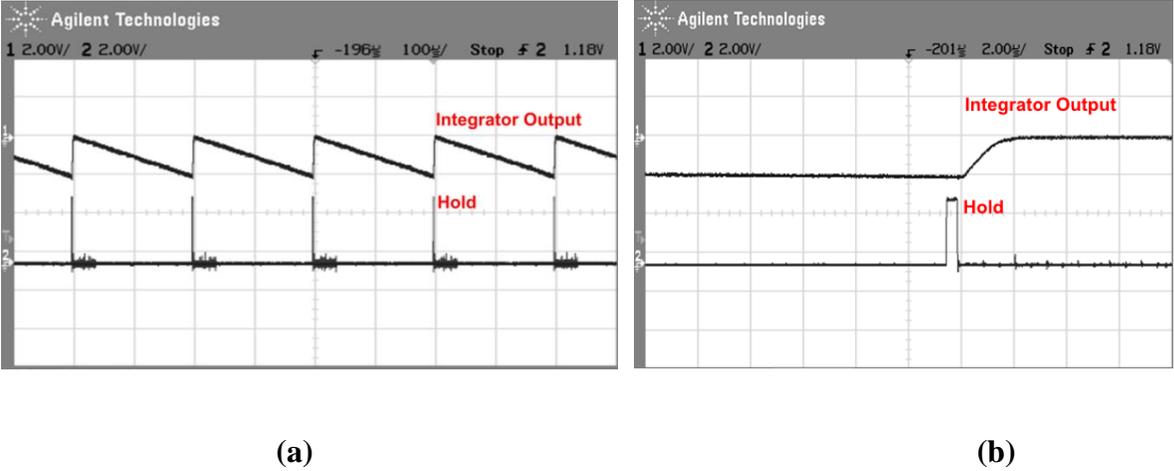


Figure 4-36: Oscilloscope timing of the integrator output with the “hold” signal at (a) 100 μ s per division and (b) 2 μ s per division

4.7.3 Data Output

The AD7357 has a 14-bit output, as shown in Figure 4-37.

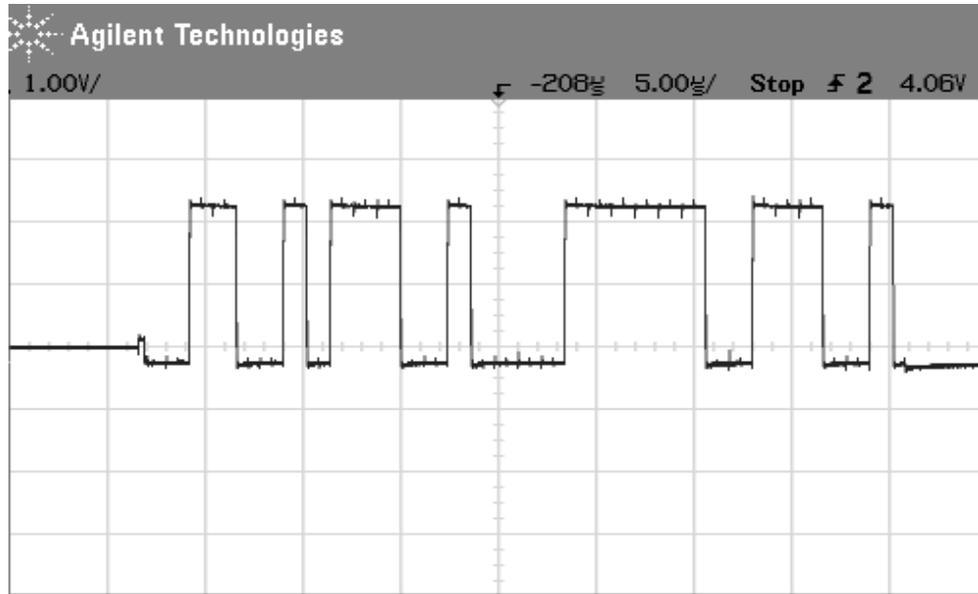


Figure 4-37: Oscilloscope reading of the AD7357 14-bit output

4.8 Voltage Regulation

To minimize cross-talk between channels and reduce noise between components, each integrated circuit on the analog back-end board was given its own voltage regulator. Figure 4-38 shows the analog back-end board with all voltage regulators labeled. In total, each analog back-end board consumes 190 mA at + 12 V and 180 mA at – 12 V, for a total of 4.4 W.

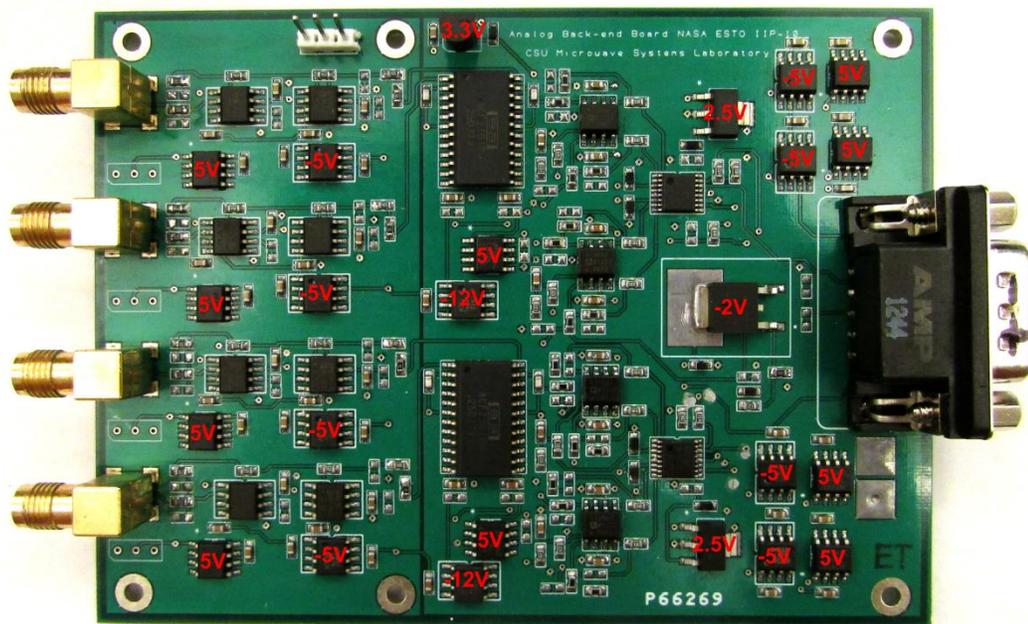


Figure 4-38: Analog back-end board with voltage regulators labeled in red

Each voltage regulator has input and output decoupling capacitors. Table 4-1 shows a list of the voltage regulator, input decoupling capacitor and output decoupling capacitor for each voltage level.

Table 4-1: Voltage regulator models and decoupling capacitors used on the analog back-end board

Voltage Level	Regulator Model	Input Capacitor	Output Capacitor
5 V	LM78L05 [30]	0.1 μ F Ceramic	0.1 μ F Ceramic
-5 V	LM79L05 [31]	0.1 μ F Ceramic	0.1 μ F Ceramic
-12 V	LM79L12 [31]	0.1 μ F Ceramic	0.1 μ F Ceramic
3.3 V	LP2950 [32]	0.1 μ F Ceramic	10 μ F Tantalum
2.5 V	LM2937 [33]	0.1 μ F Ceramic	10 μ F Tantalum
-2 V	LM337 [34]	0.1 μ F Ceramic	1 μ F Tantalum

4.9 Test Results

Every channel of every analog back-end board was tested to ensure that the boards function properly. Three tests were conducted; the first to determine the noise of the board, the second to determine the linearity of the board, and the third to quantify the standard deviation of noise as a function of the gain of the board. The first two tests were conducted by injecting the same signal into the input of all four channels simultaneously. These tests were conducted on all analog back-end boards, and all boards produced similar results. For convenience, the test results of just one analog back-end board are presented.

These tests were set up by connecting four Bayonet Neill–Concelman (BNC) connector coaxial cables to the analog back-end board via SMA-to-BNC adapters to the analog back-end board. This test setup is shown in Figure 4-39.

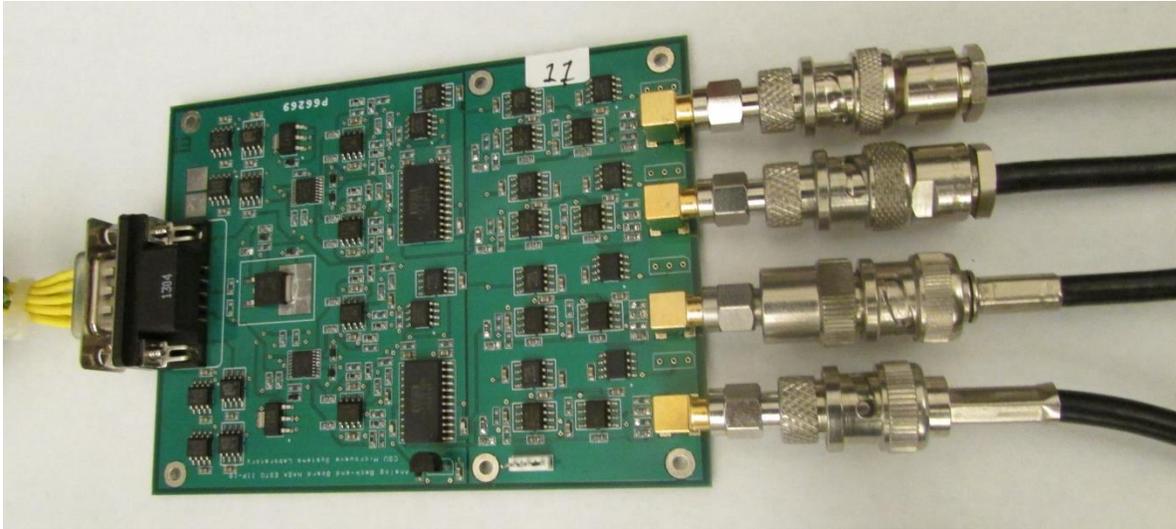


Figure 4-39: Test set up for noise and linearity tests

4.9.1 Noise Test

The noise test was to determine whether the noise added by the analog back-end board was similar to the expected standard deviation, in counts, of the ADC. The AD7357 has an expected standard deviation of approximately 2 counts. Thus if the output of the analog back-end board can output a signal with a standard deviation approximately 2 counts the assumption can be made that the noise introduced by stages previous to the ADC on the analog back-end board is less than the noise that can be measured by the ADC. An Agilent E3610A [35] DC power supply was used to provide a DC signal to the coaxial cables using BNC T-jacks, as shown in Figure 4-40.

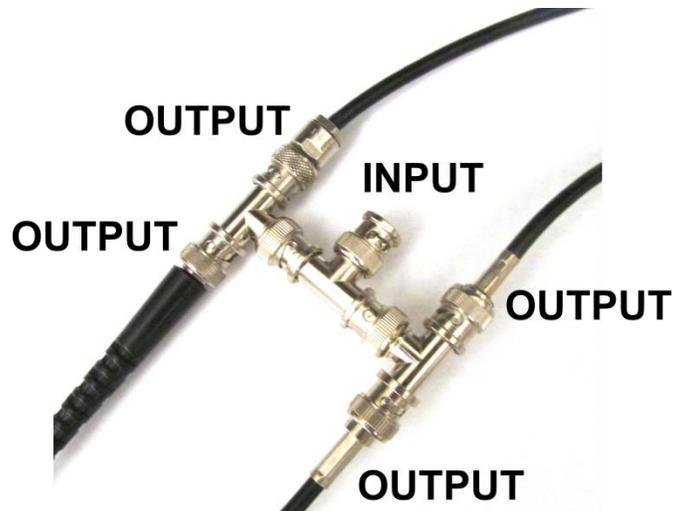


Figure 4-40: BNC T-connection setup used for noise and linearity tests

The gain of every channel on the analog back-end board was set to 2, and data was collected for approximately 3000 samples. The output signal from the Agilent E3610A power supply was set to 1 V. An oscilloscope reading of the signal is shown in Figure 4-41.

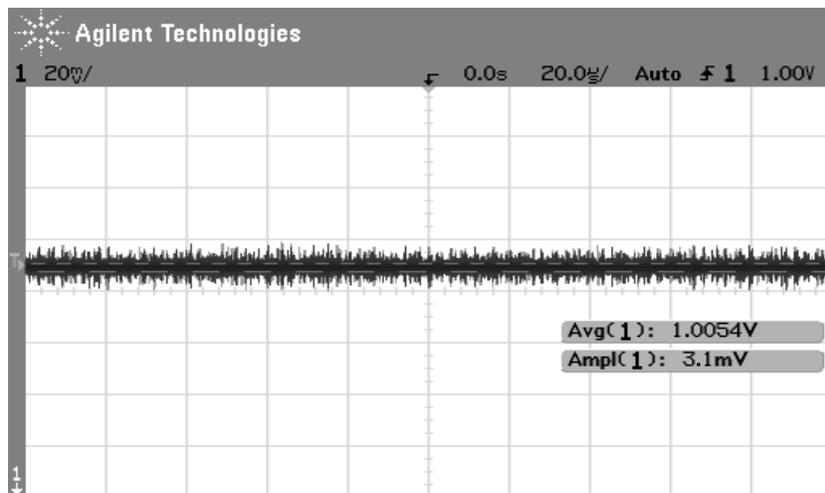


Figure 4-41: Input signal used for the noise test on the analog back-end board

The data from the output of the ADC was recorded, and the standard deviation of the counts was calculated using Matlab. A script for this calculation is available in Appendix IV, entitled

Matlab Script for Analog Back-End Board Tests. Figure 4-42 is a plot of the recorded output signal from the analog back-end board along with the standard deviation of the counts. Note that the first two counts of output are disregarded in the standard deviation calculation. Also note that Channel 2 is zoomed in to show the fluctuation of the signal.

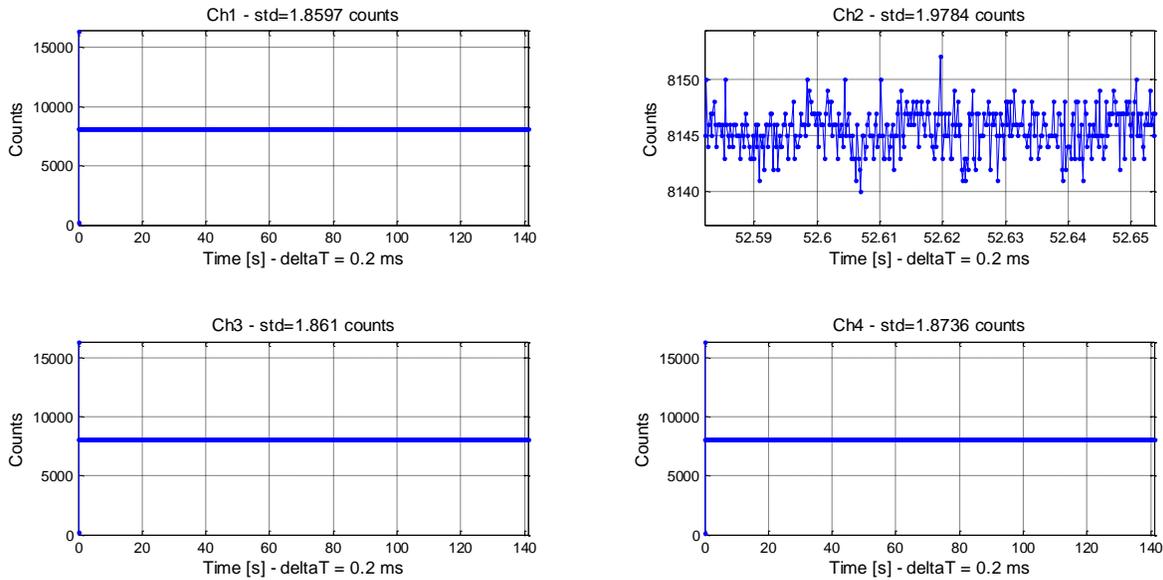


Figure 4-42: Standard deviation of counts for all channels on analog back-end board number 1

All analog back-end boards had similar outputs. These standard deviations of approximately 2 counts show that the board does not add significant noise to the signal. However, one should understand that these test results do not prove that the standard deviation of the output cannot be larger than two counts. If the input signal itself has a large enough standard deviation or if the gain on the analog back-end board is set to a level to produce a large enough standard deviation, the output of the ADC will also show this standard deviation.

Furthermore, comparing the output of the analog back-end board with the input recorded with the oscilloscope, it is evident that the input is indeed amplified by a factor of two (2), as expected. Also, though the input has 3.1 mV fluctuations from the 1 V DC signal, the output still has fluctuations of approximately 3.1 mV. This shows that the integrator is indeed filtering out some noise. Figure 4-43 shows the output of the ADC on the analog back-end board in volts. Note that again Channel 2 is zoomed in to show fluctuations.

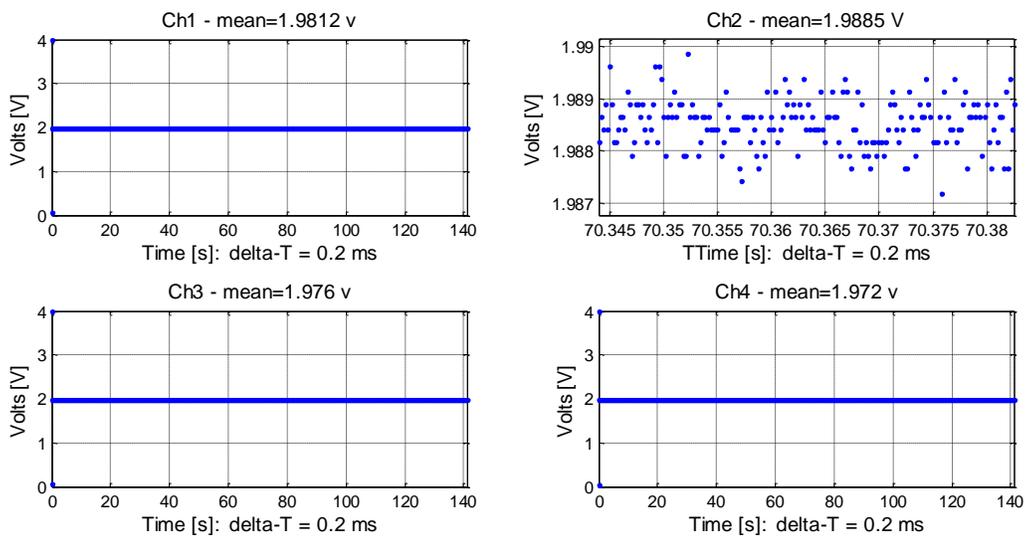


Figure 4-43: ADC output in volts of analog back-end board number 1

4.9.2 Linearity Test

The next test conducted was to determine the linearity throughout the range of the analog back-end board. To perform this test, the analog back-end board was connected to a Hewlett Packard 8116A [36] sine wave generator using the same connection as the noise test. A 500-Hz sine wave from the function generator was set to fill the entire range of the ADC. The output of the sine wave generator is shown in Figure 4-44. Note that although the frequency on the sine wave generator is set to 500 Hz, the output is actually 495 Hz.

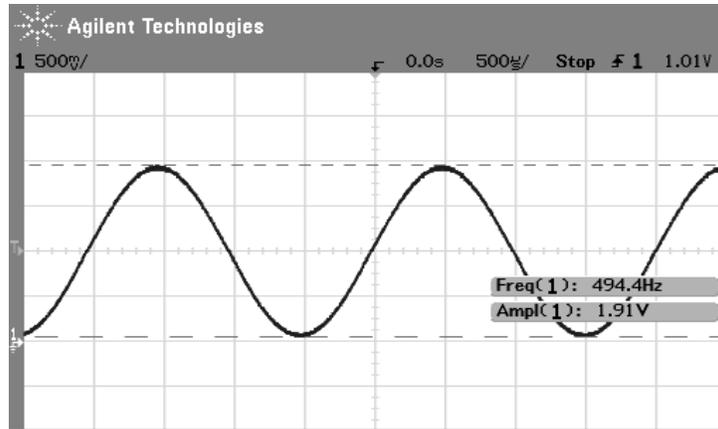


Figure 4-44: 495 Hz sine wave input used for linearity test of analog back-end board

Data from the output of the ADC was collected for approximately 3000 samples, and a Fast Fourier Transform (FFT) of this data was performed using the same Matlab script as the noise test. Figure 4-45 shows the FFT of all four analog back-end board channels.

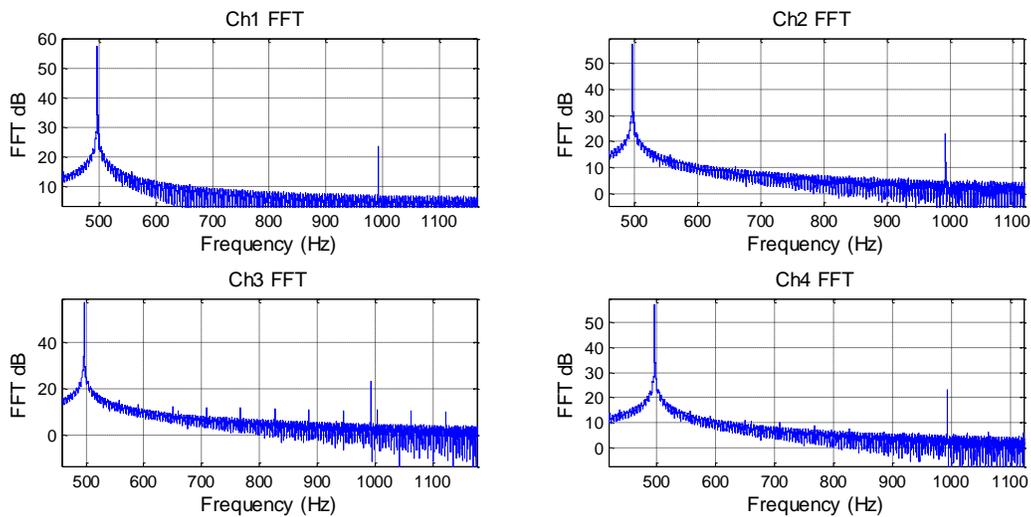


Figure 4-45: FFT of outputs of analog back-end board number 1 with 495 Hz input

The FFT shows that a 56 dB spike is at 495 Hz with a 26 dB harmonic at 990 Hz. This is a 33 dB difference between harmonics showing that no significant linear distortion is prevalent.

4.9.3 Standard Deviation as a Function of Gain

The final test conducted was to test the standard deviation as a function of the gain of the analog back end-board. The purpose of this test is to quantify the characteristic the input and output standard deviation as a function of gain on the analog back-end board. A input signal from a DC battery with a standard deviation of approximately 0.52 mV was connected to a potentiometer controlled voltage divider so that a variety of voltages could be produced. This schematic is shown in Figure 4-46.

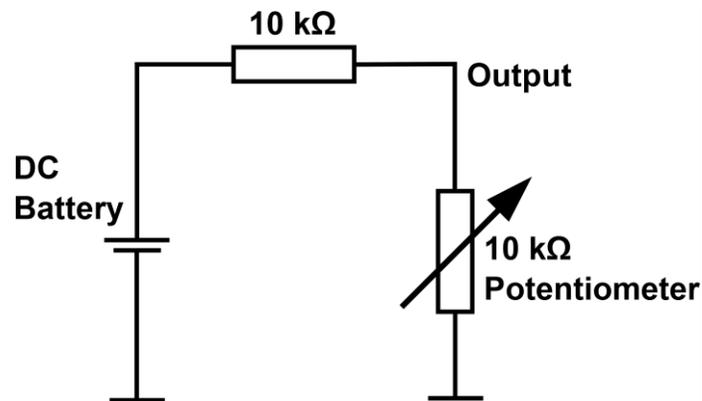


Figure 4-46: Voltage divider setup for standard deviation vs gain test.

The output of this voltage divider was connected to the analog back-end board, and the digitized signal was recorded. This test was performed while varying the gain on the analog back-end board with the values of 0.5, 1, 2, 100 and 1000.

The ratio of input and output standard deviation was then plotted as a function of gain, as shown in Figure 4-47.

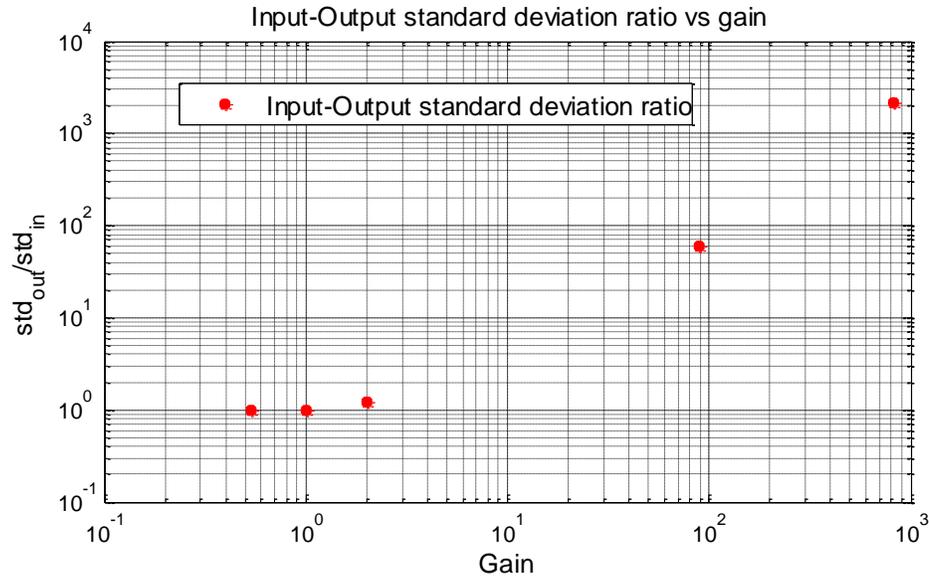


Figure 4-47: Input-output standard deviation ratio as a function of gain for analog back-end board number 1

This graph is as expected and shows that as the gain increases, the standard deviation ratio increases as well. This quantification of input to output ratio vs gain will be a useful reference for the behavior of the analog back-end board.

4.9.4 Summary of Tests

Three tests were conducted to determine the behavior of the analog back-end board. The noise test determined that the analog back-end board does not add significant noise to the signal because the standard deviation of the counts of the ADC is approximately the expected value. The linearity test showed that the analog back-end board does not add linearity distortion through the entire range of the ADC because an FFT of the signals shows a 33 dB difference between the first and second harmonics. Finally, the test of the standard deviation as a function of gain

quantified the behavior of the input to output standard deviation ratio as a function of the gain of the analog back-end board, as shown in Figure 4-47.

4.10 Analog Back-End Chassis

To digitize all 25 channels present on the airborne radiometer, seven analog back-end boards are needed. A chassis was built to house all of these boards. This chassis is 6" x 4.5" x 4.5" and is shown in Figure 4-48.

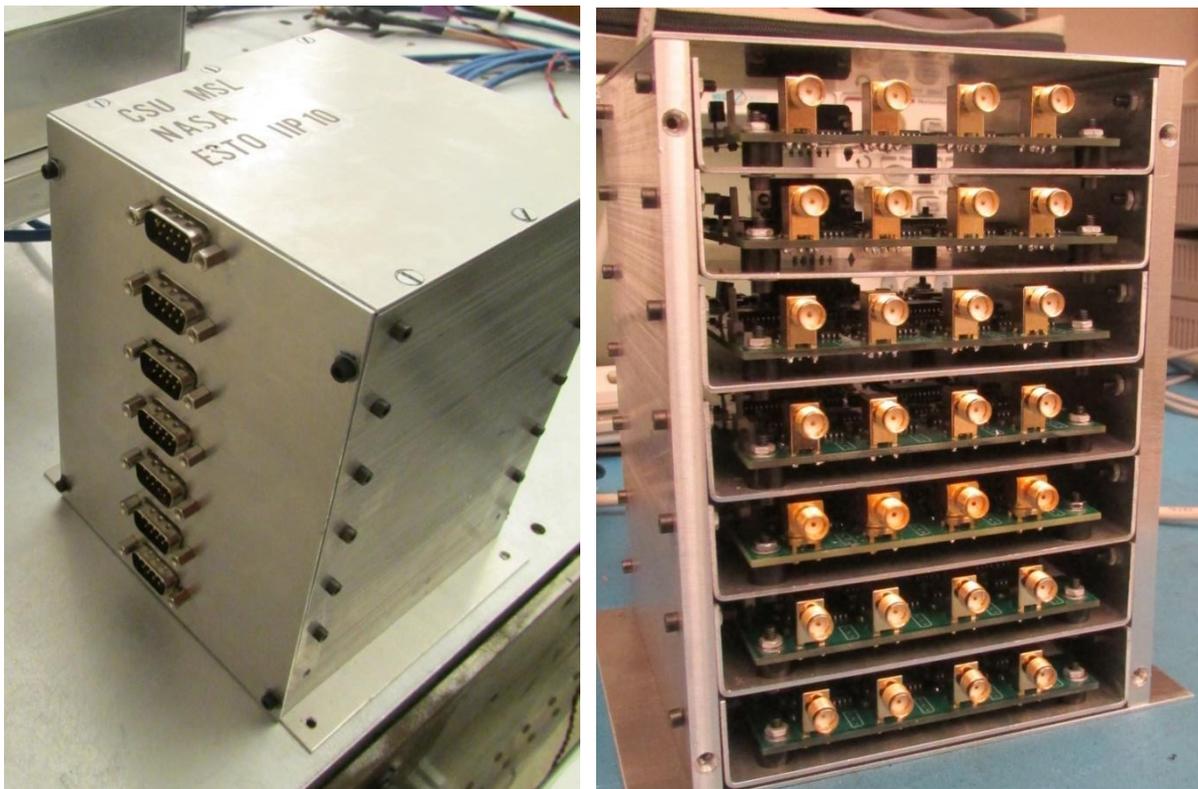


Figure 4-48: Analog back-end board chassis with (a) DE-9 side with lid and (b) SMA side without lid

The analog back-end boards are stacked vertically and are separated by aluminum trays. The analog back-end board chassis is mounted in the airborne radiometer chassis. The DE-9 connectors face the buffer board, while the SMA connections face the radiometers.

5. Buffer Board Design

This chapter will give an explanation of all interfaces, components, and signals on the buffer board. To interface all signals input into and output from the BeMicro SDK FPGA [18], a buffer board was created. This board buffers all radiometer, analog back-end, control and motor control signals and drives them at the appropriate voltage levels. All input data from the analog back-end board and motor control is also routed and interfaced through the buffer board to the FPGA. Figure 5-1 shows the block diagram of the buffer board.

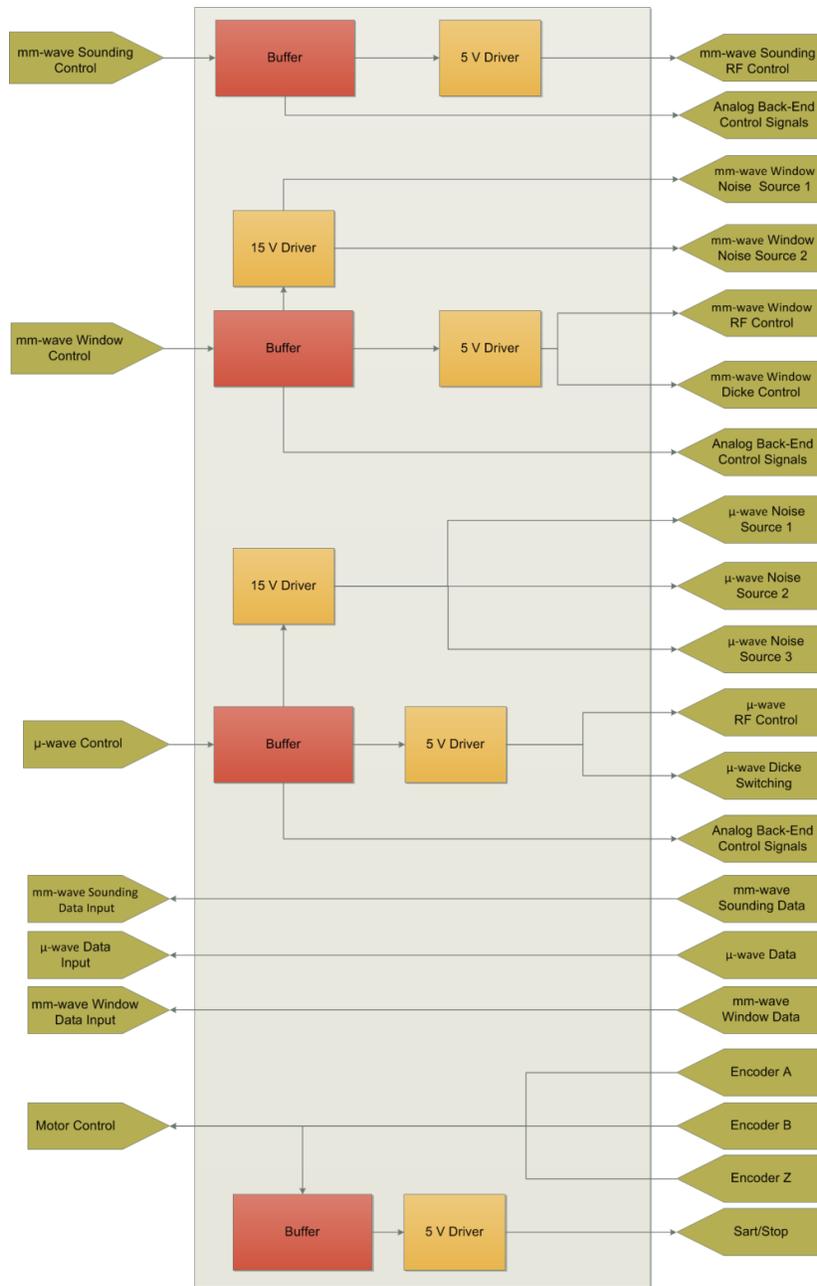
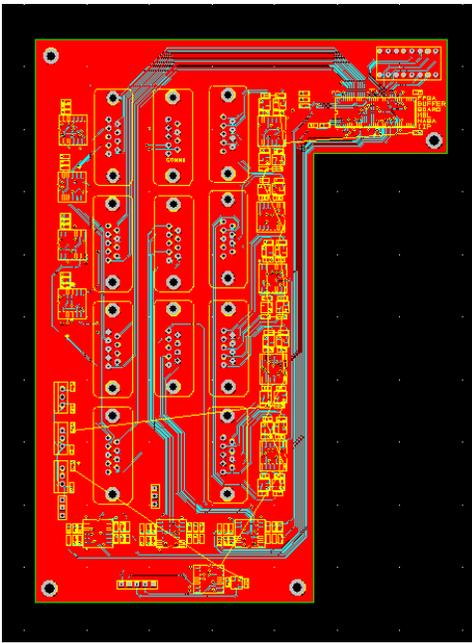
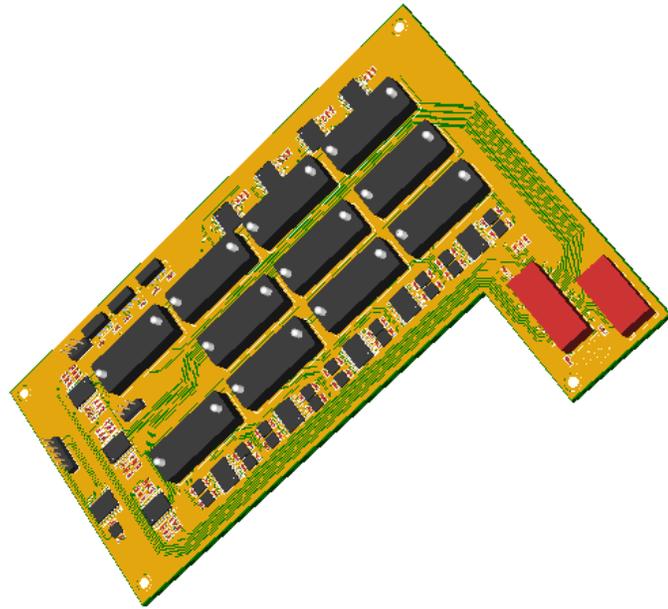


Figure 5-1: Buffer board block diagram

The buffer board was designed using Allied Devices DesignSpark Schematic and Printed Circuit Board Software [20]. Figure 5-2 shows the two-dimensional, (a) and three-dimensional (b) drawings of the Buffer Board made in DesignSpark. The Buffer Board is approximately 9” by 5” with a 2” x 7” cut-out for the BeMicro SDK FPGA.



(a)



(b)

Figure 5-2: (a) Buffer board PCB layout and (b) 3-dimensional drawing

The buffer board was fabricated at Advanced Circuits [37] and populated by hand at Colorado State University. Figure 5-3 shows an image of the fully-populated buffer board with the FPGA attached.

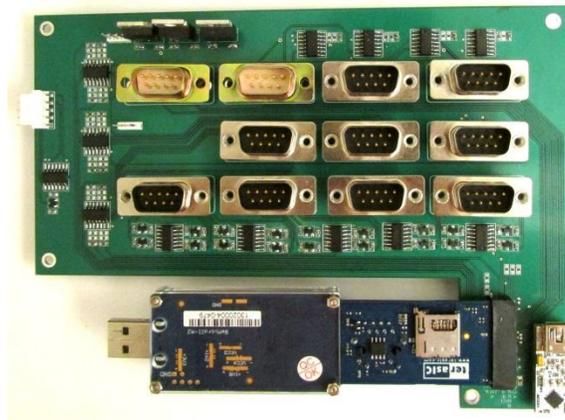


Figure 5-3: Fabricated and populated buffer board with FPGA attached

5.1 FPGA Connection Interface

The BeMicroSDK is connected to the buffer board via a SAMTEC MEC6-140-02-L-D-RA1 Card Edge Connector [38]. The card edge of the BeMicro SDK FPGA has 80 pins and slides directly into this connection. Both the card edge connector (a) and card edge (b) are shown in Figure 5-4.

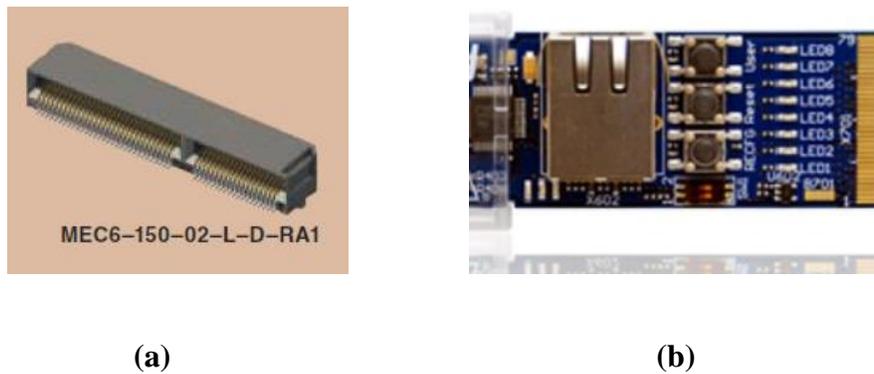


Figure 5-4: (a) Female SAMTEC MEC6-140-02-L-D-RA-1 card edge connector and (b) Male BeMicro SDK FPGA card edge [38]

5.2 Buffer Design

The output signal from the FPGA is first buffered using a NXP 74HC125 quad (4 channel) buffer integrator circuit (IC) [39]. The 74HC125 quad buffers ICs are circled in red on the buffer board shown in Figure 5-5.

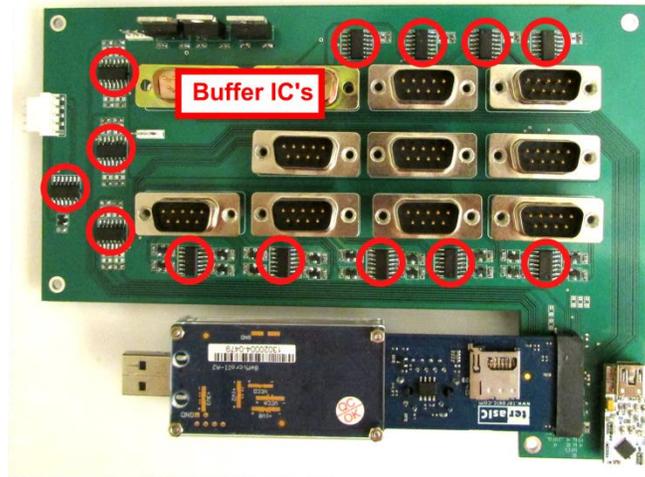


Figure 5-5: Buffer board with buffer ICs circled in red

The 14 pin small outline integrated circuit (14-SOIC) package for the 74HC125 buffers was used on the buffer board. These buffers are used to protect the FPGA outputs from being the load on both the analog back-end board, as explained in Chapter 4, and the radiometer front-end. A schematic of the 74HC125 is shown in Figure 5-6.

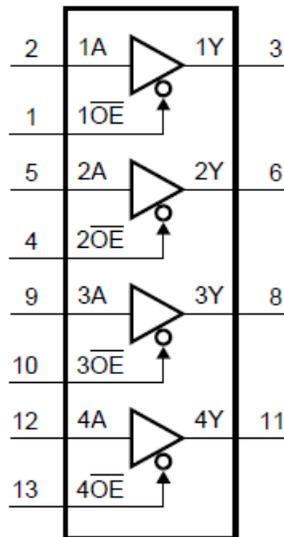


Figure 5-6: Functional block diagram of 74HC125 buffer IC [39]

All output enable or “ \overline{OE} ” are inverse logic signals and are grounded in the buffer board design. This requirement comes from Table 3 on the 74HC125 datasheet and is shown in Table 5-1 [4]. For all analog back-end signals, the 74HC125 is powered with 3.3 V, which produces 3.3 V logic level outputs appropriate for analog back-end board controls. For the radiometer control signals all 74HC125 are powered with 5 V, which produces 5 V logic level outputs.

Table 5-1: Function table for the 74HC125

Control	Input	Output
\overline{OE}	\overline{A}	\overline{Y}
L	L	L
L	H	H
H	X	Z

* H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

At the input of every buffer, an optional filter and voltage dividing circuitry was placed in case additional signal conditioning was needed. The circuitry is not used in the current buffer board design, so a 0 Ω resistor is used for the series resistor and the shunt resistor and capacitor connection is left blank. A schematic of this circuitry is shown in Figure 5-7.

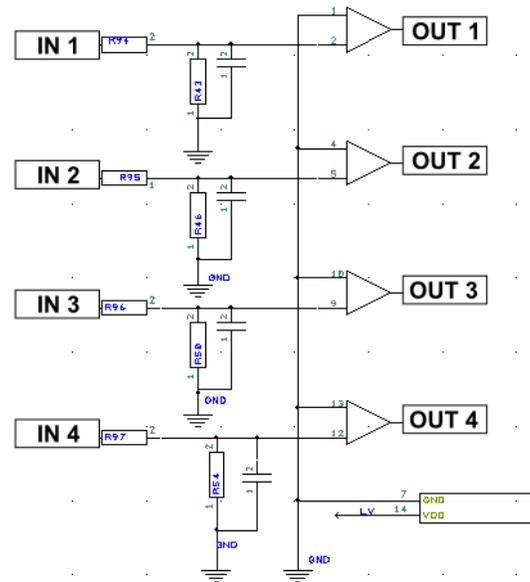


Figure 5-7: Schematic of input to each buffer

5.3 Signal Voltage Level Conversion

After buffering the radiometer control signals, the logic levels are then converted to higher voltage levels. The required voltage levels for radiometer controls are as follows:

- Noise Sources : 15 Volts
- Dicke Switch: 5 Volts
- RF Control : 5 Volts

As explained in Section 5.2 the logic level coming from the 74HC125 is 5 V, however the level converting circuitry is still applied to both the Dicke and RF control so these signals remain at 5 V when loaded with low-impedance loads. To accomplish the level converting, the Metal-Oxide-semiconductor field-effect transistor (MOSFET) level converter circuit shown in Figure

5-8 was used. The specific MOSFET used in the design is a BSS138 N-Channel double-diffused meta-oxide semiconductor (DMOS) [40].

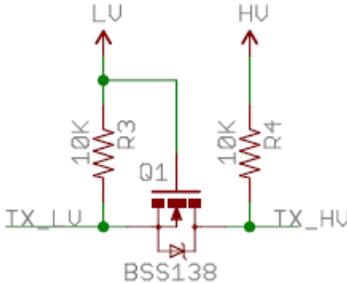


Figure 5-8: Level converter schematic [41]

The “LV” is the low voltage level which should be matched to the input logic level or “TX_LV”. The “HV” is the high voltage level which should be matched to the desired output voltage or “TX_HV.” Both TX signals are pulled up to the corresponding “LV” or “HV” logic level through a 10 KΩ resistor. The BSS138 DMOS transistors used in level converting were Small Outline Transistor (SOT-23) packages. All level converting circuits on the buffer board are shown in Figure 5-9 circled in red.

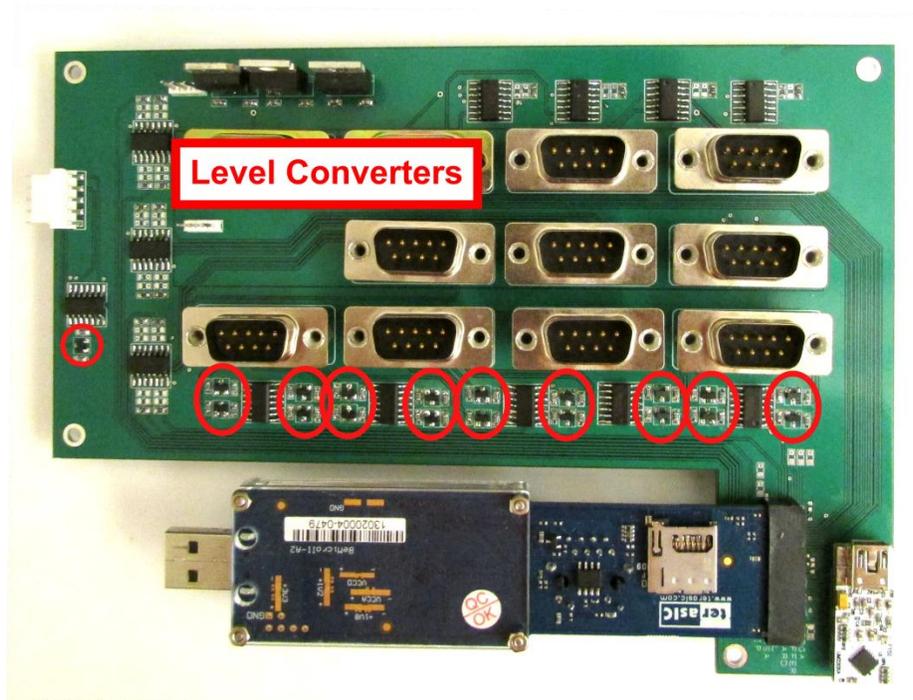


Figure 5-9: Level converters on the buffer board circled in red

5.4 Buffer Board Radiometer Control Interface

The radiometer front-end and the buffer board are interfaced through a 9-pin D-subminiature (DE-9) connector. Each DE-9 pin-out is different for each radiometer and can be seen circled in red in Figure 5-10.

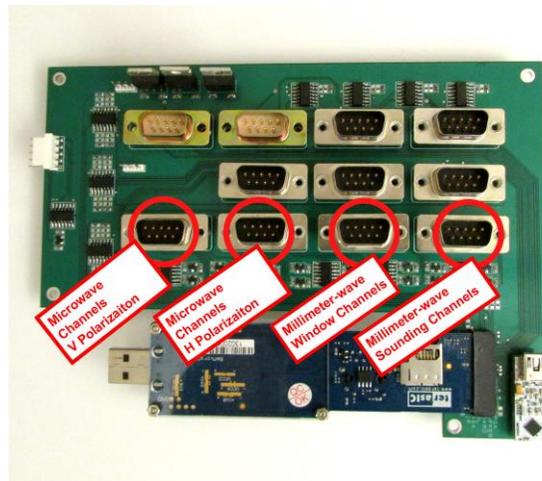


Figure 5-10: DE-9 connections for radiometer control on the buffer board

The pin outs for (a) the microwave channels, (b) the millimeter-wave window channels, and (c) the millimeter-wave sounding channels are shown in Figure 5-11. “DIG GND” is the ground for all digital components and “ANLG GND” is the ground for all analog components. The grounds are separated to remove as much noise as possible from high-speed digital switching on the analog ground. “Dicke” controls the Dicke switching, “NS” controls the noise sources, and “RF” turns the radiometer on and off.

Dicke	5	9	DIG GND
NS1	4	8	DIG GND
NS2	3	7	ANLG GND
NS3	2	6	ANLG GND
RF	1		

(a)

Dicke	5	9	DIG GND
NS1	4	8	DIG GND
NS2	3	7	ANLG GND
RF	2	6	ANLG GND
	1		

(b)

RF Sounder 1	5	9	DIG GND
RF Sounder 2	4	8	DIG GND
RF Sounder 3	3	7	ANLG GND
RF Sounder 4	2	6	ANLG GND
	1		

(c)

Figure 5-11: DE-9 interface layout for (a) Microwave (b) Millimeter-wave Window and (c)

Millimeter-wave Sounding channels

5.5 Analog Back-End Control Interface

The buffer board and the analog-back end board are also interfaced through a DE-9 connector.

Figure 5-12 shows all analog back-end board interfaces circled in red.

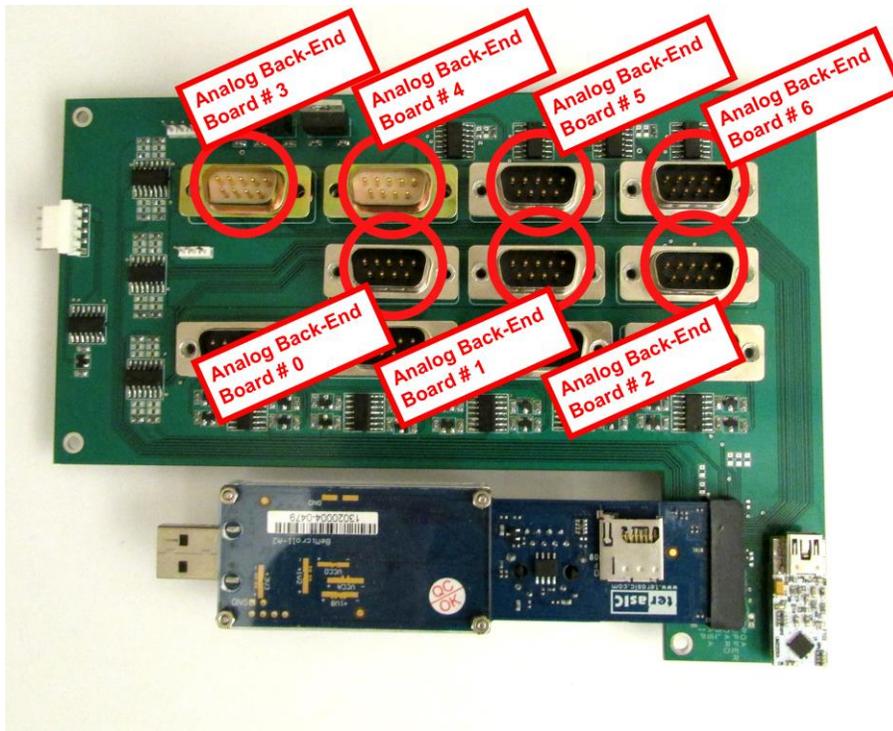


Figure 5-12: DE-9 connections for analog back-end on buffer board

All integrator control signals, ADC timing signals, data outputs, and power are provided through this connector. A schematic of the Analog Back-End Board DE-9 connector is shown in Figure 5-13. The “Hold,” “Reset,” “CS,” “SPI,” “Data A,” and “Data B” signals are explained in Chapter 4. “DIG GND” is the digital ground. “POWER NEG” and “POWER POS” are the negative and positive power connections, respectively, for the analog back-end board, which are supplied with -12 V and $+12\text{ V}$, respectively.

HOLD	5	9	DATA B
RESET	4	8	POWER POS
DIG GND	3	7	POWER NEG
CS	2	6	SPI
DATA A	1		

Figure 5-13: Analog back-end DE-9 interface connector layout

5.6 Motor Driver Interface

The buffer board also interfaces with the motor for the rotating flat reflector. The motor is the A34HK-1 I grade from QuickSilver Motors [42]. It has one control line and three motor position lines. Lines “A” and “B” have the encoding for clockwise rotation, as shown in Table 5-2.

Table 5-2: Clockwise rotary encoding for Quicksilver A34HK-1 I grade motor

Phase	A	B
1	0	0
2	0	1
3	1	1
4	1	0

These lines are 90° out of phase with each other [9]. A timing diagram of these lines with the corresponding phase is shown in Figure 5-15.

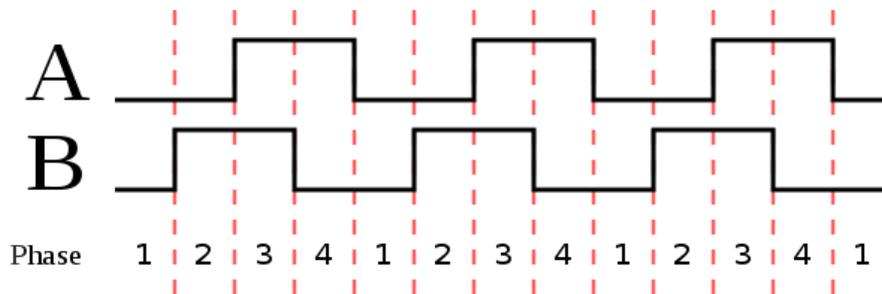
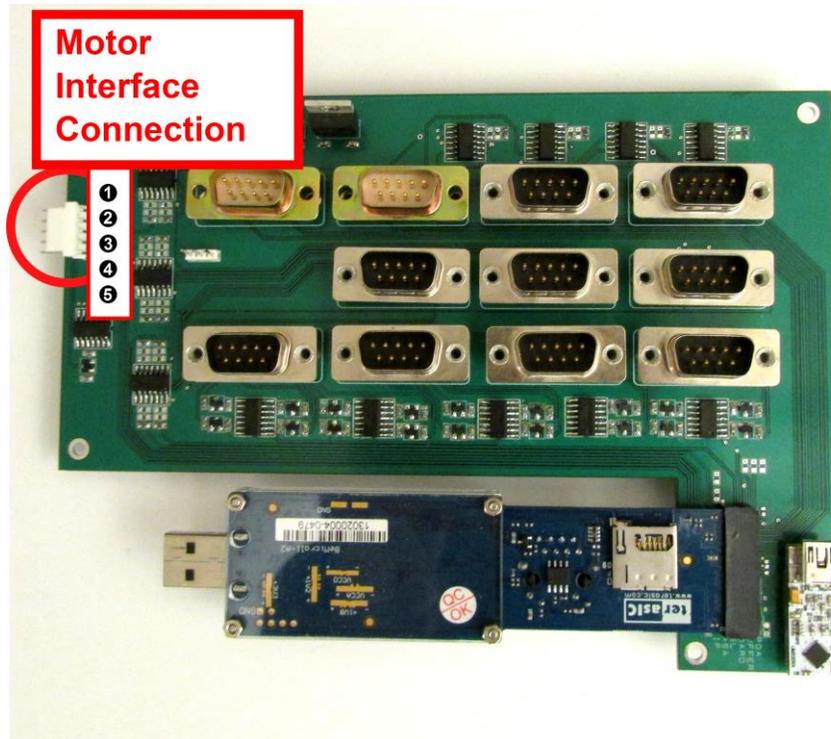


Figure 5-14: A34HK-1 I grade [42]

The “Z” line is used for the linear compensation of motor drift, which sends 49 pulses per motor revolution. For the “start/stop” control line, a logic “high” starts the motor, while a logic “low”

stops the motor. Figure 5-165 shows (a) the 5-pin motor control interface connection circled in red and (b) the 5-pin motor control interface connection layout.



(a)

- ① A
- ② B
- ③ Start/Stop
- ④ Z
- ⑤ GND

(b)

Figure 5-15: (a) 5-pin motor control interface connection circled in red and (b) the 5-pin motor control interface connection layout.

5.7 FPGA to Computer Interface

The BeMicro SDK FPGA is connected to a computer through an UMFT220XA USB to 4-Bit SPI/FT1248 development module [43]. The UMFT220XA interfaces the FPGA to a ‘mini-B’ USB. On the other end, this USB cable is connected to a computer for control and data input. The UMFT220XA has the following features.

- Easy-to-mount 16-pin dual in-line package with 0.1 inch pitch
- 500 kBps maximum data throughput
- 4-bit serial peripheral interface (SPI)
- Drivers available for both Windows and Linux

Figure 5-16 shows the UMFT220XA USB-to-SPI converter circled in red on the buffer board.

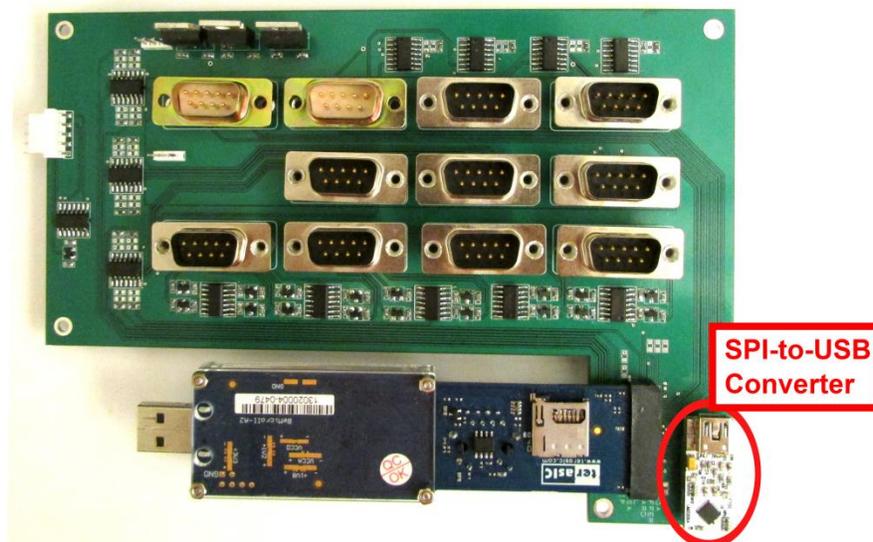


Figure 5-16: UMFT220XA USB-to-SPI converter circled in red on the buffer board

5.8 Buffer Board Power Regulation and Distribution

The buffer board requires three regulated voltage levels: 3.3 V for analog back-end board control, 5 V for Dicke and RF control as well as FPGA power, and 15 V for noise source control. Table 5-3 lists each regulator with the corresponding output voltage, input capacitor, and output capacitor values.

Table 5-3: Buffer board voltage regulators with corresponding output voltages, input capacitors, and output capacitor values

Regulator	Output Voltage	Input Capacitor	Output Capacitor
TLV2217-33CSE3 [44]	3.3 V	0.1 μ F Ceramic	22 μ F Tantalum
UA78M05KCS [45]	5.0 V	0.33 μ F Ceramic	0.1 μ F Ceramic
KA7815ETU [46]	15.0 V	0.33 μ F Ceramic	0.1 μ F Ceramic

The analog back-end board power is also routed, though not regulated, through the buffer board. Figure 5-17 shows the buffer board power input connection, analog back-end board power connection, and buffer board regulators circled in red. At 16 V the buffer board and FPGA consumes 210 mA of current or 3.36 W of power.

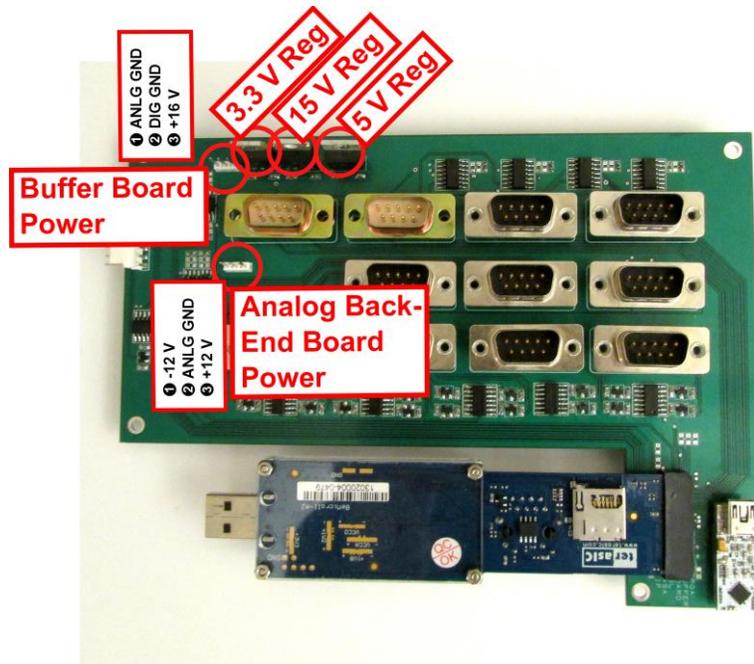


Figure 5-17: Power connections and voltage regulators on the buffer board

5.9 Ground Connections

To ensure that no ground loops are present in back-end system a grounding convention was created. The diagram is shown in Figure 5-18.

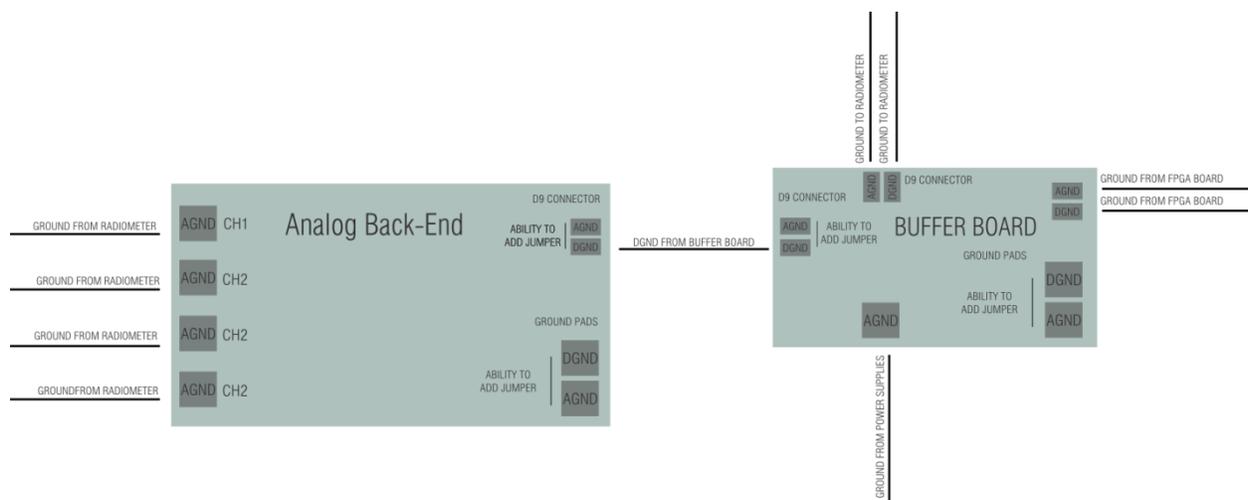


Figure 5-18: Ground connection diagram for analog and digital back-ends

All of the analog grounds are grounded through the chassis and the radiometer. The power grounds for the buffer board are grounded to the power supplies, which can also be considered analog ground. The analog back-end board and the buffer board both have digital grounds which are connected together through the DE-9 connection between the two boards.

5.10 Buffer Board Chassis

A chassis was designed for the buffer board and FPGA. This chassis, made from 50-mil thick aluminum, is 2" x 6" x 8", as shown in Figure 5-19.

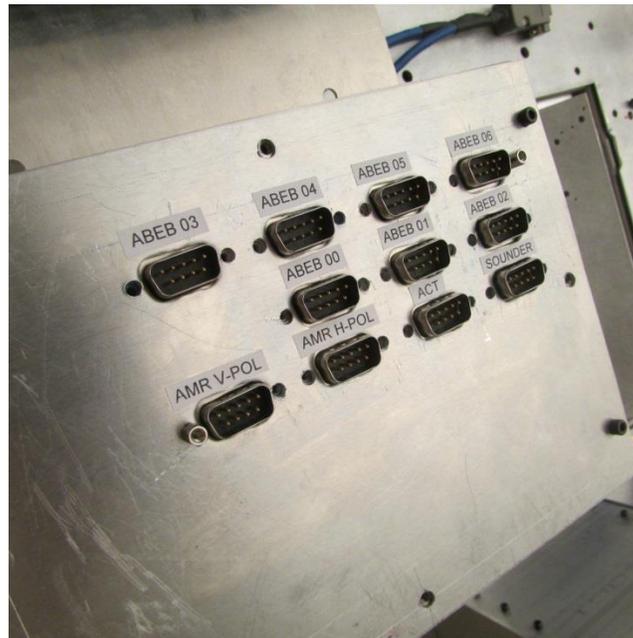


Figure 5-19: Buffer board chassis

All DE-9 connections are on the top of the chassis. Furthermore, the buffer board power, analog back-end board power, USB, Ethernet, and motor control connections are on the sides of the chassis. The buffer board chassis securely mounts to the top of the airborne radiometer chassis, and all DE-9 cables can be easily routed to either the analog back-end board chassis or the radiometers.

6. Summary and Conclusion

A data acquisition and control subsystem was designed, fabricated and tested for an internally-calibrated, wide-band airborne radiometer to reduce risks associated with wet-path delay correction for the SWOT mission. First, an analysis of the control and data acquisition subsystem design requirements was conducted. From this analysis, requirements based on the required beam efficiency, airborne platform footprint size, acquisition capabilities, and sampling error were derived. These requirements in turn helped to define acceptable paraboloid roughness, integration time, data throughput, and filtering architecture, respectively. Considering these requirements, both an analog back-end, for data acquisition via analog-to-digital conversion, and a digital back-end, for data routing and system control, were successfully designed, fabricated and tested.

Table 6-1 provides a list of the per channel area, mass and power consumption of the analog back-end board.

Table 6-1: Analog back-end board per channel size, mass, and power consumption

Area per channel	$0.002316 \text{ m}^2 = 23.16 \text{ cm}^2$
Mass per channel	$0.01519 \text{ kg} = 15.19 \text{ g}$
Power consumption per channel	1.11 W

The area, mass and power consumption of the digital back-end, including the FPGA, are shown in Table 6-2. These specifications are for the entire control and data handling subsystem, instead of per channel.

Table 6-2: Digital back-end board total size, mass, and power consumption

Total area	$0.0234 \text{ m}^2 = 234 \text{ cm}^2$
Total mass	$0.1433 \text{ kg} = 143.3 \text{ g}$
Total power consumption	3.36 W

Additional documentation of the schematics and designs of the printed circuit boards are provided in Appendices V and VI, “DesignSpark Design for Analog Back-end Board” and “DesignSpark Design for Buffer Board,” respectively. The software versions of these designs have been archived and documented for use in the project. Chassis have been built to physically support and electrically protect the analog back-end and digital back-end boards. These chassis will be mounted in the IIP-10 Airborne Radiometer system chassis for testing and science flights.

7. Bibliography

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Appendix I Matlab Script for Footprint Analysis

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%% This script calculates the available integration time and the distance
%% between centers of two consecutive footprints. For that purpose the
%% required inputs are the height and speed of the plane, the spinning
%% velocity of the parabolic reflector and the beamwidths of the
%% radiometers.
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%
%%           Maximum altitude [m]   Maximum Speed [m/s]
%%
%% Twin Otter           3000           33
%% King Air              9100           140
%% Global Hawk          19800          172
%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all

close all

clc;

%
% CONSTANTS - Flight parameters
%
```

```

h = 19800; % Altitude [m]
FOV = 60*pi/180; % Field of View (FOV) [rad]
THETA_HP = (0.6356)*(pi/180); % Half Power Beamwidth [rad] 90 GHz mm-wave
radiometers
THETA_HP = (3.2)*(pi/180); % Half Power Beamwidth [rad] 18 GHz Low-
frequency microwave radiometers
v = 172; % Velocity [m/s]
RPM = 59.4929; % Revolutions Per Minute [RPM]
% RPM = 10;
%
% CALCULATIONS
%
SPR=1/(RPM/60); % Seconds for Revolution [s]
MaxTime = 4*SPR % Time of Two Revolutions [s]
NumberOfEvents=2*pi/THETA_HP % Number of Independent Footprints per Scan
DeltaTime=SPR/NumberOfEvents % Integration Time [s] per footprint
Time=0:DeltaTime:MaxTime; % Increment Time For Two Rotations [s]
IncidenceAngle=mod(Time.*2*pi/SPR, 2*pi); % Incidence Angle [rad]
FOVMask= (IncidenceAngle>=(2*pi-FOV)) | (IncidenceAngle<=FOV); % FOV Mask
Measurements=sum(FOVMask);
Steps=length(FOVMask);
ratio=Measurements/Steps;

```

```

% Along Track Axis & Cross Track Axis, Ellipse
AlongTrackAxisVector(1: Measurements) =
2*tan(THETA_HP/2)*h*sec(IncidenceAngle(FOVMask));
CrossTrackAxisVector = h*((tan(IncidenceAngle(FOVMask)+THETA_HP/2)-
tan(IncidenceAngle(FOVMask)-THETA_HP/2)));

% %%MIN MAX
maxcrosstrack = h*((tan(FOV+THETA_HP/2)-tan(FOV-THETA_HP/2)))

% X (Cross Track) Axis & Y (Along Track) Axis, Ellipse center
YCoordinate=Time(FOVMask).*v;
XCoordinate= h*tan(IncidenceAngle(FOVMask));

% Assume A Tilt of 0
TiltAngle(1:Measurements)=0;

% Find the min and max along and crosstrack axis

ymin = min(AlongTrackAxisVector)
xmin = min(CrossTrackAxisVector)
ymax = max(AlongTrackAxisVector)
xmax = max(CrossTrackAxisVector)

% Calculating the minimum RPM for ensuring complete coverage of the scene
%
```

```

DeltaX = tan(THETA_HP)*h;           % This is the along flight length of the
footprint, the 1 would be changed to a 2 if the HPBW was defined as the
radius.

TT = DeltaX/v                       % This is the time it takes the aircraft
to do one swath scan

ASR_ideal = (2*pi)/TT;             % This is the angular scanning rate in
radians.

RPS_ideal = ASR_ideal/(2*pi)       % Revolutions Per Second
RPM_ideal = RPS_ideal * (60)       % Revolutions Per Minute
SPR_ideal = 1/(RPS_ideal)          % Seconds Per Revolution put in as a
check, should equal TT

% Calculating some NEDT values, Total temperature based on estimates
% NEDT and per footprint

NEDT18=800/sqrt(200e6*DeltaTime)
NEDT23=925/sqrt(400e6*DeltaTime)
NEDT34=1050/sqrt(800e6*DeltaTime)

NEDT90=1600/sqrt(8000e6*DeltaTime)
NEDT130=1700/sqrt(12000e6*DeltaTime)
NEDT166=1800/sqrt(12000e6*DeltaTime)

%
% Ellipse Plotting Function -----

```

```
% ELLIPSE(ra,rb,ang,x0,y0) adds an ellipse with SEMImajor axis of ra,  
% a SEMImajor axis of radius rb, a semimajor axis of ang, centered at  
% the point x0,y0.  
hw=ellipse(CrossTrackAxisVector./2,  
AlongTrackAxisVector./2,TiltAngle,XCoordinate,YCoordinate);  
xlabel('Cross Track [m]','fontsize',16);  
ylabel('Along Track [m]','fontsize',16);  
axis equal  
grid on
```

Appendix II Analog to Digital Converter Bit Analysis

```
close all

clear all

clc

bits=8:20

%%% This plot assumes that the Tsys spans all the conversion window of the
%%% adc

figure(1); hold on, grid on

plot(bits, 1./2.^bits)

Bw=9e10, Tint=0.1e-3,

plot(bits, ones(1,length(bits)).*1./sqrt((Bw*Tint)), 'g*')

Bw=0.3e10, Tint=0.2e-3,

plot(bits, ones(1,length(bits)).*1./sqrt((Bw*Tint)), 'm*')

Bw=0.5e10, Tint=1e-3,

plot(bits, ones(1,length(bits)).*1./sqrt((Bw*Tint)), 'r*')

title(sprintf('Required number of bits for all the radiometers types'))

ylabel('unitless error [normalized]')

xlabel('number of bits')

legend('Quantization error', 'ACT08 radiometer uncertainly, B_w=9 GHz and
T_{int}=0.1 ms', 'AMR readiometer uncertainly, B_w=0.5 GHz and T_{int}=0.2
ms', 'Sounding Channel uncertainly, B_w=0.5 GHz and T_{int}=1 ms', 0)

Bw=9e10, Tint=0.1e-3,
```

```
plot(bits, ones(1,length(bits)).*1./sqrt((Bw*Tint)), 'g')
Bw=0.3e10, Tint=0.2e-3,
plot(bits, ones(1,length(bits)).*1./sqrt((Bw*Tint)), 'm')
Bw=0.5e10, Tint=1e-3,
plot(bits, ones(1,length(bits)).*1./sqrt((Bw*Tint)), 'r')
```

Appendix III Low Pass Filter vs Integrator

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Low Pass Filter vs. Integrator Script
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Scott Nelson,
% V0005 2/15/12
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all,
close all,
clc,
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Define Sampling Rate
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Fs=1e3, % minimum 10KHz

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Creates the Thermal Noise
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% what is the statistic before a power detector??? GAUSSIAN

% Creating the noise after the LNA and filters, already in baseband

one_ms=1e-3
Nfootprints=100;
NeventsPerFootPrint=one_ms*Fs;
NanalogSamplesPerEvent=10*NeventsPerFootPrint;
NanalogSamplesFootprint=NeventsPerFootPrint*NanalogSamplesPerEvent;
```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Low Pass Filter
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

fc = 4999;
Wn = 2*fc/(NanalogSamplesPerEvent*Fs);
[B,A] = butter(2,Wn,'low');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Integrator
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

NUM = 1;
DEN = 1;

A = [DEN 0];
B = [0 NUM];

T_S = tf(B,A)

%%% Sampling with no filter
% B=1, A=1

% this means that there is 1000 samples in each calibration
% cycle, or footprint, if we assume 10 samples per footprint

```

```

%(100 simulated points per sample) and each footprint takes
% 1 ms then the time resolution is Tres=1ms/100; Tres =10us

PercentageOfLoad=0.1    % Right now should be 0.1 or multiples
PercentageOfAntenna=1-PercentageOfLoad;
Tanalogbasis=(1/(Fs))/NanalogSamplesPerEvent; % this is determined by the Fs,
now assumed to be 1Khz

NanalogSamplesLoad=round(PercentageOfLoad*NanalogSamplesFootprint);
NanalogSamplesAntenna=round(PercentageOfAntenna*NanalogSamplesFootprint);
%
Tantenna=200           % Kelvin
Tload=800              % Kelvin
Trec=2000              % Kelvin 1200

noise=[]

for i=1:Nfootprints

    noise=[ noise sqrt(Tload+Trec).*randn(1,NanalogSamplesLoad)
sqrt(Tantenna+Trec).*randn(1,NanalogSamplesAntenna)];

end

Nsamples=length(noise);
timeanalogBasis=0:Tanalogbasis:Tanalogbasis*(Nsamples-1);

```

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Compute the Power of the Signal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% what is the statistic after a power detector??? RAYLEIGH

PowerDetected=noise.^2;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Low Pass Filter the Detected Power
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%This is the RC filter

FilteredPower=filter(B,A,PowerDetected);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Plots
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Filtered Power Detector

figure(3)
hold on, grid on,
plot(timeanalogBasis,FilteredPower)
plot(timeanalogBasis,FilteredPower,'r.')
title('Filtered Power Detector')
xlabel('Time [s]')

```

```
ylabel('power [K]')
```

```
N = (NanalogSamplesPerEvent)-20:NanalogSamplesPerEvent:length(FilteredPower);
```

```
SampledPower = FilteredPower(N);
```

```
SampledTime = timeanalogBasis(N);
```

```
figure(3)
```

```
plot(SampledTime, SampledPower, 'ko')
```

```
MatrixSampledPower= reshape(SampledPower, NeventsPerFootPrint,  
length(SampledPower)/NeventsPerFootPrint)';
```

```
SampledPowerMean = mean(MatrixSampledPower)
```

```
SampledPowerSTD = std(MatrixSampledPower)
```

```
figure(4)
```

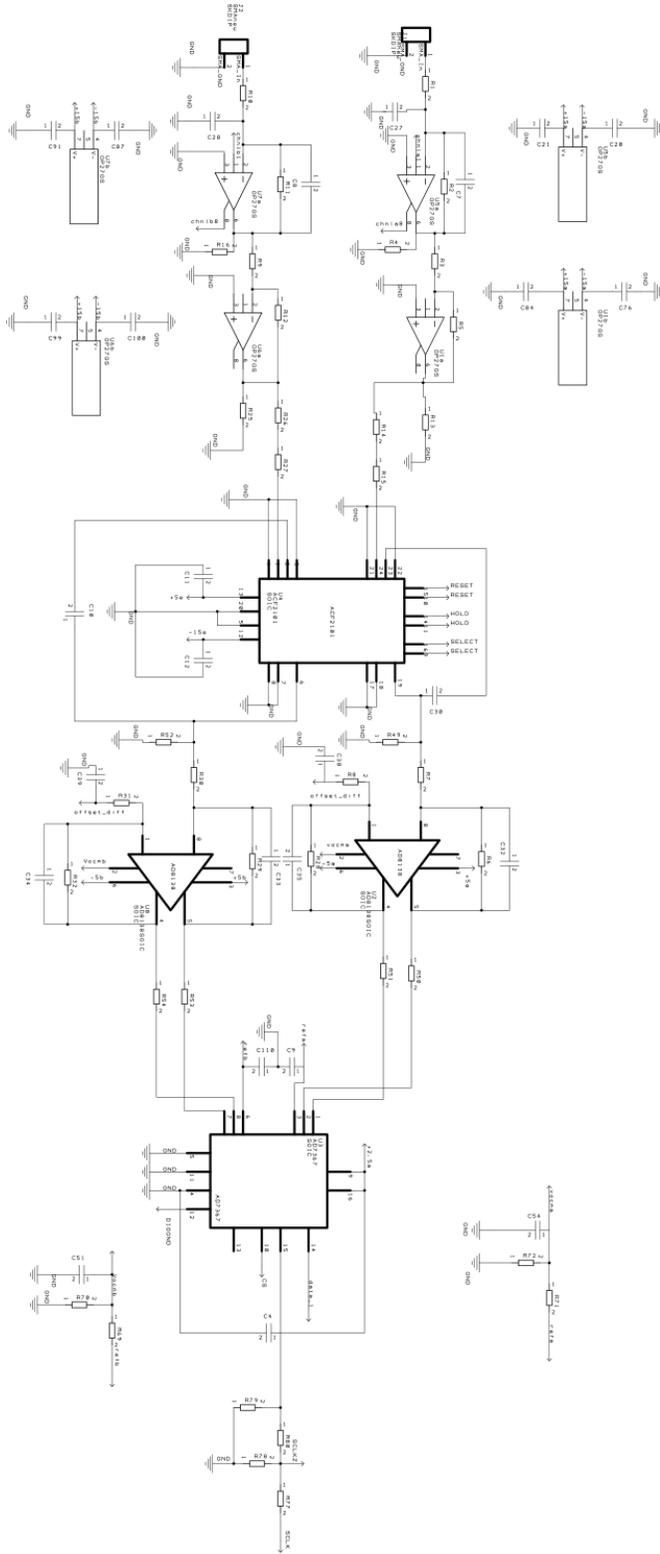
```
subplot(2,1,1), hold on,
```

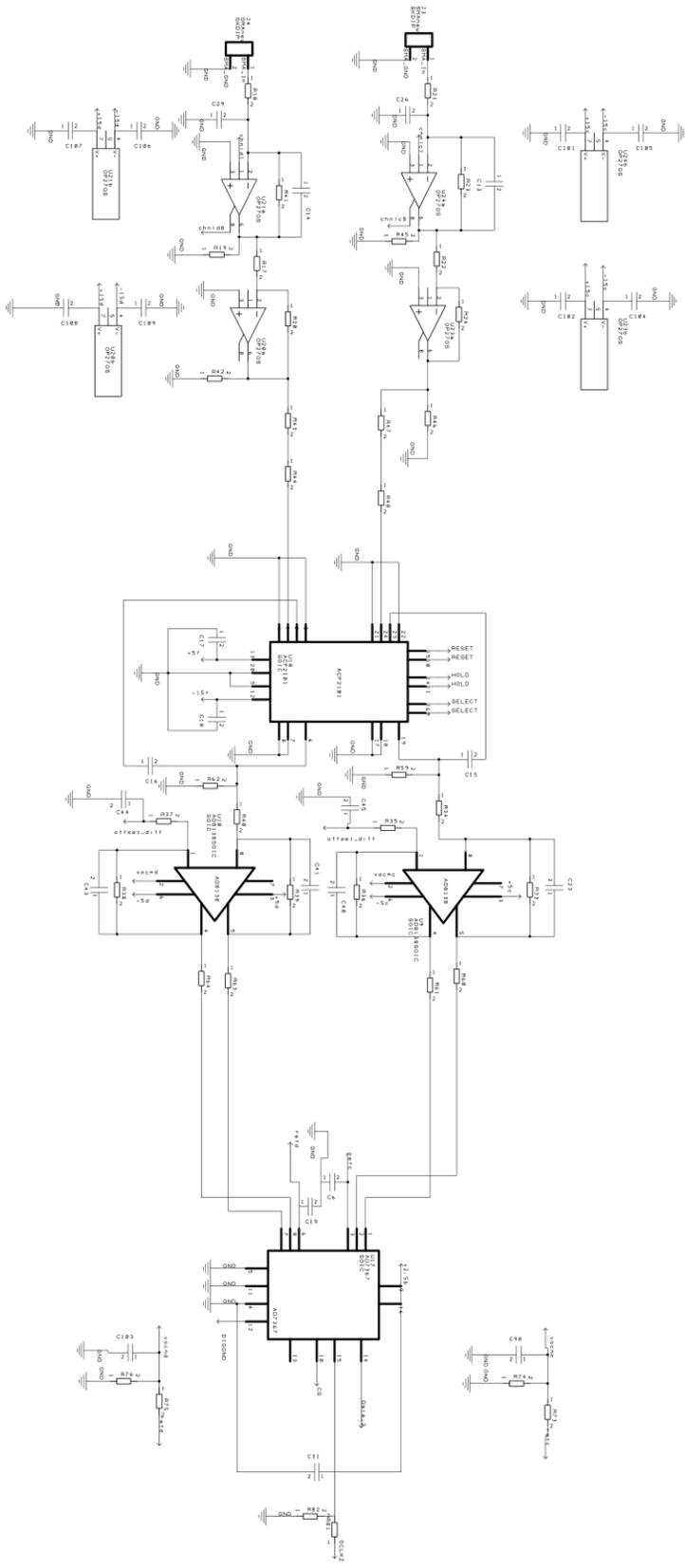
```
plot(SampledPowerMean, '*'), grid on
```

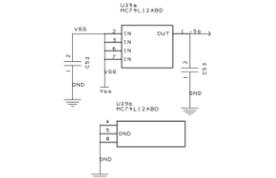
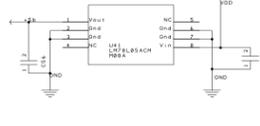
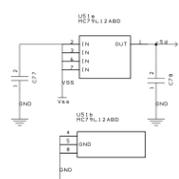
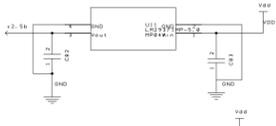
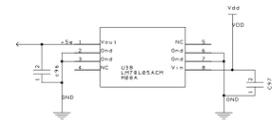
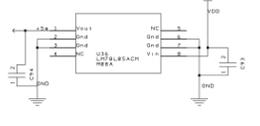
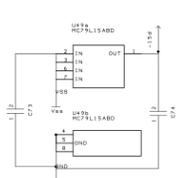
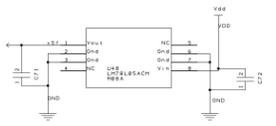
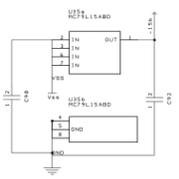
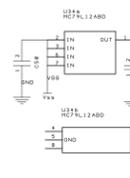
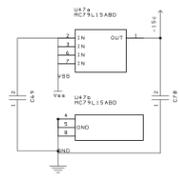
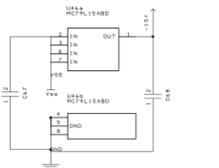
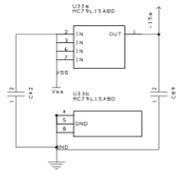
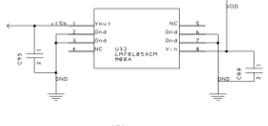
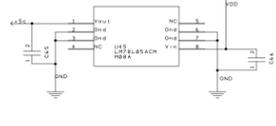
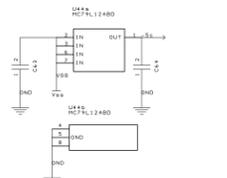
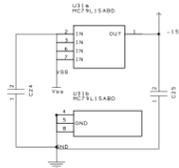
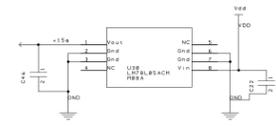
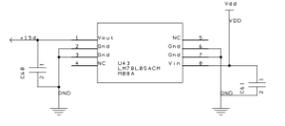
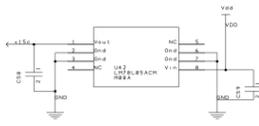
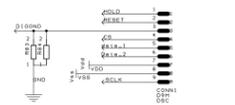
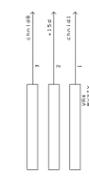
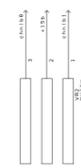
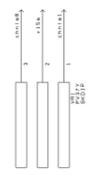
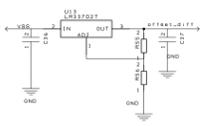
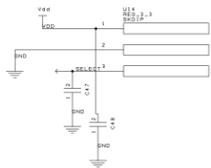
```
subplot(2,1,2), hold on,
```

```
plot(SampledPowerSTD, 'r*'), grid on
```

Appendix IV Analog Back-End Board Schematic from DesignSpark







Appendix V Matlab Script for Analog Back-End Board Acquisition

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Matlab Script for Analog Back-End Board Acquisition
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

clear all

close all

clc

%-----
%-----

filename='2013_07_01__15_33_45__Bone_OneVolt';

%-----
%-----

CONF_filename=[filename '.txt'];
DATA_filename=[filename '.bin'];

%-----

% IMPORT CONFIGURATION -----
%-----

newData1 = importdata(CONF_filename);

% Create new variables in the base workspace from those fields.

vars = fieldnames(newData1);

for i = 1:length(vars)
    assignin('base', vars{i}, newData1.(vars{i}));
end

%-----

% Reading configuration data from config.txt file -----
%-----

Ts=data(1,1);

TsDisplay=[data(1,1) zeros(1,10)]';
```

```

numberSlots=[data(1,2) zeros(1,10) ]';

for i=1:10
    Seq(i)=data(i,3);
    LengthSeq(i)=data(i,4);
end

SequenceLength=sum(LengthSeq);

%-----
% Display configuration DATA -----
f = figure('Position',[718 613 424 246],'Resize','off');
dat1 = [TsDisplay, numberSlots, [0 Seq]', [0 LengthSeq]'];
cnames = {'Tint [ms]','#Slots', 'Sequence*', 'Length'};
rnames = {'General',
'Seq0','Seq1','Seq2','Seq3','Seq4','Seq5','Seq6','Seq7','Seq8','Seq9'};
t =uitable('Parent',f,'Data',dat1,'ColumnName',cnames,'RowName',rnames, ...
    'Position',[12 12 404 230]);
set(t,'ColumnWidth',{80})

%-----
% Start Reading Radiometric Data -----
%-----
% Opening the file
fid = fopen(DATA_filename);
content=fread(fid,'uint32','ieee-le');

%-----
% Reading the data in 1024 bytes chunks
%-----
ADC1=content(1:3:end);           % 1:3 samples belong to ADC1
ADC2=content(2:3:end);           % 2:3 samples belong to ADC2
AuxData=content(3:3:end);        % 3:3 samples belong to AuxData

%-----

```

```

%--- Separating each channels for each ADC
%-----

Ch1=mod(ADC1, 2^16);      % Less Significant Byte
Ch2=(ADC1-Ch1)/2^16 ;    % Most Significant Byte
Ch3=mod(ADC2, 2^16);     % LSB
Ch4=(ADC2-Ch3)/2^16 ;   % MSB
%-----

% Converting Counts to Voltage
%-----

Ch1Voltages=4.01*((2^14)-1-Ch1)./((2^14)-1);
Ch2Voltages=4.01*((2^14)-1-Ch2)./((2^14)-1);
Ch3Voltages=4.01*((2^14)-1-Ch3)./((2^14)-1);
Ch4Voltages=4.01*((2^14)-1-Ch4)./((2^14)-1);
%-----

%--- Getting Time Information
%-----

time=linspace(0, 1e-3*Ts*(length(Ch1)-1),length(Ch1));
timelabel=sprintf('Time [s] - {deltaT = %0.5g ms}', Ts);
%-----

%--- Extracting the Auxiliar Data Information
%-----

strAuxData=dec2bin(AuxData,24);
motorPosition=bin2dec(strAuxData(:,11:24));
DickeSwitch=bin2dec(strAuxData(:,10));
NS1=bin2dec(strAuxData(:,9));
NS2=bin2dec(strAuxData(:,8));
NS3=bin2dec(strAuxData(:,7));
RF_ONOFF=bin2dec(strAuxData(:,6));
res1=bin2dec(strAuxData(:,5));          % Not used!

```

```

res2=bin2dec(strAuxData(:,4));           % Not used!
res3=bin2dec(strAuxData(:,3));           % Not used!
trash=bin2dec(strAuxData(:,1:2));        % Not used!

%-----
% sequence data should match the information displayed in the slots and
% sequence Figure.
%-----

sequencedata=16*NS3+ 8*NS2 +4*NS1 +2*DickeSwitch + RF_ONOFF;

%-----

% Ploting Auxiliar data: Motor position and Control Signal Flags
%-----

figure(112)
subplot(2,1,1),plot(time, motorPosition.*360/2^14, 'r.'), grid on, hold on
title('Motor Position')
ylabel('[Degrees]'), xlabel(timelabel)
subplot(2,1,2), plot(time,RF_ONOFF,'y*'), grid on, hold on
subplot(2,1,2), plot(time,DickeSwitch, '.'),
subplot(2,1,2), plot(time,NS1,'r.'), grid on, hold on
subplot(2,1,2), plot(time,NS2,'g.'),
subplot(2,1,2), plot(time,NS3,'k.'),
legend('RF ON/OFF', 'Dicke Switch', 'NS1', 'NS2', 'NS3', 0)
title('Control Signal Flags')
ylabel('Flag value [1/0]'), xlabel(timelabel)

%-----

% Ploting Auxiliar data: Control signal sequences
%-----

figure(116)
SeqLen=2;

```

```

subplot(5,1,1),
plot(time(1:SequenceLength*SeqLen),RF_ONOFF(1:SequenceLength*SeqLen),'y*'),
grid on, title('RF ON/OFF')
subplot(5,1,2),
plot(time(1:SequenceLength*SeqLen),DickeSwitch(1:SequenceLength*SeqLen),
'.'),grid on, title('DickeSwitch')
subplot(5,1,3),
plot(time(1:SequenceLength*SeqLen),NS1(1:SequenceLength*SeqLen),'r.'), grid
on, title('NS1')
subplot(5,1,4),
plot(time(1:SequenceLength*SeqLen),NS2(1:SequenceLength*SeqLen),'g.'), grid
on, title('NS2')
subplot(5,1,5),
plot(time(1:SequenceLength*SeqLen),NS3(1:SequenceLength*SeqLen),'k.'), grid
on, title('NS3')
%-----
% Plotting radiometric data: Acquired channels in Volts
%-----

figure(22)
subplot(2,2,1), plot(time,Ch1Voltages,'.'), grid on, hold on,
axis([0 time(end) 0 4])
ylabel('Volts'), xlabel(timelabel)
title(sprintf('Ch1 - std=%0.5g mv - mean=%0.5g v',
1000*std(Ch1Voltages(1024:end)), mean(Ch1Voltages(1024:end))))
subplot(2,2,2), plot(time,Ch2Voltages,'.'), grid on, hold on,
axis([0 time(end) 0 4])
ylabel('Volts'), xlabel(timelabel)
title(sprintf('Ch2 - std=%0.5g mv - mean=%0.5g v',
1000*std(Ch2Voltages(1024:end)), mean(Ch2Voltages(1024:end)) ))

```

```

subplot(2,2,3), plot(time,Ch3Voltages, '.'), grid on, hold on,
axis([0 time(end) 0 4])
ylabel('Volts'), xlabel(timelabel)
title(sprintf('Ch3 - std=%0.5g mv - mean=%0.5g v',
1000*std(Ch3Voltages(1024:end)), mean(Ch3Voltages(1024:end)) ))
subplot(2,2,4), plot(time,Ch4Voltages, '.'), grid on, hold on,
axis([0 time(end) 0 4])
ylabel('Volts'), xlabel(timelabel)
title(sprintf('Ch4 - std=%0.5g mv - mean=%0.5g v',
1000*std(Ch4Voltages(1024:end)), mean(Ch4Voltages(1024:end)) ))
%-----
% Plotting radiometric data: FFT of the channels
%-----

figure(28)
Fmax=1/(2*Ts*1e-3)
Tsamples=length(Ch1Voltages(1024:end));
Freq=linspace(-Fmax, Fmax, Tsamples);
subplot(2,2,1), plot(Freq,10.*log10(abs(fftshift(fft(Ch1Voltages(1024:end))-
mean(Ch1Voltages))))), grid on, hold on,
ylabel('fft [dB]'), xlabel('f [Hz]')
title(sprintf('Ch1 - std=%0.5g mv - mean=%0.5g',
1000*std(Ch1Voltages(1024:end)), mean(Ch1Voltages(1024:end)) ))
Tsamples=length(Ch2Voltages(1024:end));
Freq=linspace(-Fmax, Fmax, Tsamples);
subplot(2,2,2), plot(Freq,10.*log10(abs(fftshift(fft(Ch2Voltages(1024:end))-
mean(Ch2Voltages))))), grid on, hold on,
ylabel('fft [dB]'), xlabel('f [Hz]')
title(sprintf('Ch2 - std=%0.5g mv', 1000*std(Ch2Voltages(1024:end))))
Tsamples=length(Ch3Voltages(1024:end));

```

```

Freq=linspace(-Fmax, Fmax, Tsamples);
subplot(2,2,3), plot(Freq,10.*log10(abs(fftshift(fft(Ch3Voltages(1024:end))-
mean(Ch3Voltages))))), grid on, hold on,
ylabel('fft [dB]'), xlabel('f [Hz]')
title(sprintf('Ch3 - std=%0.5g mv', 1000*std(Ch3Voltages(1024:end))))
Tsamples=length(Ch4Voltages(1024:end));
Freq=linspace(-Fmax, Fmax, Tsamples);
subplot(2,2,4), plot(Freq,10.*log10(abs(fftshift(fft(Ch4Voltages(1024:end))-
mean(Ch4Voltages))))), grid on, hold on,
ylabel('fft [dB]'), xlabel('f [Hz]')
title(sprintf('Ch4 - std=%0.5g mv', 1000*std(Ch4Voltages(1024:end))))

%-----
%-----
%-----
% Parsing the data for system status and channel
%-----
%-----
%-----
%-----
% Identifying an index for each status
%-----

offset=2;
IndexNS1=find(NS1==1)+offset;
IndexNS2=find(NS2==1)+offset;
IndexNS3=find(NS3==1)+offset;
IndexRef=find(DickeSwitch==0)+offset;
IndexAnt=find(DickeSwitch==1&NS1==0&NS2==0&NS3==0)+offset;

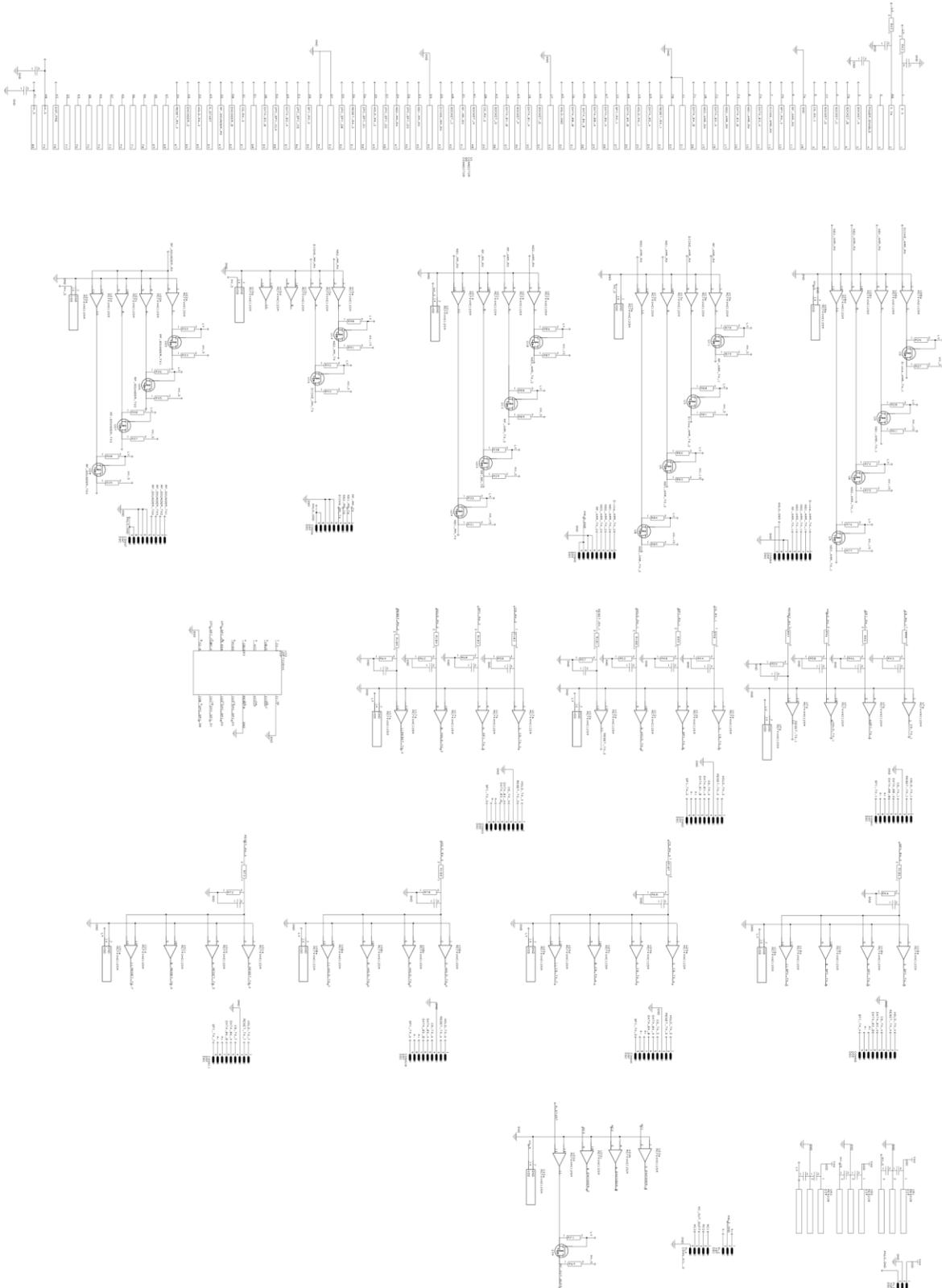
%-----

% Plotting radiometric data: Parsed channel in volts

```

```
%-----  
figure(9900), hold on, grid on,  
plot(time(IndexAnt(1:end-10)), Channel2Plot(IndexAnt(1:end-10)), 'g.')  
plot(time(IndexNS1(1:end-10)), Channel2Plot(IndexNS1(1:end-10)), 'k.')  
plot(time(IndexNS2(1:end-10)), Channel2Plot(IndexNS2(1:end-10)), 'b.')  
plot(time(IndexNS3(1:end-10)), Channel2Plot(IndexNS3(1:end-10)), 'm.')  
plot(time(IndexRef(1:end-10)), Channel2Plot(IndexRef(1:end-10)), 'c.')  
legend('Ant', 'NS1', 'NS2', 'NS3', 'Ref', 0)
```

Appendix VI Buffer Board Schematic



List of Acronyms and Abbreviations

ADC – Analog to Digital Converter

ANLG GND – Analog Ground

BNC - Bayonet Neill–Concelman

CCL – Communications Circuits Laboratory

CS – Chip Select

CSU – Colorado State University

DC – Direct Current

DE-9 – 9 Pin D-Subminiature

DMOS – Double-Diffused Metal Oxide Semiconductor

DIG GND –Digital Ground

FFT – Fast Fourier Transform

FPGA – Field Programmable Gate Array

GPS – Global Positioning System

HAMSR – High Altitude MMIC Sounding Radiometer

HPBW – Half-Power Beamwidth

IIP – Instrument Incubator Program

IMU – Inertial Measurement System

JPL – Jet Propulsion Laboratory

MMIC – Monolithic Microwave Integrated Circuit

MOSFET – Metal-Oxide Semiconductor Field Effect Transistor

MSL – Microwave Systems Laboratory

MSPS – Mega Samples per Second

NASA – National Aeronautics and Space Administration

NCAR – National Center for Atmospheric Research

PCB – Printed Circuit Board

RF – Radio Frequency

RMS – Root Mean Square

SDK – Standard Development Kit

SAR – Successive Approximation Register

SCLK – Serial Protocol Interface Clock

SMA – Sub Miniature Version A

SOIC – Standard Outline Integrated Circuit

SOT – Small Outline Transistor

SPI – Serial Protocol Interface

SPICE - Simulation Program with Integrated Circuit Emphasis

SWOT – Surface Water and Ocean Topography

UCLA – University of California Los Angeles

USB – Universal Serial Bus