THESIS

MODELING AND DESIGN OF A CURRENT MODE CONTROL BOOST CONVERTER

Submitted by

Hong Yao

Department of Electrical and Computer Engineering

In partial fulfillment of the requirements

For the Degree of Master of Science

Colorado State University

Fort Collins, Colorado

Fall 2012

Master's Committee:

Advisor: George J. Collins

Tom W. Chen
Siddharth Suryanarayanan
Hiroshi Sakurai

ABSTRACT

MODELING AND DESIGN OF A CURRENT MODE CONTROL BOOST CONVERTER

The boost or step up converter produces an undesirable Right-Half Plane Zero (RHPZ) in the small signal analysis of the "Duty Cycle Control to Output Voltage" transfer function. It is well documented that the boost converter has the reputation of low-performance and stability is complicated due to the RHPZ which makes Voltage Mode Control (VMC) very hard to implement. Even when Current Mode Control (CMC) is applied in the topology of converters operating in Continuous Conduction Mode (CCM), the current feedback loop becomes unstable if the duty cycle exceeds 0.5---the instability is known as Subharmonic Oscillation.

This research presents the theoretical analysis of the origin of the RHPZ and the modeling of a current mode control boost converter operating in continuous conduction mode. It details how to properly design both the control loop and the compensation loop to maintain the stability of the current-mode regulator. The simulation results and experimental results are given and contrasted based on a 3.5V-5.5V DC input, 12V DC output, and 1.3MHz switch frequency boost converter design.

ACKNOWLEDGEMENTS

This research project would not have been possible finished without the support of many people. I would like to thank all the people who have helped and inspired me through the duration of my studies at Colorado State University.

I would like to express my deepest gratitude to my advisor, Dr. George Collins, not only for his invaluable guidance but for his encouragement and support in various ways which exceptionally inspire and enrich my growth as a student. The opportunities he provided to me have made great difference in my life that I had never dreamed of.

I would like to express my gratitude to my thesis committee members for their valuable feedback. I would like to thank Dr. Tom Chen for helping me on many occasions. I benefited a lot from his good teaching in Analog IC design course which have provided me a strong background in understanding IC controller in my thesis research. I would like to thank Dr. Siddharth Suryanarayanan for helping me with numerous questions in Electrical Power Quality and being part of the committee. I would also like to thank Dr. Hiroshi Sakurai for kindly agreeing to be in my committee.

I would also like to express my gratitude to my classmates and friends Hai Chi, Haonan Chen, zheng Li, Xiao Chang, Sam Choi, Michael Kabala and all other friends for their support and helping me get through some difficult times. Thanks for the friendship and unforgettable memory at CSU.

I would like to thank my employer Analog Device, Inc. for providing the internship opportunity and laboratory facilities. I would like to thank Luca Vassalli, who has always been there and helped me to solve the problems I encountered. My research would not have been possible without his help and inspiration. Many thanks to Kevin Tompsett for his patience and great efforts to explain things clearly and simply on wide variety of research related issues. Many thanks to Jeff Weaver, Aaron Hanson, Glenn Maxey, John Ellenberger, Vong Philavanh and Wayne Rewinkel for all their help and providing an excellent atmosphere for doing research, and the associated working experience in Power Management area broadened my perspective on the practical aspects in industry.

Finally, to my beloved family, I would like to thank my husband, Dejiang Chen, for his understanding and a source of encouragement through the good times and bad. And I would also like to thank my children, Alec and Emily for the joy and inspiration they bring to me, filling me with energy and teaching me that life is a never ending learning process.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1 INTRODUCTION

1.1 Basic Operation of Boost Converter

A Boost converter or step-up switch mode power supply that can also be called a switch mode regulator. It steps up the input voltage to produce a higher output voltage. The popularity of a switch mode regulator is due to its high efficiency, compact size and low cost.

Generally, any basic switch power supply consists of the same basic power components: two switches, usually a MOSFET, and a diode *D*, an inductor and an output capacitor, all components are same as the buck and buck-boost converter but placed in different circuit locations. The boost converter was configuration is shown in Figure 1.1.

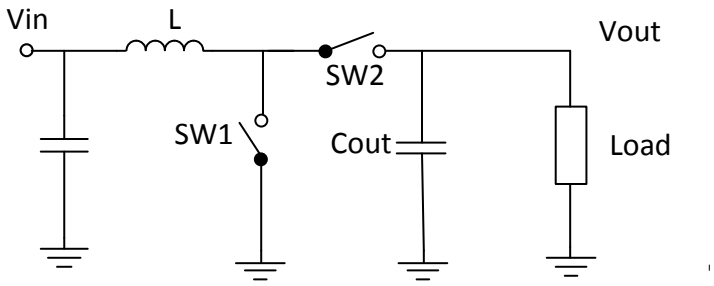


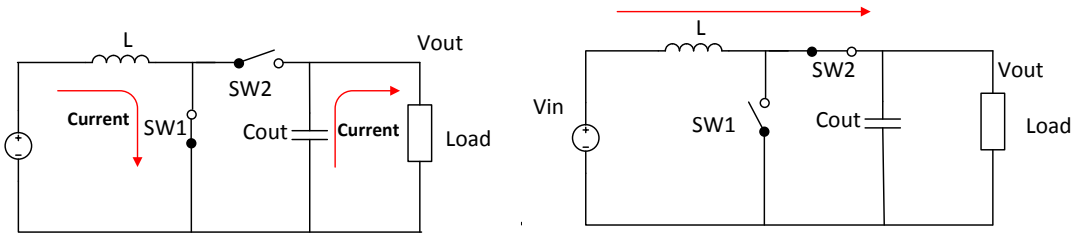
Figure 1.1 Basic boost converter topology

Deriving the output voltage conversion ratio will be done by evaluating the inductor Volt-Second balance as described in [1]. In steady state, the inductor average voltage must equal zero, which means that the energy flows into the inductor is equal to the energy flows out of the inductor over one complete switch cycle.

The operation of the boost converter is fairly simple, with an inductor and two switches that control the inductor. It alternates between connecting the inductor to source voltage to store energy in the inductor and discharging the inductor into the load.

During the ON time, shown in Figure1.2 a, the power switch SW1 is in ON state, inductor current flows through the inductor L and the power switch SW1 during the ON time or DTsw, resulting in the current ramping up waveform I_L, as shown in Figure1.3. During the power switch SW1 in the ON state, energy is first stored in the inductor and the voltage across the inductor is just the input voltage V_{in} which provides half of the inductor Volt-Second balance.

During the OFF time, shown in Figure1.2 b, the power switch SW1 is in OFF state, the energy in the inductor is transferred to the output capacitor C_{OUT} and to the load through switch SW2, the diode, further feeding the output network made of the capacitor and the load, the energy in the inductor is transferred to the output during the off time The voltage across the inductor is V_{in}-V_{out} during the switch off time.



(a) *(b)*

Figure 1.2 The two circuit configurations of boost converter (a) On Time (b) OFF time

The waveforms of current and voltage in a boost converter operating in continuous mode is shown in figure 1.3. The Junction of the inductor, switch SW1 and SW2 is called Switch Node and the voltage at the switch node is abbreviated on the figure as V_{SW}.

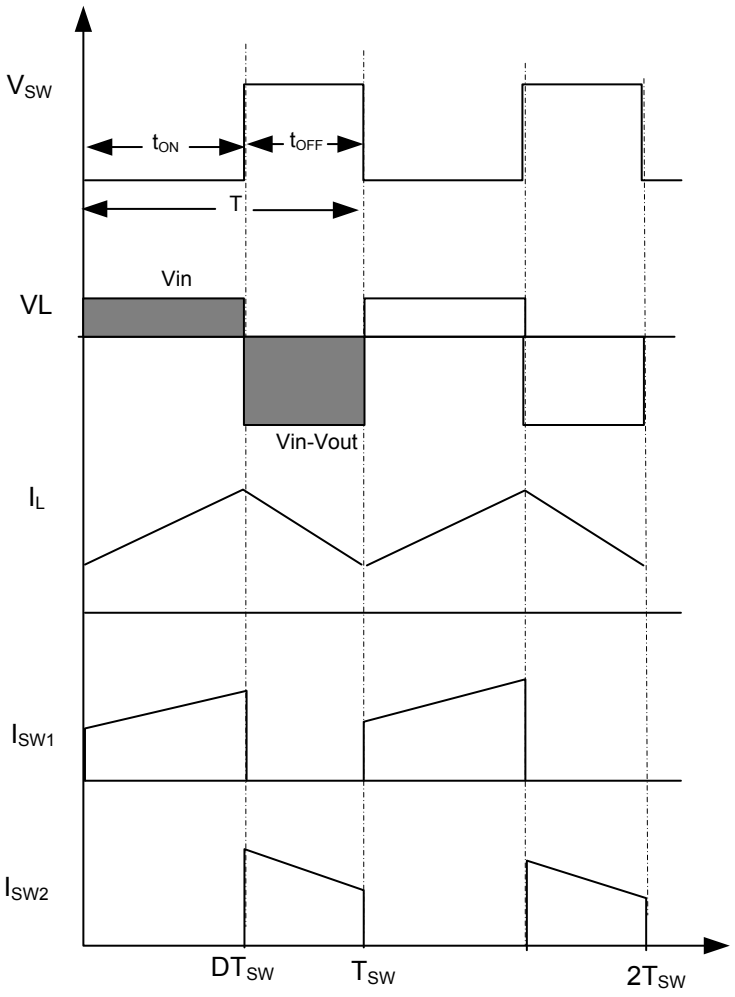


Figure 1.3 Waveforms of current and voltage in a boost converter operating in continuous conduction mode

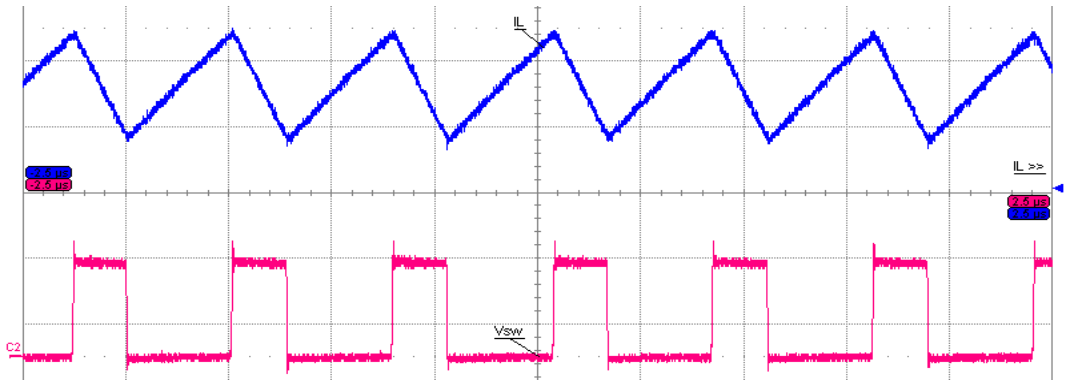
Applying inductor volt-second balance,$Vin * D\,T_{SW} + (Vin - Vout)(1 - D)T_{SW} = 0$, we get the voltage conversion ratio $M = \frac{V_{in}}{V_{out}} = \frac{1}{1-D}$.

where D is the PWM Duty cycle, or the ratio of the time SW1 is on, Ton, to switch period Tsw $D = \frac{T_{ON}}{T_{SW}}$.

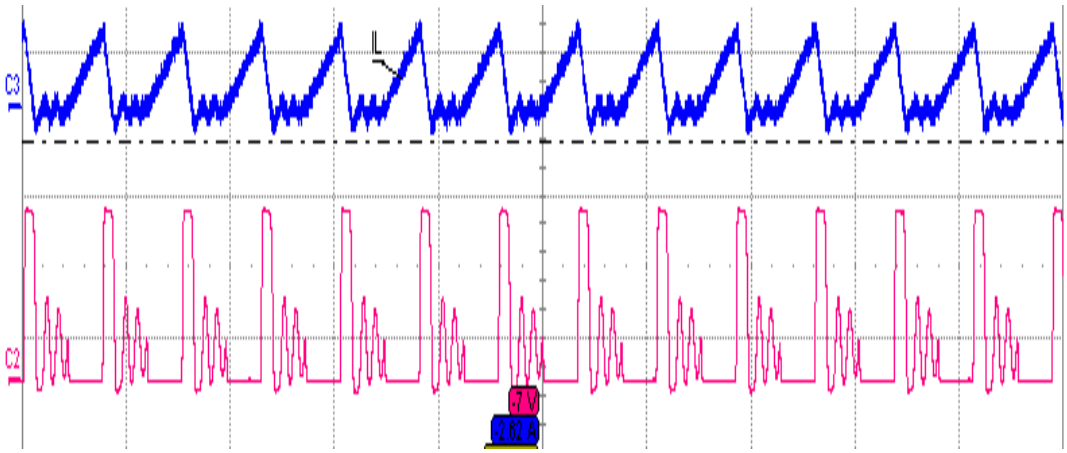
1.2 Modes of Operation: CCM and DCM

The dc-dc converters have two fundamentally different modes of operation: Continuous-Conduction Mode (CCM) and Discontinuous-Conduction Mode (DCM). The boost converter and its control are designed based on both modes of operation.

In the Continuous Conduction mode, the inductor current flows continuously that is the inductor current is always above zero throughout the switching period as shown in Fig 1.4a. The blue line represents the inductor current and the red line represents the switch node voltage. The inductor current zero line is below the lower tips of the inductor current and that's the important distinction between these two conduction modes. When the boost converter operates in CCM mode, the output voltage can be controlled by controlling the duty cycle D. The input and output voltage conversion ratio is given by $M = \frac{V_{in}}{V_{out}} = \frac{1}{1-D}$.



(a) CCM



(b) DCM

Figure 1.4 Inductor Current (blue) and switch node voltage (red) waveforms (a) CCM operation *(b) DCM* operation

In the Discontinuous Conduction Mode, the inductor current is discontinuous, that is inductor current reaches zero before the end of each switching period, as shown in Figure 1.4 (b). As the DC load current is reduced to a value that causes the average inductor current to be less than half the inductor ripple current. When the inductor current becomes zero, the power to the load is supplied by the capacitance alone. In DCM, the output voltage depends on the circuit component values and the duty ratio of the switch. The input and output voltage conversion ratio is $M = \frac{1+\sqrt{1+4D_1^2/K}}{2}$, where $K = \frac{2L}{R_{load}T_s}$, D1 is the duty cycle when the transistor is ON.

In DCM, when the instantaneous inductor current reaches zero during the cycle, ringing can be observed in the waveforms of the inductor current and MOSFET drain voltage (switch node) due to the resonant circuit formed by inductor and the total capacitance from the switch node to GND, including parasitic capacitors of the switches and any parasitic capacitances from the PCB. The ringing can produce undesirable noise at the output.

The two different operating modes have significant influence on the performance of the converter. It's important to make a selection in which of these two modes the converter is to operate based on different application.

The advantages of CCM over DCM include the DC conversion ratio is independent of the load, which makes DC analysis of converters operating in CCM easier. While operating in DCM, the output voltage depends on the load and the duty ratio of the switch, which makes DC analysis of converters operating in DCM more complicated. Also, to deliver the same power in DCM as in CCM, the peak currents are higher, resulting in greater losses in the conduction paths leads to reduced efficiency and higher peak current can also cause switch stress and greater input and output current ripple that adversely affects EMC noise issues.

CHAPTER 2 BOOST CONVERTER CONTROL LOOP ANALYSIS

2.1 Transfer Function of the Open Loop Boost Converter

All converter system invariably requires feedback to regulate the output voltage, regardless of the variable loads and input ripple. In a small-signal analysis, transfer function is necessary for the design of a stable feedback loop for a converter whose output voltage is regulated.

Using AC equivalent circuit modeling method illustrated in [1], derive the boost converter small-signal equivalent circuit model shown in figure 2.1

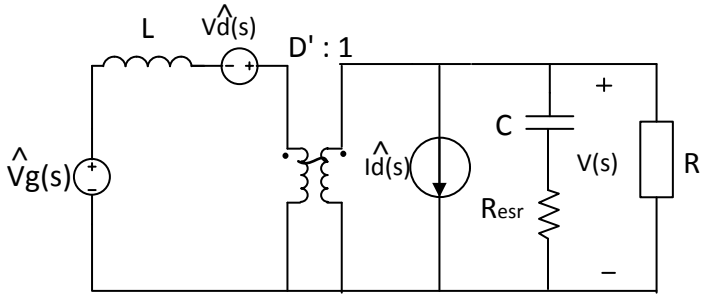


Figure 2.1 The small-signal equivalent circuit model of boost converter

As usual, in an AC analysis, all DC sources disappear. The converter has two independent AC input: one is the control input d(s) and the other is the line input $V_g(s)$. The AC output voltage can be expressed as the superposition of the two terms:

$$\hat{v}(s)=G_{vd}\,\hat{d}(s)+G_{vg}\,(s)\,\hat{V}_g(s) \qquad (2.1)$$

The Control to output transfer function G_{vd} can be determined as:

$$G_{vd}(s)=\left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{V}_g(s)=0} \qquad (2.2)$$

And the line to output transfer function G_{vg} can be determined as

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)}\Big|_{\hat{d}(s)=0} \quad (2.3)$$

To find the line to output transfer function$G_{vg}(s)$, set source $\hat{d}(s)$ to zero, moving voltage source $\hat{V}_g(s)$ and the inductor through the DC transformer, resulting the circuit in Figure 2.2

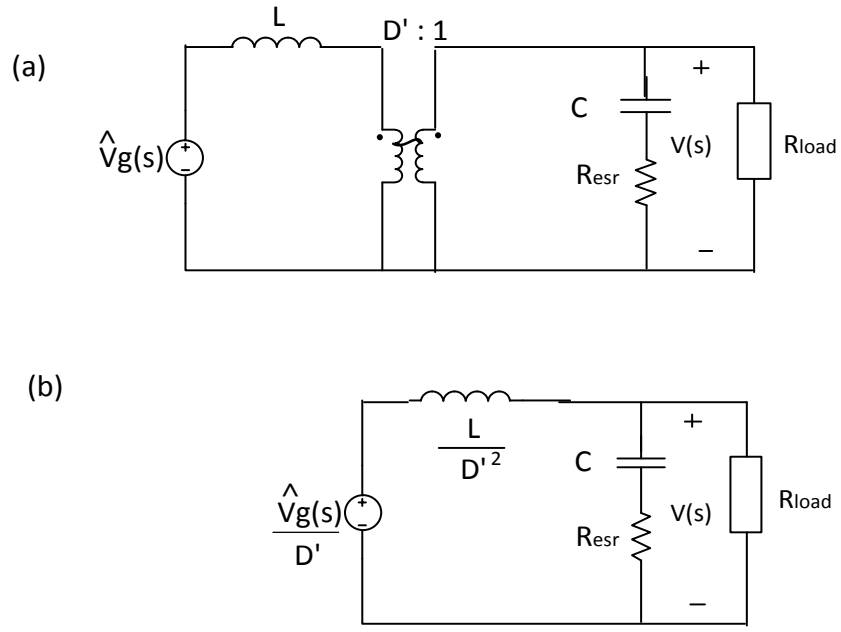


Figure 2.2 Manipulation of the boost equivalent circuit model to find $G_{vg}(s)$: (a) set source $\hat{d}(s)$ to zero (b) moving voltage source $\hat{V}_g(s)$ and the inductor through the DC transformer

Solving the circuit shown in Figure 2.2 (b) for $\hat{v}_g(s)$, the line to output transfer function can be expressed as:

$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)}\Big|_{\hat{d}(s)=0} = \frac{R_{load} \| (\frac{1}{sC} + R_{esr})}{D' \left[\frac{sL}{D'^2} + R_{load} \| \left(\frac{1}{sC} + R_{esr}\right)\right]} \quad (2.4)$$

where $D' = 1-D$

C is the capacitance of the output capacitor

R_{ESR} is the Equivalent Series Resistance of the output capacitor

Expand the parallel expression and, get

$$G_{vg}(s) = \frac{\frac{R_{load}(\frac{1}{sC} + R_{esr})}{R_{load} + (\frac{1}{sC} + R_{esr})}}{D'\left[\frac{sL}{D'^2} + \frac{R_{load}(\frac{1}{sC} + R_{esr})}{R_{load} + (\frac{1}{sC} + R_{esr})}\right]}$$

After rearranging,

$$G_{vg}(s) = \frac{(1 + sR_{esr}C)}{D'\left[1 + s(\frac{L}{D'^2 R_{load}} + R_{esr}C) + s^2 \frac{LC(R_{load} + R_{esr})}{D'^2 R_{load}}\right]} \quad (2.5)$$

The boost converter exhibits the line to control transfer function comprising two poles and one ESR origin Zero.

To find the control to output transfer function $G_{vd}(s)$, set source $\hat{V}_g(s)$ to zero, moving voltage source $V\hat{d}_s(s)$ and the inductor through the DC transformer, resulting the circuit illustrated in Figure2.3

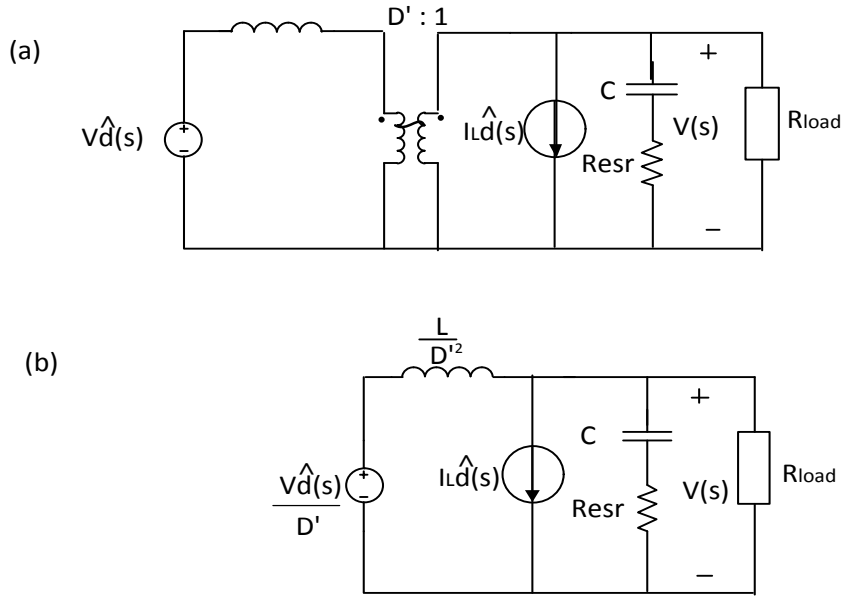


Figure 2.3 Manipulation of the boost equivalent circuit model to find $G_{vd}(s)$: (a) set source $\hat{V}_g(s)$ to zero (b) moving voltage source $\hat{d}(s)$ and the inductor through the DC transformer

Figure2.3 (b) includes $\hat{d}$ controlled voltage source $\frac{V\hat{d}(s)}{D'}$ and $\hat{d}$ controlled current source$I\hat{d}(s)$. Appling the principle of superposition, the control to output transfer function $G_{vd}(s)$ can be expressed as:

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)}\bigg|_{\hat{V}_g(s)=0} = \frac{V\left[R_{load}\|(\frac{1}{sC} + R_{esr})\right]}{D'\left[\frac{sL}{D'^2} + R_{load}\|\left(\frac{1}{sC} + R_{esr}\right)\right]} + I_L\left[\frac{sL}{D'^2}\middle\| R_{load}\|\left(\frac{1}{sC} + R_{esr}\right)\right]$$

where C is the capacitance of the output capacitor

R_{ESR} is the Equivalent Series Resistance of the output capacitor

Expand the parallel expression and simplify the equation using the DC relationship $I_L = \frac{V}{D'R_{load}}$, get:

$$G_{vd}(s) = \frac{V(1 + sR_{esr}C)(1 - s\frac{L}{R_{load}D'^2})}{D'\left[1 + s(\frac{L}{D'^2R_{load}} + R_{esr}C) + s^2\frac{LC(R_{load} + R_{esr})}{D'^2R_{load}}\right]} \quad (2.6)$$

Hence, the boost converter exhibits the control to output transfer function comprising two poles determined by the denominator of Equation 2.6, one ESR Zero and most importantly one Right Half Plane Zero which are given by Equation2.7 and 2.8 respectively. The later zero causes closed loop instability issues as detailed herein.

$$\omega_z = \frac{1}{R_{esr}C} \quad (2.7)$$

$$\omega_{rhpz} = \frac{R_{load}D'^2}{L} \quad (2.8)$$

2.2 Physical Origin of Right Half Plane Zero (RHPZ)

The small-signal mathematical analysis of boost converters reveals the presence of The Right half plane Zero (RHPZ) in the transfer functions of the control to the output. The RHPZ occurs in the boost converter circuit operating in Continuous Conduction Mode (CCM). It has the following normalized expression:

$$G(s) = (1 - \frac{s}{\omega_0}) \quad (2.9)$$

The RHPZ has the same 20 dB/decade rising gain magnitude as a conventional left-half plane zero, $\|G(\omega)\| = \sqrt{1 + (\frac{\omega}{\omega_0})^2}$, exhibiting the magnitude response as a left half-plane Zero, yet the phase response as a pole with the phase lag given by $\angle G(\omega) = -\tan^{-1}(\frac{\omega}{\omega_0})$.

Figure 2.4 illustrates the current waveform variation for a boost converter operating in the Continuous Conduction Mode (CCM). During the ON time, the inductor current I_L flows through the MOSFET and during the OFF time, the inductor current I_L flows through the output diode. The ripple goes into the output capacitor and average output capacitor current is zero. So the average load current is the diode average current I_D.

$$I_D = (1 - D)I_L = I_{load} \qquad (2.10)$$

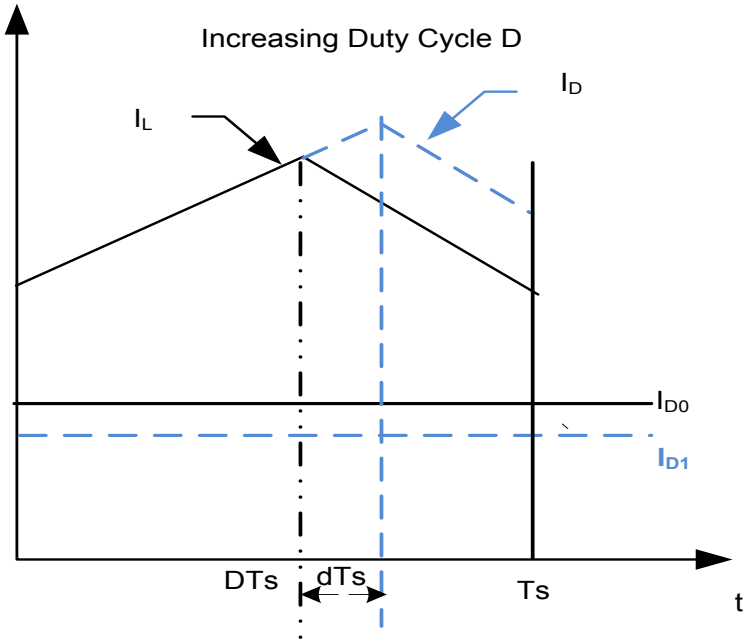


Figure 2.4 The current decreases in the output diode with increasing duty cycle D [9]

When there is requirement for increasing the load current, the input current will increase.

$$Pout=Vout*Iout=ɲ* Vin*Iin \qquad (2.11)$$

To increase the input current, the inductor current need to be increased as the average input current equals to the inductor current. Increasing the inductor current requires increasing the duty cycle D, the associated relationship is shown in Equation 2.12.

$$\Delta I_L = \frac{V_{in}}{L} D\, T_s \qquad (2.12)$$

The increased duty cycle causes decreased OFF time (1-D) Ts which leads to LESS Current to Load. In Figure 2.4, we can see the current in the inductor increasing with a slope imposed by input voltage Vin during the ON time and decreasing with a slope imposed by the voltage across the inductor, V_L = Vout -Vin , during OFF time. And the diode current jumps to the peak inductor current as soon as the switch opens and equals to the inductor current during OFF time. The diode average current in the black waveform is I_{D0}, The blue waveform on the right side of the figure shows that the duty cycle has slightly increased. The inductor current peaks a little bit higher, yet given the reduction of the (1−D) term in Equation 2.10 due to the increase of D, the average current I_{D1} is lower than before, resulting less current to the load. The initial behavior of system appears to have positive feedback.

Figure 2.5 presents the bode plot of the power stage of a boost converter without compensation. As shown in Equation 2.8., the location the RHPZ is $\omega_{\mathrm{rhpz}} = \frac{\mathrm{R_{load}D'^2}}{\mathrm{L}}$ .The presence of a Right Half-Plane Zero tends to push out the crossover frequency and decreases the phase margin.

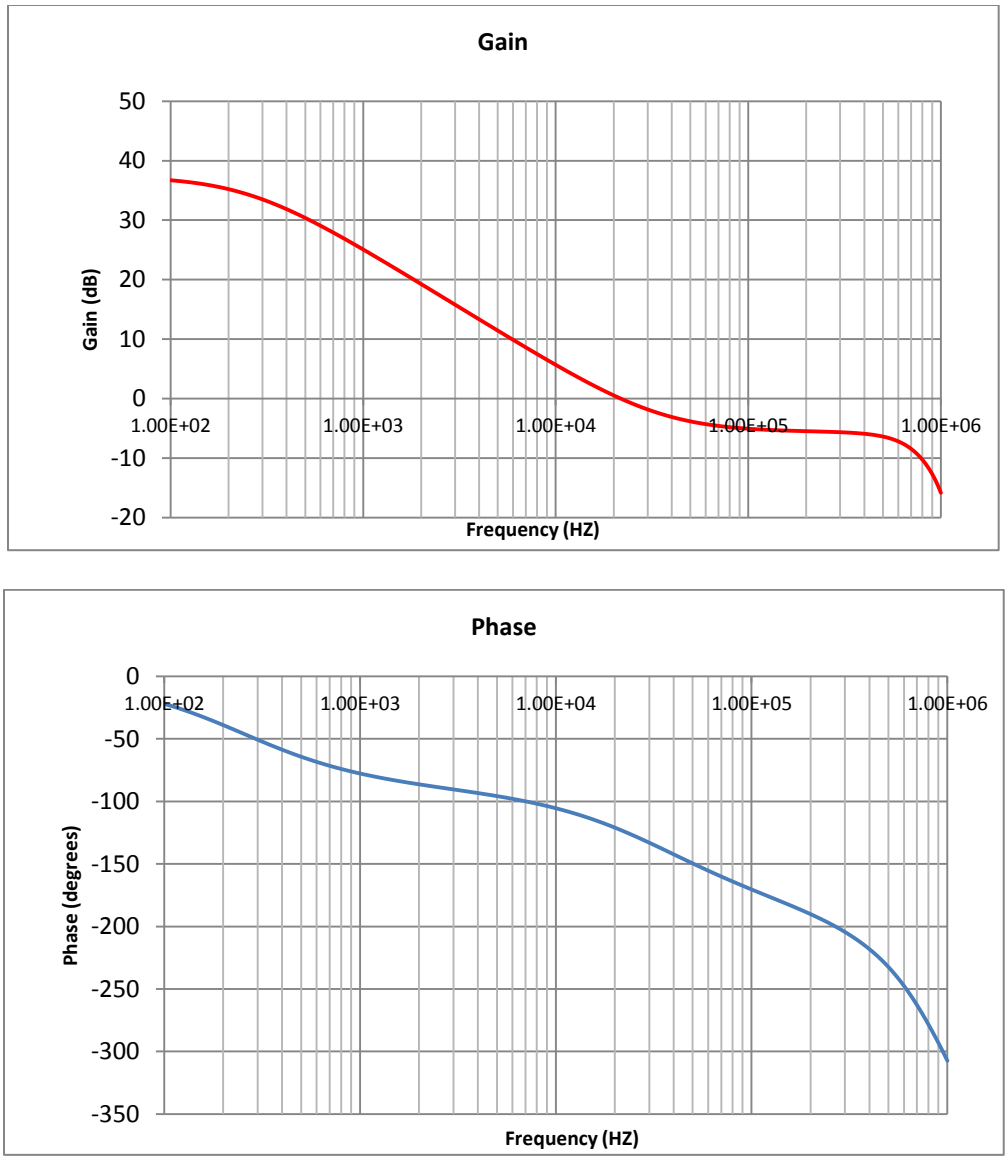


Figure 2.5 RHPZ observed in the power stage from the output of the error amplifier (COMP pin) to the output

2.3 Voltage Mode Control

To regulate the output voltage, Pulse-Width Modulation (PWM) is necessary for adjusting Duty Cycle to obtain the desired voltage output. There are two control methods for boost converter: Voltage Mode Control (VMC) and Current Mode Control (CMC).

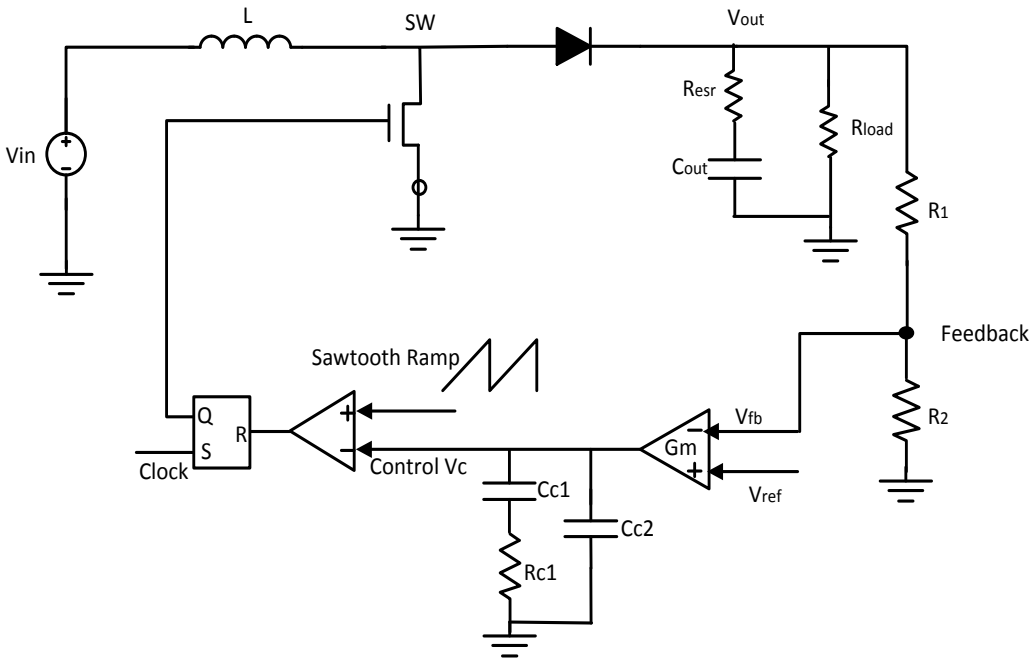


Figure 2.6 Control circuit of the boost converter with VMC

The block diagram of a VMC boost converter is illustrated in Figure 2.6. The converter output voltage is monitored through a voltage divider. The voltage at feedback is compared to the reference voltage by the error amplifier to create an error current through the transconductance of the error amplifier. After going through the compensation impedance, the error current was converter to control voltage and was connected to the Pulse Width Modulator (PWM) that drives the MOSFET.

In voltage–mode control, this control voltage is compared with a sawtooth ramp. When the converter output voltage changes, the control voltage Vc also changes and thus causes the duty cycle of the power switch to change. The higher the error voltage, the longer is the duty cycle. This change of duty cycle adjusts the output voltage to reduce to error signal to zero. The Control signal Vc, switch current and duty cycle waveforms are given in Figure 2.7

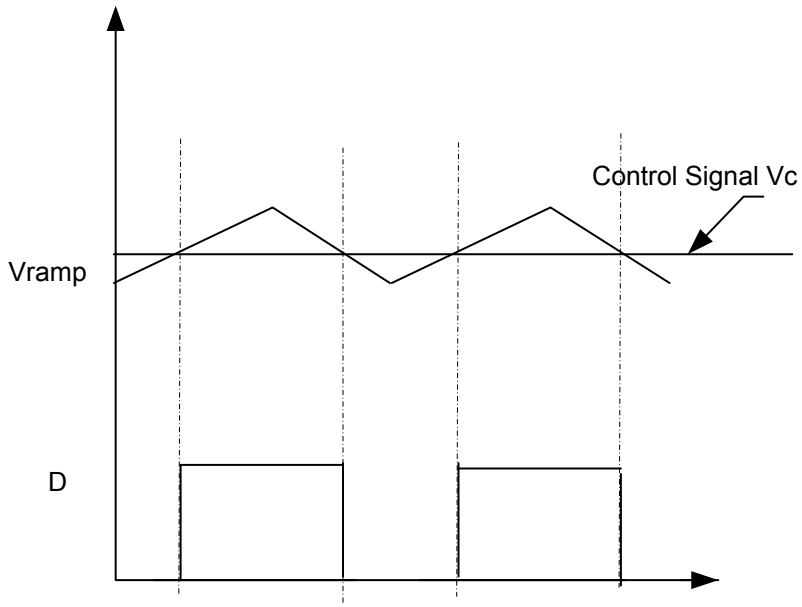


Figure 2.7 Switch current, control signal and Duty Cycle D of the VMC

The control to output transfer function for the boost converter under voltage mode control shown in Figure 2.6 is given by [15] shown in Equation 2.13:

$$\frac{\hat{v}(s)}{\hat{d}(s)} = \frac{V_g(1 + sR_{esr}C)(1 - s\frac{L}{R_{load}D'^2})}{D'^2\left[1 + \frac{s}{\omega_0 Q} + \frac{s^2}{{\omega_0}^2}\right]} \tag{2.13}$$

The resonance frequency ω_0 can be expressed as

$$\omega_0 = \frac{D'}{\sqrt{LC}} \tag{2.14}$$

Figure 2.8 shows the open loop bode plots of amplitude and phase of typical boost converter in continuous conduction mode under voltage Mode control for given the following parameters: Vin= 5.5V, Vout= 12V and Iout=0.8A, L= 10uH, Cout= 10uF, Resonance frequency ω_0=7KHZ, RHP zero 44. 6KHZ.

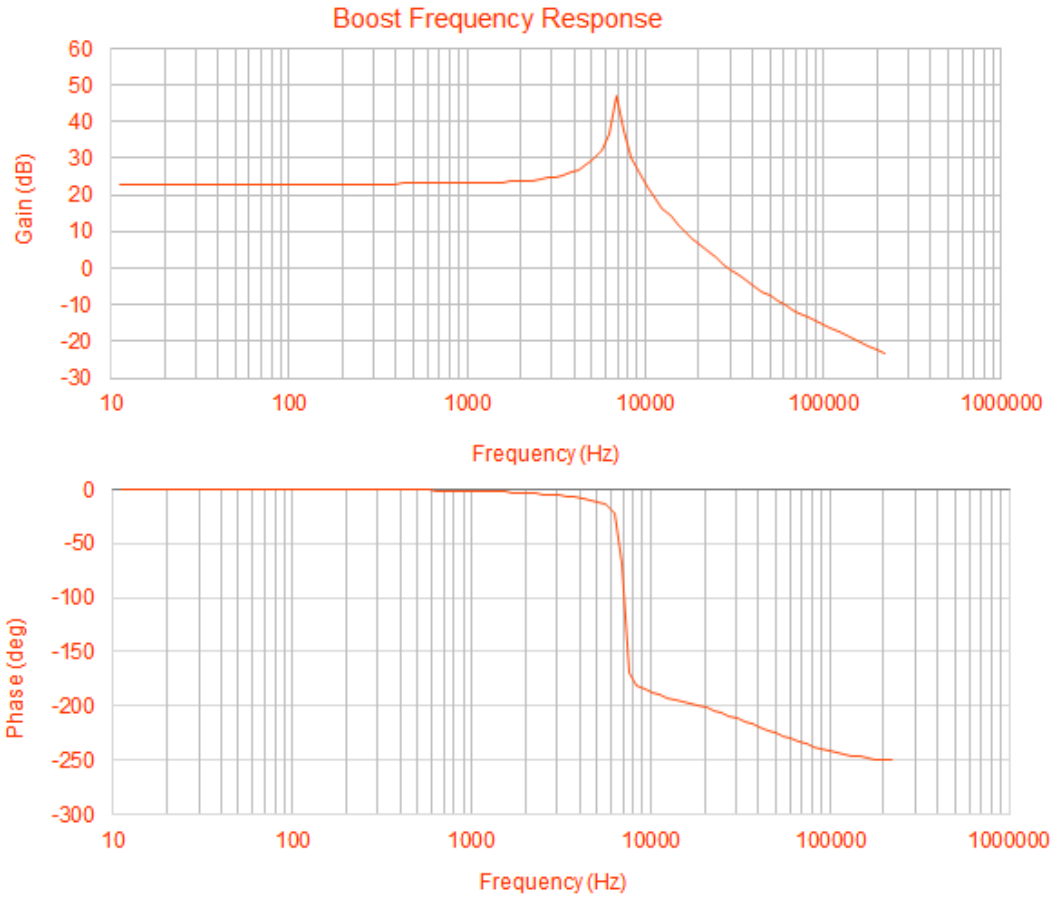


Figure 2.8 VMC boost converter open loop bode plot

Under Voltage-Mode Control, the sharp phase drop after the resonant frequency requires a type III compensator for the phase boost to stabilize the system. Also, different input voltage cause a shift of the resonance frequency of the LC filter which can be seen from Equation2.14.

2.4 Current Mode Control

2.4.1 Operation of Current Mode Control

Another control scheme which has wide application in industry is Current Mode Control (CMC) in which the converter output voltage is controlled by the inductor current.

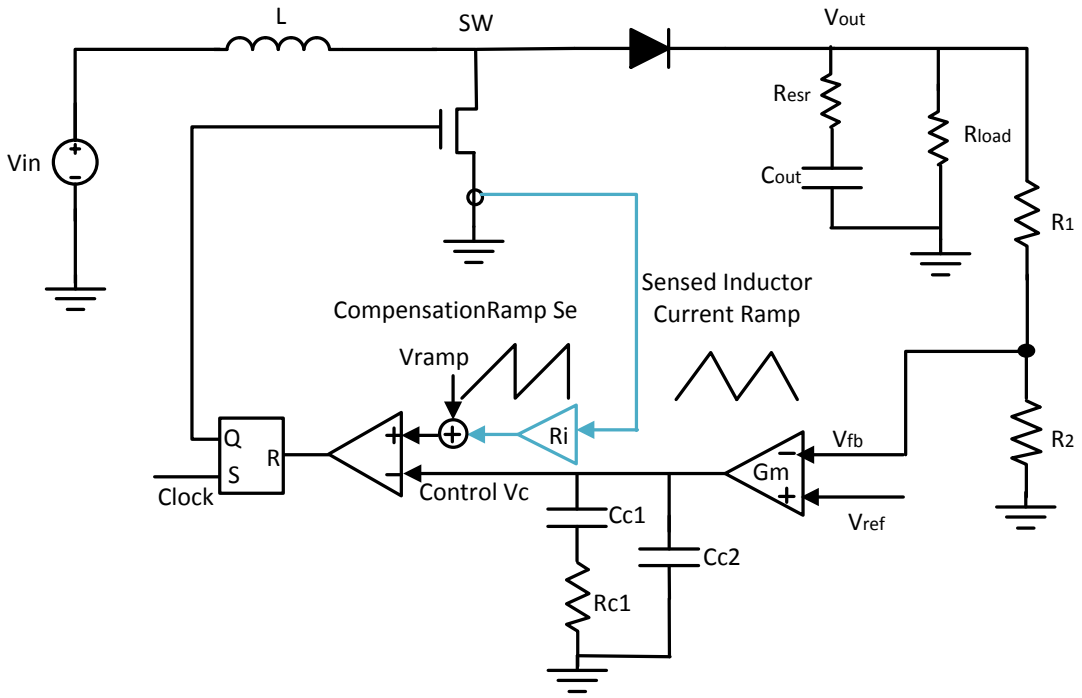


Figure 2.9 control circuit of the boost converter with CMC

The basic structure of a boost converter with current mode control is illustrated in Figure 2.9. The current feedback is the additional path which is different from the basic control block diagram of boost converter with voltage mode control. Rather than using a sawtooth ramp to control the duty cycle of the converter used in Voltage Control Mode, the current mode control regulates the peak of the inductor current with a control signal Vc.

At the beginning of the duty cycle DTs, A clock pulse initiates the switching period, the MOSFET is turned on. While the transistor conducts, its current is equal to the inductor current which ramps up with a positive slope Vin/L. The switch current is measured and converted to a voltage using current sensor resistor. When the sum of the sawtooth ramp Vramp and sensed voltage are greater than the control voltage, the controller turns the transistor switch off, and the inductor current decreases till next switching cycle. The duty-cycle of the PWM modulator is

thus adjusted to provide the necessary load current at the desired output voltage. The Switch current, control signal and Duty Cycle D of the CMC is illustrated in figure 2.10.

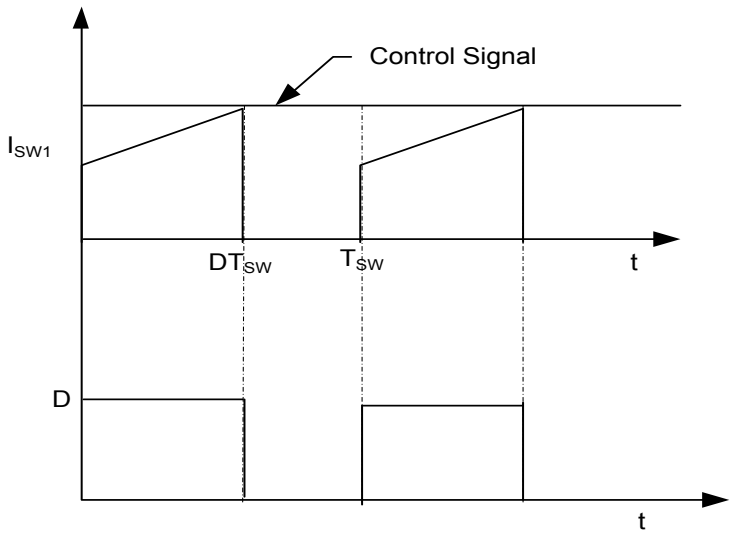


Figure 2.10 Switch current, control signal and Duty Cycle D of the CMC

As the converter regulates the peak inductor current through the control voltage, this scheme is called peak current-mode control [23]. The transistor duty cycle d(t) is controlled by the control voltage, the inductor current and the current sensor tranconductance of the converter. As the peak switch current equal to the peak inductor current, in many cases instead of sensing the inductor current directly, the switch current was sensed to reduce the power losses.

2.4.2 Subharmonic Oscillations

When current-mode control is applied in converters, or any topology of converter operating in continuous conduction mode, the difference between the average inductor current and the value of current when the sample is taken causes the instability if the duty cycle exceeds 50%. In some cases, the instability even occurs at lower duty cycles. Figure 2.11 shows the oscillation waveform of the inductor current and the voltage at the switch node. This instability is known as

subharmonic oscillation, which occurs when the inductor current does not return to its initial value at the start of the next switching cycle [12]. Subharmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. The perturbation increases from cycle to cycle, and the inductor current waveform can have a mountainous pattern that repeats on subsequent switching cycles or even have a chaotic behavior. If it's not damped, the current mode oscillation, like any other oscillation, will continue to ring and grow in amplitude which leads to the instability of the converter.

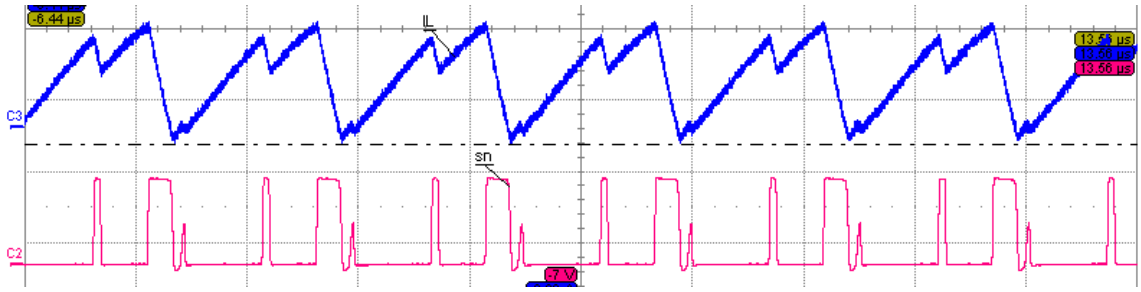
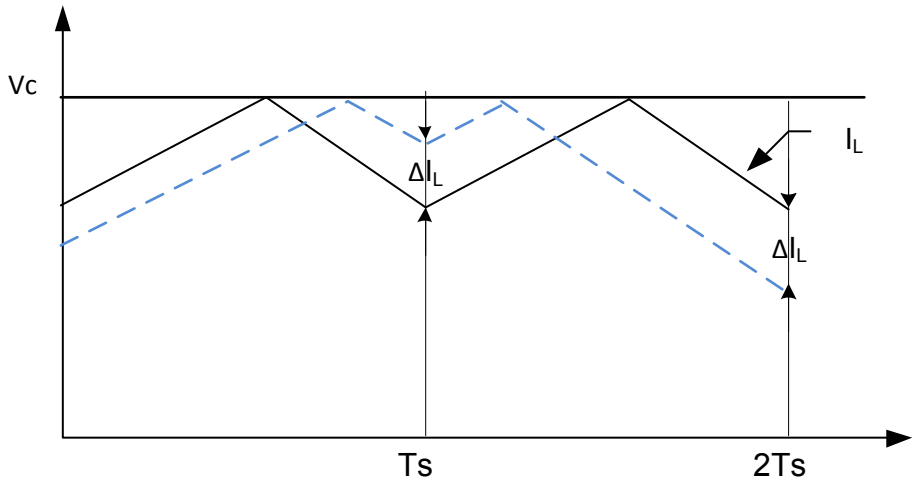


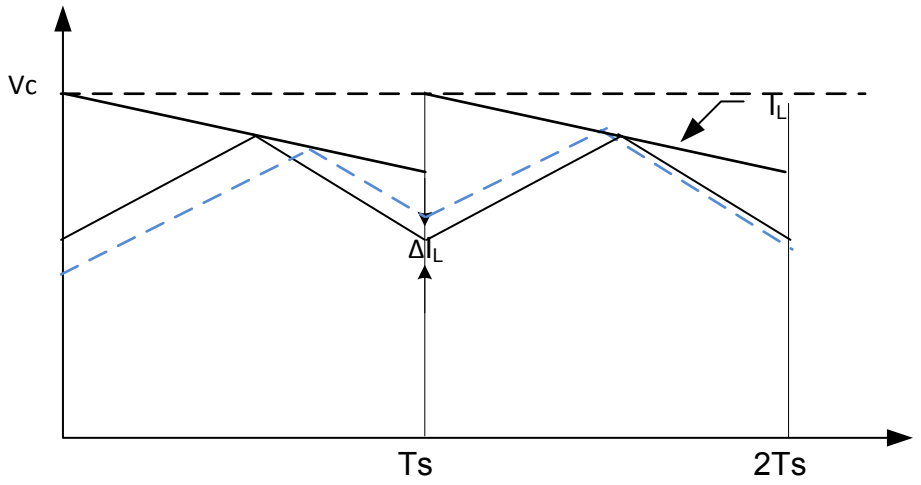
Figure 2.11 Sub harmonic oscillation waveform in Current Mode Control

3.4.3 Ramp Compensation in the feedback loop

Current–mode control is the industry standard method of controlling switching power supplies [13]. A control reference is used to regulate the peak current of the converter directly, simplifying the dynamic of the converter. However, in some application, the current feedback loop becomes unstable under certain operating conditions. Adding an external ramp, the slope compensation, to the current-sense signal prevents this oscillation.



(a)



(b)

Figure 2.12 Slope Compensation (a) without slope
(b) *adding a slope to the inductor current signal*

Figure 2.12 (a) shows the subharmonic oscillation in peak current –mode control with duty cycle exceeds 50%. However, the oscillation is damped by adding the slope compensation. Adding a slope compensation to the current signal is equivalent to subtracting a slope from the

error voltage (Vc), and the disturbance decreases at the end of the cycle, shown in Figure2.12 (b).

2.4.4 Small Signal Modeling of Current Mode control

The main advantage of current mode control is its simpler dynamics. This control method is simplified by viewing the inductor as a controlled current source in early analysis [13] as shown in figure 2.13

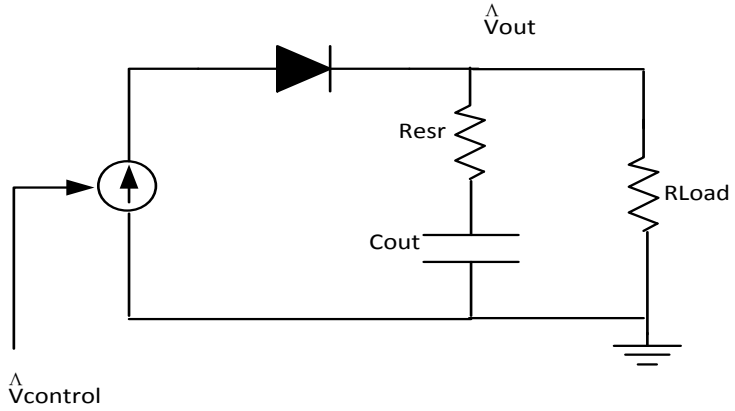


Figure 2.13 Boost converter simple average model

For the boost converter, the low frequency model of the control to output in current control mode has been found to be[13]:

$$f_p\ (s) = K\frac{(1+\frac{s}{\omega_z})(1-\frac{s}{\omega_{rhpz}})}{\left(1+\frac{s}{\omega_p}\right)} \qquad (2.15)$$

Where ω_z is the capacitor ESR Zero

ω_{rhpz} is the RHP zero

ω_p is the dominant-pole

And K is the DC Gain of the control to output transfer function and is given by[1]:

$$K = \frac{V_{out}F_m}{(1-D)(1+2\frac{F_m V_{out}}{(1-D)^2 R_{load}})} \tag{2.16}$$

Where D is the duty cycle.

Vout is the regulated output voltage

Rload is the equivalent load resistance

Fm is the modulator gain defined as the change in control voltage causes the duty cycle from go from 0 to 1[19]:

$$F_m = \frac{f_{sw}}{(S_e + S_n)} \tag{2.17}$$

Where f_{SW} is 1.3MHZ switch frequency and S_e is the slope of the added ramp

$$S_e = \frac{V_{pp}}{T_{sw}} \tag{2.18}$$

And S_n is the sensed inductor current slope $S_n = \frac{V_{on}}{L} R_i$, R_i is the current sensor gain from the inductor current to the sensed voltage connected to the PWM . The R_i of ADP1614 is 1/7 V/A. And Von is the voltage across the inductor during subinterval DTs when the inductor current is ramping up. For a boost converter, Von equals to the input voltage.

At low frequencies, the power stage has a response of dominant-pole which is determined by the time constant of the output capacitor and load resistor.

$$\omega_{p=} \frac{2}{R_{Load} C_{out}} \tag{2.19}$$

The current feedback does not change the capacitor ESR Zero which is located at

$$\omega_{z=}\frac{1}{R_{ESR}C_{out}} \tag{2.20}$$

The current-mode boost converter has the exact same RHP zero as the voltage-mode and the RHP zero is

$$\omega_{rhpz}=\frac{R_{load}(1-D)^2}{L} \tag{2.21}$$

Notice that the small-signal control to output transfer function contains one less pole than V(s)/d(s) in voltage mode control. The dynamics is simplified to the first order using current mode. Actually the other pole was moved to a high frequency near the converter switching frequency. Although the current mode control does not eliminate or move the right-half plane zero, it is easier to compensate as the current- mode looks like a single pole system at low frequency. In voltage-mode control, the sharp phase drop after the double pole response frequency requires type III compensation and that makes the converter hard to control.

The simple average model works fine under many conditions. But it doesn't model the oscillation of current mode control which is well known and documented. To model the subharmonic oscillation in the current mode system, a high frequency correction term need to added to the basic power stage transfer function, illustrated in Figure 2.14 .

The dynamic analysis of current mode involves many advanced techniques, including discrete-time and sampled-data modeling. This is essential to arrive at a model which explains all the phenomena observed in the converters and accurately predicts the control-to-output response and loop gain of the current-mode converter. Formula derivation of the high frequency correction is covered in [17], shown in Equation 2.22

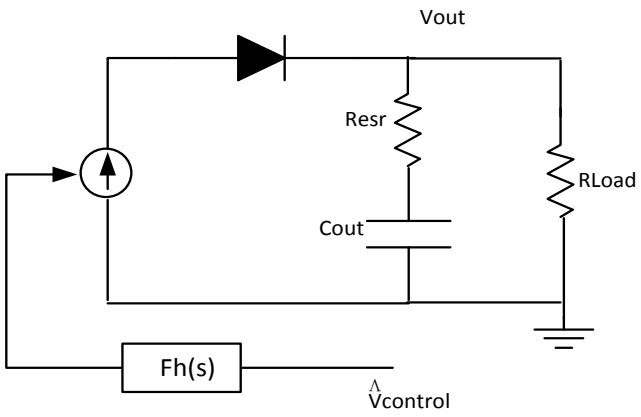


Figure 2.14 Current Mode control Boost converter enhanced model with high frequency correction

$$f_h\ (s) = \frac{1}{(1 + \frac{S}{\omega_n Q_p} + \frac{S^2}{\omega_n^2})} \tag{2.22}$$

The power stage has an additional pair of complex poles at half the switching frequency which, under certain conditions, it will create instability in the current feedback loop. The double poles oscillate at half of the switching frequency can be expressed as:

$$\omega_n = \frac{\pi}{T_{Sw}} = \pi * f_{sw} \tag{2.23}$$

The damping factor of these complex poles is controlled by the compensation ramp slope and the inductor current slope. And the damping is given by

$$Q_p\ = \frac{1}{\pi(m_c * D' - 0.5)} \tag{2.24}$$

The compensation ramp factor

$$m_c = 1 + \frac{S_e}{S_n} \tag{2.25}$$

When the transfer function has a high damping factor Q_P, the inductor current will oscillate back and forth when there is disturbance. If it's well damped, the inductor current will return quickly to the equilibrium after the disturbance. To ensure the stability of the converter current loop, a designer must make sure the damping factor Q_P of the double pole is one or less [13].

Although there are only two state variables in the converter, the resulting transfer function of the power stage is third-order, which is caused by the fact that the switching power converter is a nonlinear, time-varying system. The second-order double poles at half the switching frequency cannot be ignored even though they may be far beyond the predicted open loop crossover frequency [17].

CHAPTER 3 PRACTICAL CIRCUIT DESIGN

3.1 Objective

The objective is to design a boost converter that converts 3.5 - 5.5 V input to 12V output and supplies a load current of 0.8 A. The switching frequency is 1.3MHZ. Generally a faster switching frequency leads to small size of components, but the switching losses in the circuit increase.

The specifications of the boost converter are listed as follows:

Input voltage range: 3.5 -5.5 V

Nominal output voltage: Vout=12V Vout ripple < 0.2%

Maximum output current: Ioutmax=0.8A

Iout step=30% , Step error< 8%

Operating in Continues Conduction Mode

3.2 Components Selection

IC Solution

In order to implement the switching necessary for the boost converter to work, it is desirable to find an IC solution. This is important as some parameters for the calculations must be derived from the data sheet.

The ADP1614 integrated switch boost regulator, from Analog Device, Inc., is one such solution. It can boost a 2.5V to 5.5 V input voltage with the 4A IC peak current limit up to 20V output voltage. The Block Diagram of ADP1614 is shown in Figure 3.1[23]. And the schematic of the boost converter is shown in Figure 3.2

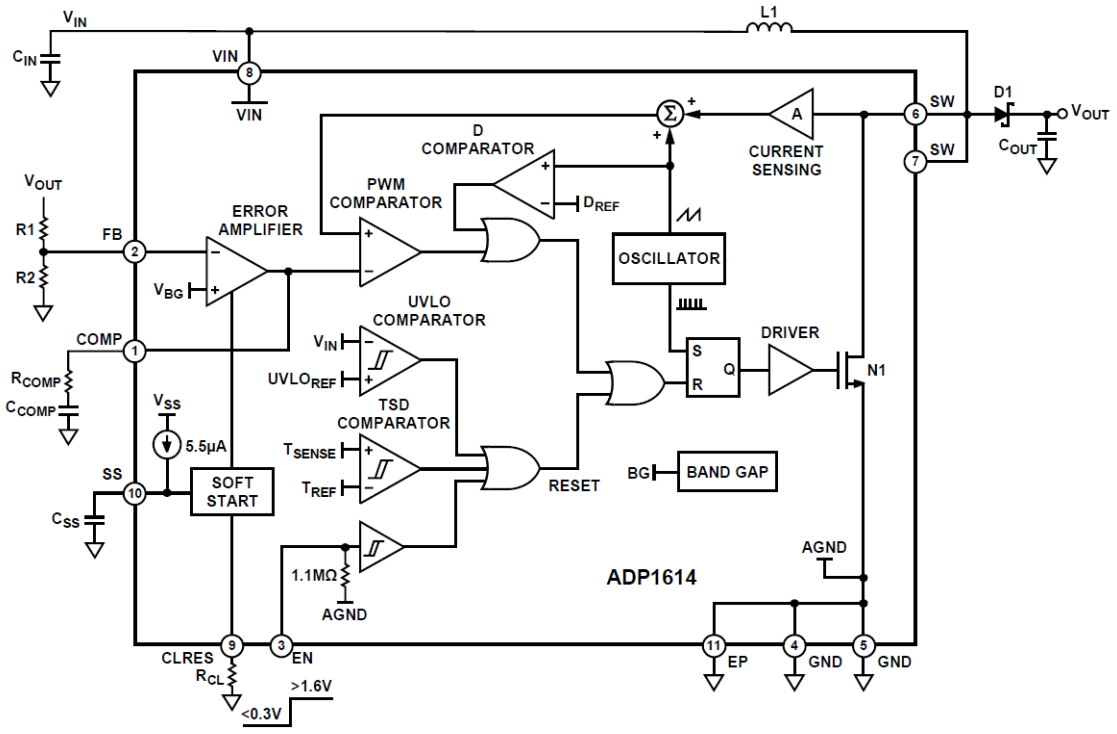


Figure 3.1 Block Diagram with Step-Up Regulator Application Circuit (courtesy of ADI)

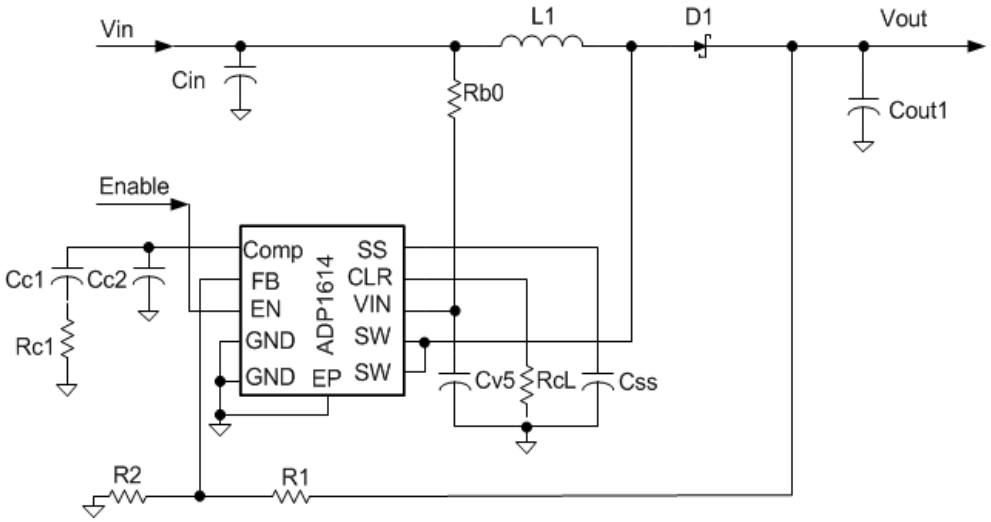


Figure 3.2 Schematic of the boost converter using ADP1614 (courtesy of ADI)

In this circuit, the output voltage Vout, is set through a voltage divider R1 and R2 from the output voltage to the FB input, shown in figure 3.2. Vout is determined by the ratio of fixed

resistors R1 and R2. These two resistors form a voltage divider that feeds a fraction of the output voltage back to the feedback (FB) pin, creating a closed-loop system. The system is at equilibrium when Vout is generating the desired output voltage and the R1 and R2 voltage divider feeds back 1.245V to the FB pin. The output voltage is regulated by the voltage reference Vref. When Vout is lower than the desired output voltage, the voltage fed back to FB is below 1.245V, the DC-DC converter IC attempts to deliver additional power until FB reaches 1.245V.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \tag{3.1}$$

Solving the above equation for R1 yields

$$R_1 = R_2 \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}}\right) \tag{3.2}$$

Using higher resistance values for R1 and R2 results in reduced output voltage accuracy due to the input bias current at the FB pin, however, using lower resistance value for R1 and R2 leads to higher quiescent current and therefore increases the power consumption. In this design for Vout=12V, select R1=165K Ω and R2= 19.1K Ω

Duty Cycle D

To determine the inductor current ripple, output voltage ripple, and slope-compensation factor in continuous conduction mode, it is necessary to determine the system duty cycle D. The duty cycle depends on input and output voltage and is given by:

$$D = 1 - \frac{V_{IN}}{V_{OUT} + V_F} \tag{3.3}$$

where Vout =12 V is the desired output voltage, Vin is the input voltage, and VF is the forward-voltage drop of the diode. A typical Schottky diode has a forward-voltage drop of 0.4 V. For given the input voltage range 3.5V-5.5V, the minimum duty cycle at maximum input voltage is 0.56 and the maximum duty cycle at minimum input voltage is 0.72.

Inductor Selection

The inductor is the most important because it determines the stability of the current sensor loop and the inductor current ripple. The peak-to-peak inductor ripple current is inversely proportional to the inductor value and is given by:

$$\Delta I_L = \frac{V_{in} DTs}{L} = \frac{V_{in} D}{f_{sw} L} \tag{3.4}$$

The minimum inductance is given by:

$$L_{min} = \frac{V_{in} D}{f_{sw} \Delta I_L} = \frac{D {V_{in}}^2}{f_{sw} V_{out} I_{out} \frac{\Delta I_L}{I_L}} \tag{3.5}$$

where f_{sw} is the switching frequency, and L is the inductance value.

The average inductor current I_L is given by

$$\mathrm{I_L} = \frac{\mathrm{I_{load}}}{\mathrm{D'}} \tag{3.6}$$

At Vinmin=3.5V, the inductor average current is the maximum, plug in the numbers Iload= 0.8A and $\mathrm{D'} = 1 - \mathrm{D} = 1 - 0.72 = 0.28$ into Equation 3.6, we get the $\mathrm{I_{Lmax}} = 2.84$ A.

For continuous conduction mode (CCM) operation, the peak inductor current is given by

$$I_{L\_peak} = I_L + \frac{\Delta I_L}{2} \tag{3.7}$$

As for inductor choice, the rated inductor saturation current needs to be well above the expected peak inductor current and the rated rms current value is greater than the maximum DC input current to the converter.

In discontinuous conduction mode (DCM) operation, the inductance required by the converter is much lower than the inductance required operating in CCM for the same load. Generally, inductors with lower inductance values are smaller in size and less expensive. Yet the peak current of the inductor in DCM is much higher than the peak current in the inductor operated in CCM converter, and the larger ripple current also increases the power losses in the inductor and the stress on the switch. Inductors with large inductance values result in less ripple current but they are bigger in size and more expensive.

Also ensure the winding resistance of the inductor will be low enough to limit power dissipation and overheating. And use shielded (closed field magnetic) structure when lower radiated EMI is required.

Output Capacitor Selection

The output capacitance of a power converter is a vital part of the overall system. It maintains the output voltage and affects stability of the regulator. The component parameters including ESR are part of the feedback control loop. The output capacitance detemines the position the dominant pole and therefore affect the stability boost converter.

The output capacitor greatly affects the output voltage ripple of the converter. The output voltage peak-to-peak ripple ΔVout can be approximated by

$$\Delta V_{out} = \frac{I_{load} t_{on}}{C_{out}} = \frac{I_{load} D}{f_{sw} C_{out}} \tag{3.8}$$

where I_{load} is the output load current, D is the duty cycle and can be expressed as $D = \frac{V_{out} - V_{in}}{V_{out}}$, f_{SW} is the switching frequency, C_{OUT} is the output capacitance. Choose the output capacitor based the equation as follows:

$$C_{out} \geq \frac{I_{load} * (V_{out} - V_{in})}{f_{sw} * \Delta V_{out} * V_{out}} \tag{3.9}$$

Substitute these values Iload=0.8A, V_{out} =12V, $V_{in} = 3.5V$, f_{sw} =1300KHZ, and ΔV_{out}=2%*Vout=0.024V into Equation 3.9, the capacitance for the output is about 11uF.

The capacitor ESR and ESL also affect the output capacitor impedance and thus the output voltage ripple. Multiple capacitors can be connected in parallel to reduce the effective ESR and ESL. Usually ceramic dielectric capacitor has lower ESR is preferred to use as the output capacitor. Keep in mind that the capacitance of a given capacitor typically degrades with increased temperature and bias voltage. Consult the capacitor manufacturer's data sheet when determining the actual capacitance of a capacitor under certain conditions. In this design, 4 Taiyo Yuden 4.7uF are selected as the output capacitors and connected in parallel to reduce the ESR, the functional capacitance is about 10uF.

Diode Selection

The diode conducts the inductor current to the output capacitor and load while the MOSFET is off. The average diode current is the load current: $I_{diode} = (1 - D)I_l = I_{load}$. Make sure the rated average forward rectified output current is greater than the load current. And the rated reverse voltage is higher than the output voltage. For better efficiency, choose the diode with

lower forward voltage drop V_F since the power dissipated in the diode is dominated by VF $*I_{load}$. For this reason, schottky diode is preferred. There is also Capacitance Loss due to the parasitic capacitor and Leakage Loss caused by leakage current which are given by $\frac{1}{2}C_{diode}(V_{out}+V_F)^2$ and $D * I_{leakage} V_{out}$ respectively. Choose diode with low capacitance and leakage current for better efficiency.

3.3 Slope Compensation

For continuous current-mode duty cycles greater than 50%, slope compensation is required to maintain stability of the current-mode regulator. For stable current-mode control loop, ensure damping Qp is in the range of 0.4 to 1[13]. However, we can loosen the requirement by calculating the magnitude of the open loop gain at the half switch frequency. In many cases, if the magnitude is less than -10dB or so, the current feedback loop is stable.

ADP1614 has internal slope-compensation. The only option for the compensation is to select the right inductor based on the input voltage range.

Assume the efficiency of the converter is 80%, from Equation2.11, we get the input current Iin is 3.43A for 3.5V input voltage and 2.18A for 5.5V input voltage respectively. V_{ON} = Vin - I_{IN}*ESRL is the voltage across the inductor when the switch is ON, and ESRL is the inductor ESR which is 10mΩ for SER1360-103KLB. Using Equation 2.18, 2.23, 2.24, 2.25 and the relative Qp value is given in Table 3.1 for different inductors.

Table 3.1 Qp varys with different inductor choices and Vin conditions

L (uH)	Vin=3.5V, Vramp=90mV			Vin=5.5V, Vramp=60mV		
	S_n	m_c	Qp	S_n	m_c	Q_p
3.3	1.50E+05	1.780	7.635	2.37E+05	1.329	2.348
4	1.24E+05	1.945	3.459	1.96E+05	1.399	1.884
5	9.90E+04	2.182	1.941	1.57E+05	1.498	1.470
6	8.25E+04	2.418	1.349	1.30E+05	1.598	1.205
7	7.07E+04	2.654	1.034	1.12E+05	1.698	1.020
8	6.19E+04	2.891	0.838	9.78E+04	1.797	0.885
9	5.50E+04	3.127	0.705	8.70E+04	1.897	0.782
10	4.95E+04	3.363	0.608	7.83E+04	1.997	0.700

From Table 3.1, we can see that if the inductance value is 3.3 uH, the current-mode control loop is unstable for Vin=3.5V or Vin=5.5V. Increasing the inductance to 10uH, Qp drops to 0.608 at Vin=3.5V and 0.7 at Vin=5.5V, the current-mode control loop is stable. In this design, we choose a 10 uH inductor.

3.4 Feedback Loop Design

There is potential risk for oscillation in a closed loop control system. Loop compensation is critical to the output voltage regulation, the stability and transient response. Oscillation may occur in a converter with poor phase margin, and small bandwidth results in very slow transient response. The goal of loop compensation is to provide enough gain and phase margin for the application.

Referring to Figure 3.3 shown below, the green line represents the gain and the red line represents the phase of the inner current loop from the control voltage (COMP pin) to the output.

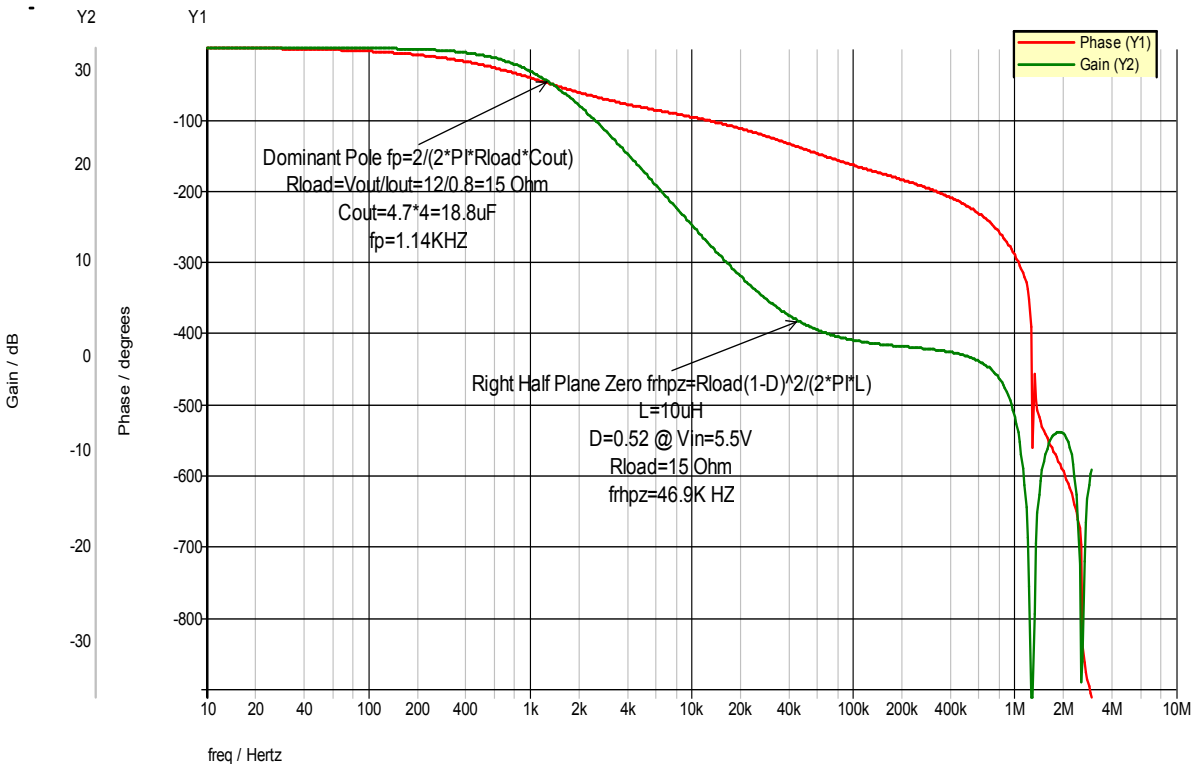


Figure 3.3 Bode Plot of Inner Current loop for CMC Boost Converter

The boost converter produces an undesirable Right-Half Plane (RHP) zero in the small signal analysis of control to output transfer function. This requires compensating the regulator such that the crossover frequency occurs well below the frequency of the RHP zero.

The general rule is to design the converter with RHPZ at the minimum input and maximum load (maximum output current), in this case the value of the RHP zero is the lowest. To stabilize the regulator, ensure that the regulator crossover frequency is less than the lowest RHP zero frequency or one-fifteenth of the switching frequency [23].

To optimize the converter dynamics for a given application, external components are used to connect to Comp pin of ADP1614 for compensating the loop[23].The required compensation can

be achieved by using a Type 2 compensation which brings two poles and one zero, as shown in Figure 3.4.

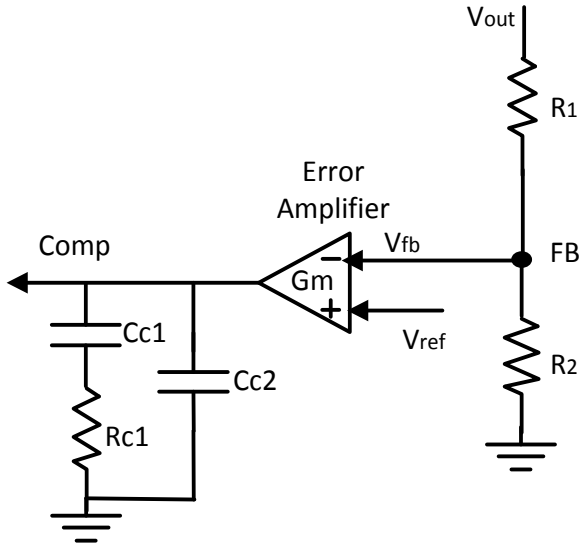


Figure 3.4 Compensation components

The output to compensation transfer function is given by

$$\frac{V_C}{V_{out}} = G_m \frac{R_2(1 + R_{c1}C_{c1}S)}{(R_1 + R_2)\left(1 + \frac{C_{c1}C_{c2}R_{c1}}{C_{c1} + C_{c2}}s\right)s} \tag{3.9}$$

The pole at origin is used to boost the DC gain. A zero of the compensation $f_z = \frac{1}{2\pi R_{comp} * C_{1comp}}$ is placed at the dominant pole of the converter, which is $\frac{2}{\pi * R_{load} * C_{out}}$ to improve the gain at the cross-over frequency. Place the 2nd pole of the compensation at ESR zero of the converter to attenuate the high switching noise. Figure 3.5 shows the bode plot of the compensator.

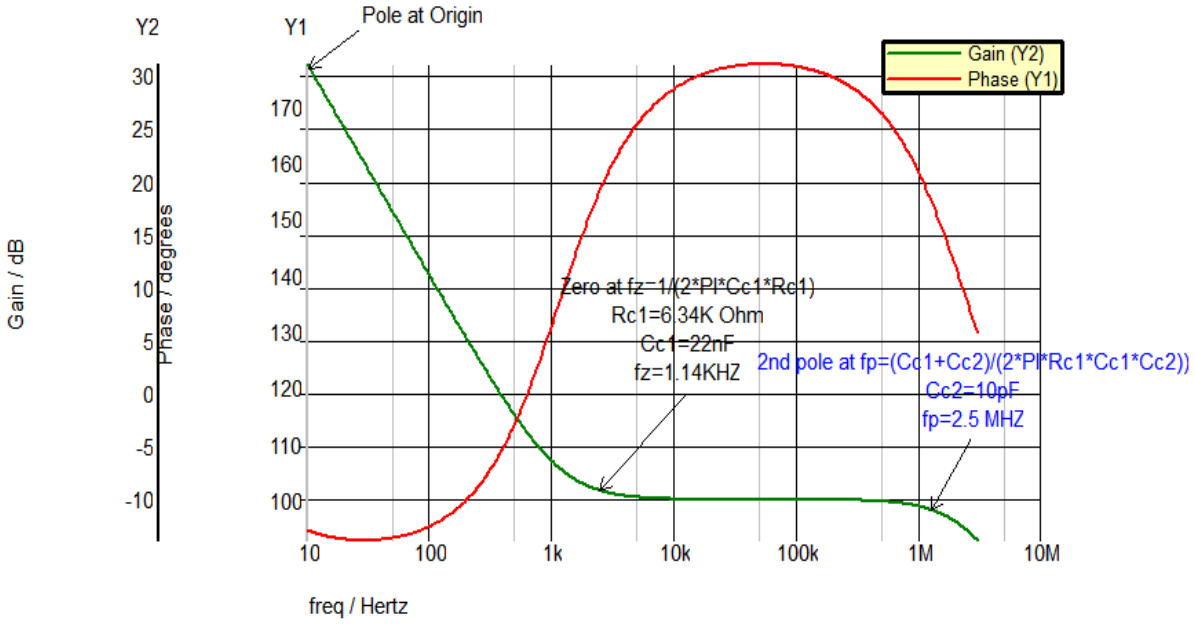


Figure 3.5 Bode Plot of type II compensation

3.4 Bill of Material

The part numbers, values and cost of all components are listed in Table 1

Table 3.2 List of Materials

Des -cription	MFG	Part Number	Component Specs	Qty	Area mm^2	Cost (USD)
U1	ADI	ADP1614ARMZ-1.3M-R7	Integrated Switching Regulator	1	9	$0.950
L1	Coilcraft	SER1360-103KLB	10uH, 10mOhms, 3.2 Apk	1	167.70	$0.710
D1	On Semi	MBRS240LT3G	2A ,40V	1	19.40	$0.128
Cin	Murata	GRM21BR71H105	1uF, 50V, 0805, X7R	1	2.5	$0.094
Cout1	Murata	EMK316 BJ475KL-T	4.7uF, 16V, 1206, X5R	4	20.48	$0.216
Cv5	Murata	GRM188R61A105K	1uF,10V,X5R	1	1.30	$0.010
Css	Vishay	10% tolerance	10 nF	1	0.70	$0.005
Rc1	Vishay	5% tolerance	6.34 kohm	1	0.70	$0.005
Cc1	Vishay	10% tolerance	22 nF	1	0.70	$0.005
Cc2	Vishay	10% tolerance	10pF	1	0.70	$0.005
Rf1A	Vishay	1% tolerance	165 kohm	1	0.70	$0.005
Rf2	Vishay	1% tolerance	19.1 kohm	1	0.70	$0.005
Rb0	Vishay	5% tolerance	1 Ohm	1	0.70	$0.005
Rs2	Vishay	5% tolerance	60.4 kOhm	1	0.70	$0.005
			Total		240.08	$2.153

CHAPTER 4 SIMULATION RESULTS

To verify the response of the current mode control boost converter, the model shown in Figure 2.9 was simulated using Simplis [34] with the following parameters: Vin=3.5-5.5V, Iout=800mA, Vout =12V, R1=19.1KΩ, R2=165KΩ, Cout=10.04 uF, ESR=5mΩ and the switching frequency = 1.3M Hz, the peak to peak Vramp is 90mV at input voltage 3.5V and 60mV at input voltage 5.5V, as listed in table 3.1.

4.1 Simulation Results Using 3.3uH Inductor

The open loop bode plot of the CCM operation using inductor L1=3.3uH is shown in figure 4.1,The current loop resonance at half of the switching frequency and the damping factor Qp of the double poles of the inner current loop is 7.635. The converter is unstable. An unstable, oscillating inductor current waveform and output voltage is shown in Figure 4.2.

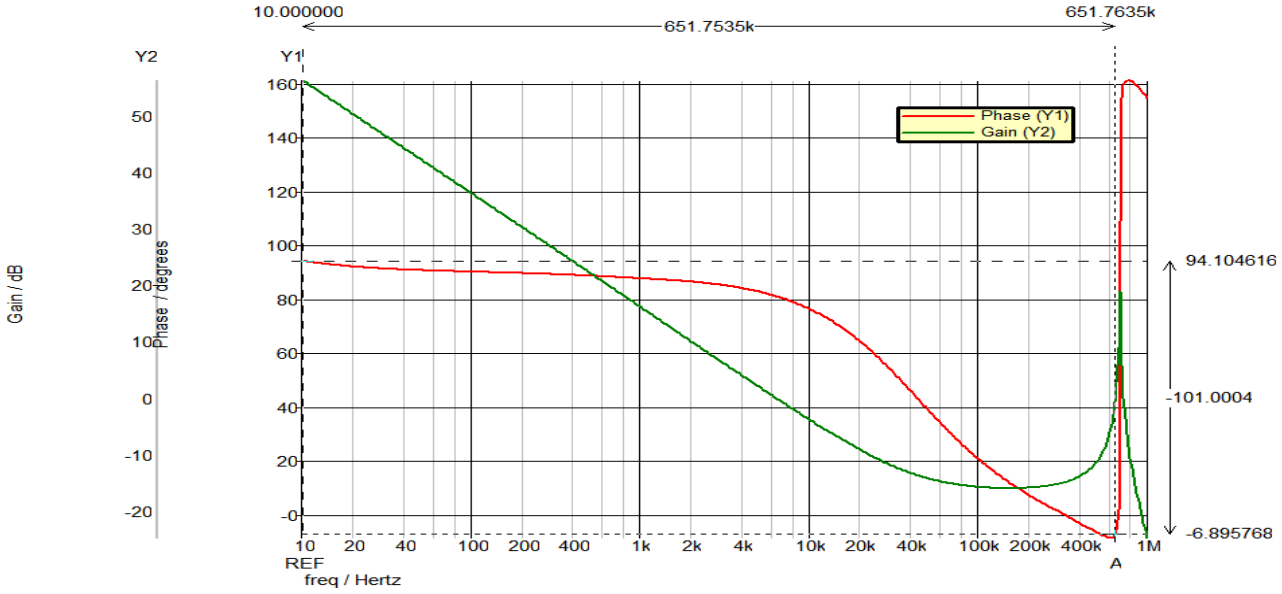


Figure 4.1 Open loop bode plot for V_{in}=3.5V, L=3.3uH

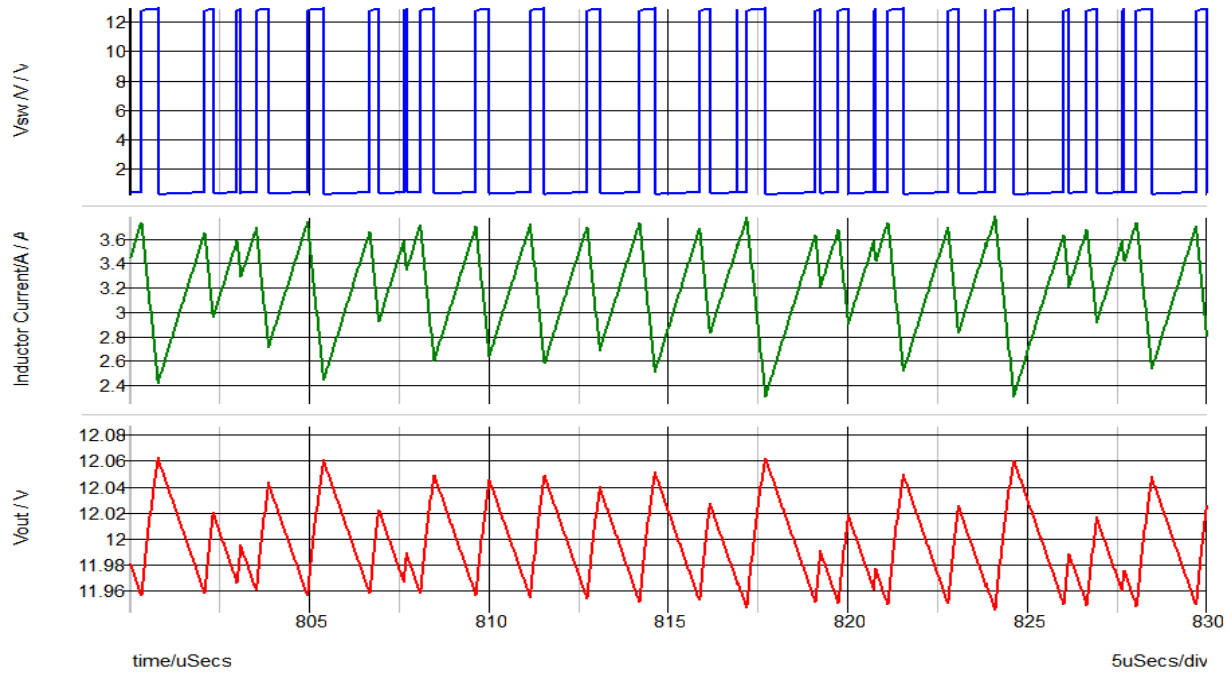


Figure 4.2 Unstable waveform of Vsw, I_L and V_{out} at Vin=3.5V, L=3.3uH

By keeping all the other parameters the same and only changing the input voltage from 3.5V to 5.5, the open loop bode plot of the converter is shown in figure 4.3, the crossover frequency is about 13.8 kHz, with a phase margin of 83 and the damping factor Qp of the double poles of the inner current loop is 2.348. The converter is at the boundary of stable. The gain at the double pole resonance frequency, half of the switching frequency is about -5dB. There are not enough margins for a practical design in case the operating condition changes due to the component tolerance or operating temperature. The switch node voltage, inductor current and output voltage is Figure 4.4.

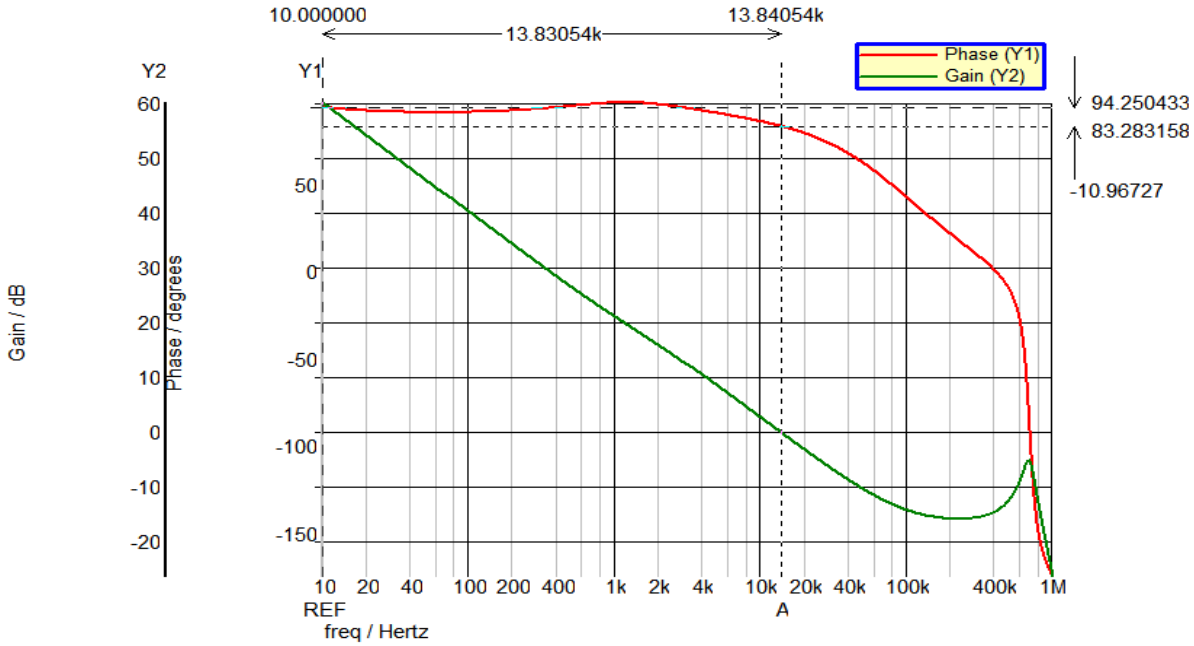


Figure 4.3 Open loop bode plot for Vin=5.5V, L=3.3uH

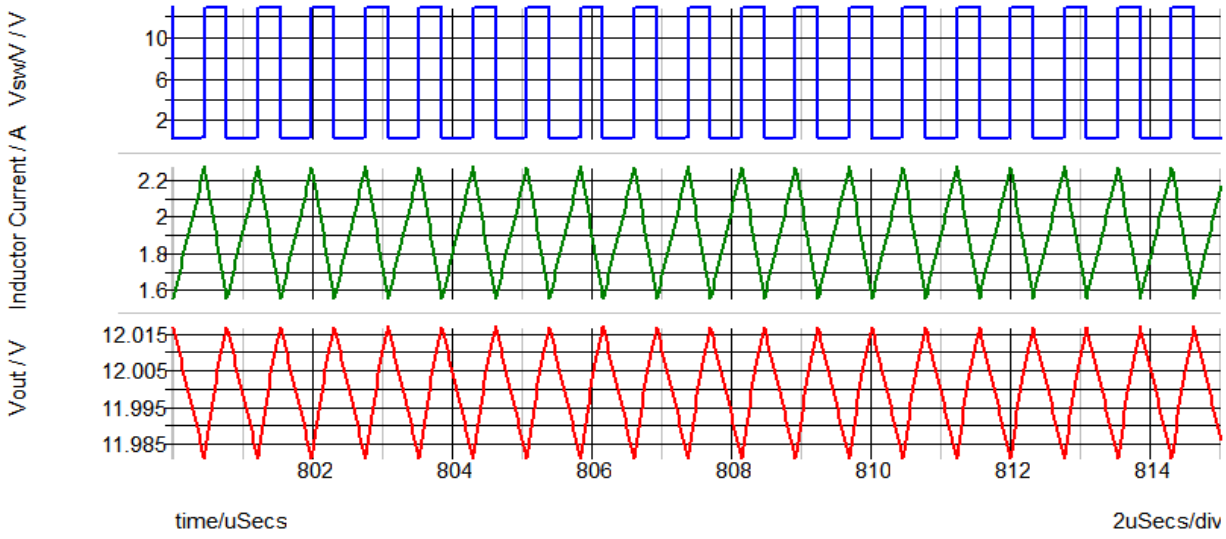


Figure 4.4 Waveform of Vsw, I_L and V_{out} for Vin=5.5V, L=3.3uH

4.2 Simulation Results Using 10uH Inductor

By keeping all the other parameters the same and only changing the 3.3uH inductor to a 10uH inductor, oscillations disappear at 3.5V input voltage, shown in Figure 4.5 and Figure 4.6. The damping factor Qp of double poles of the inner current loop transfer function is 0.608, which is in the range of 0.4 to 1. The current loop of the converter is stable.

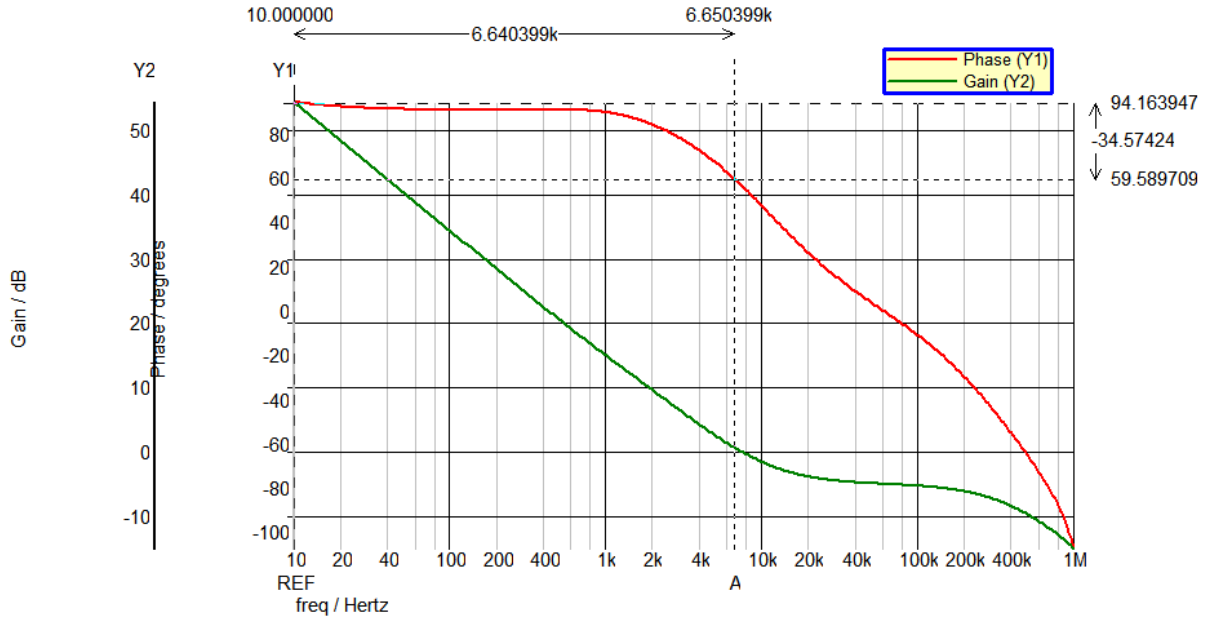


Figure 4.5 Open loop bode plot for Vin=3.5V, L=10uH

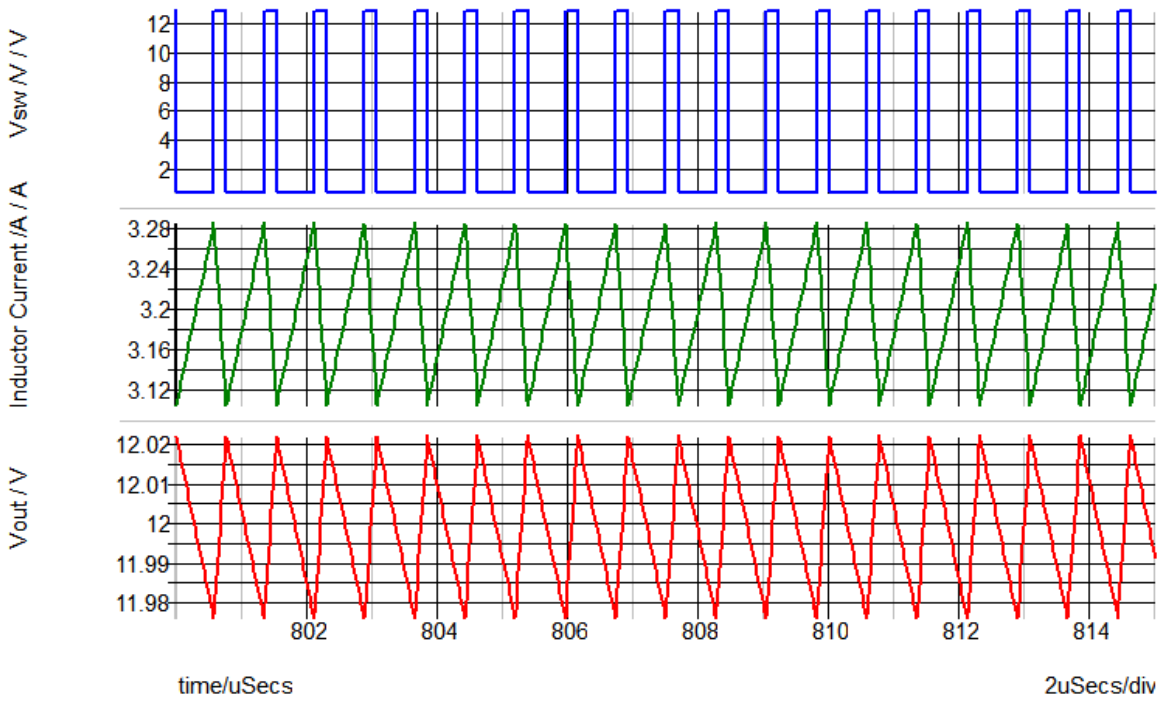


Figure 4.6 Waveform of Vsw, I_L and V_{out} for Vin=3.5V, L=10uH

Now, change the input from 3.5V to 5.5V, the open loop bode plot and the Switch node voltage, inductor current and output voltage is illustrated in figure 4.7 and 4.8 respectively. At input voltage 5.5V, the Qp value of double poles of the current loop transfer function is 0.7. The current loop of the converter is stable which can be observed from the bode plot, there is no 2nd cross at the half switch frequency. The simulations support the theoretical analysis.

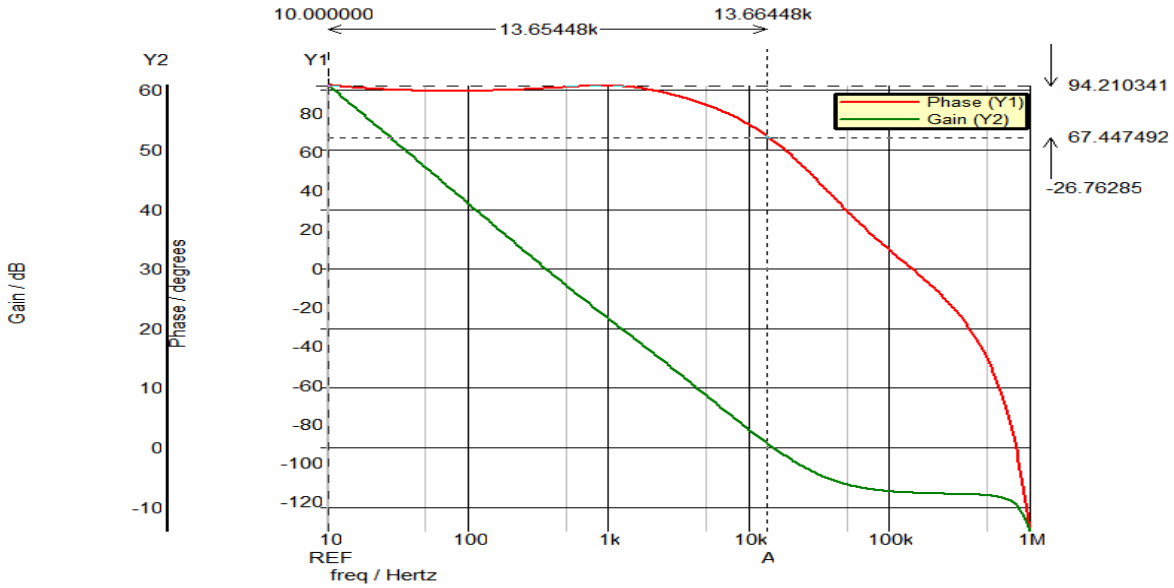


Figure 4.7 Open loop bode plot for Vin=5.5V, L=10uH

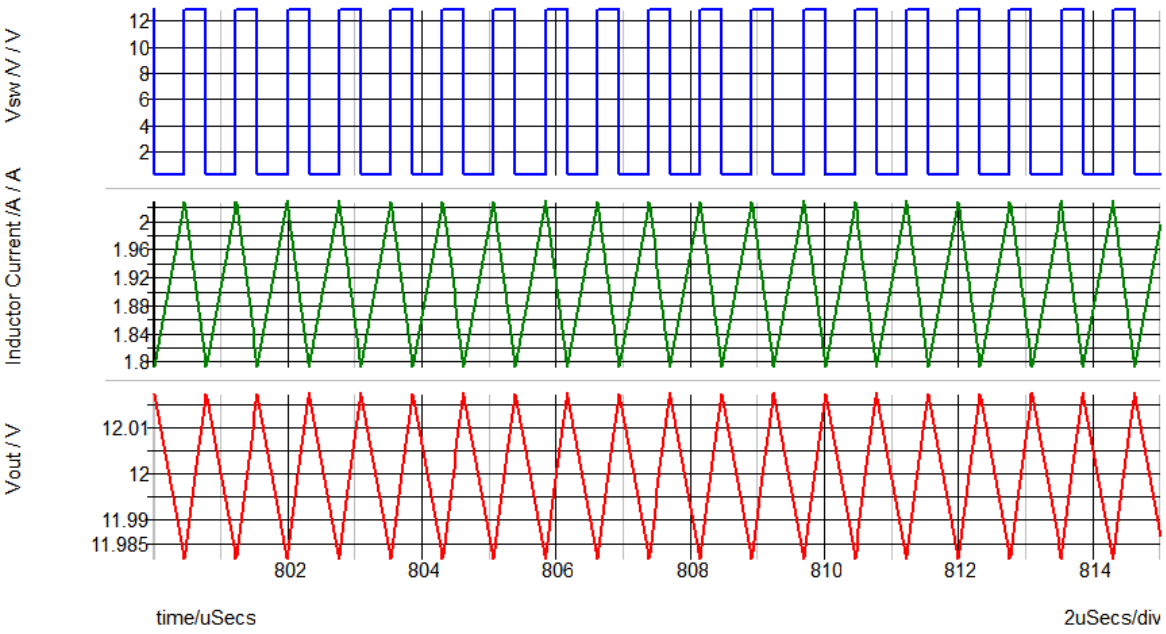


Figure 4.8 Waveforms of Vsw, I_L and V_{out} for Vin=5.5 V, L=10uH

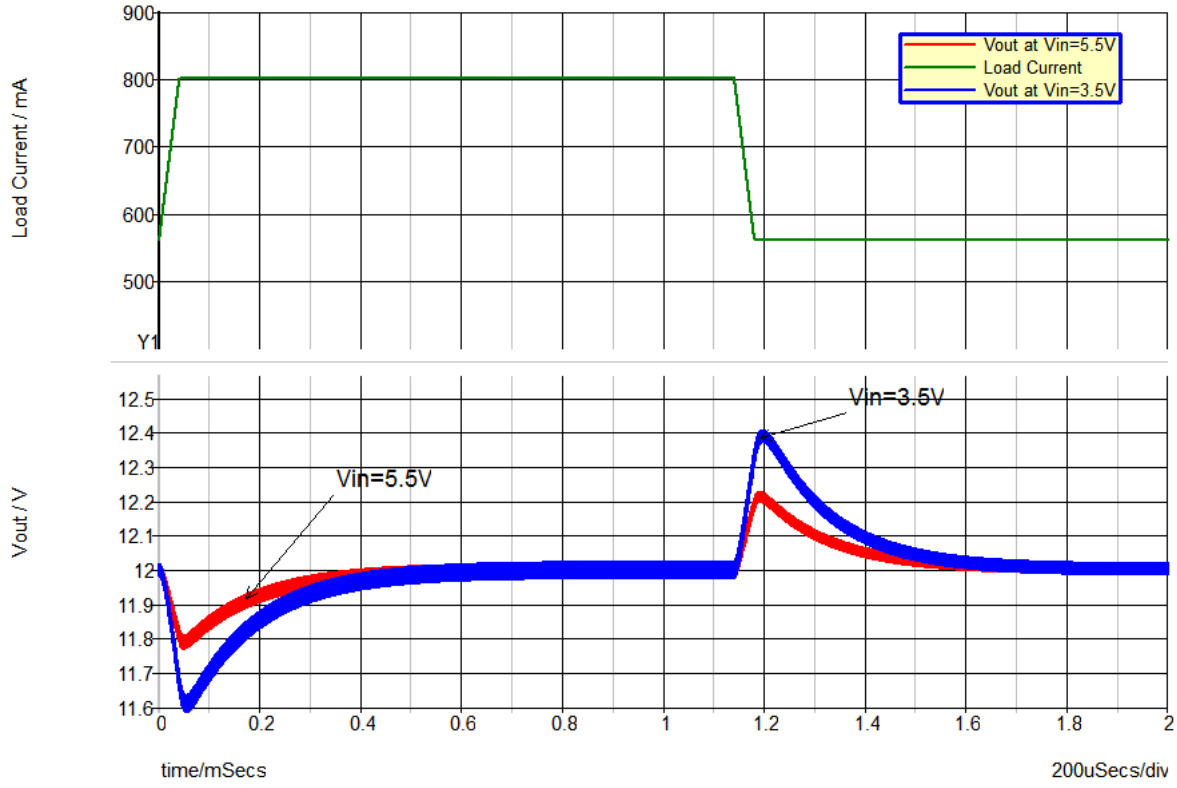


Figure 4.9 560mA to 800mA load Transient for L=10uH

The load transient response for 10uH inductor is shown in Figure 4.9. The response is overdamped for the minimum and the maximum input voltage. For both cases, the open loop phase margin is greater than 45 degree. The output step error for Vin=3.5V and Vin=5.5V are 780mV and 400mV respectively for 560mA to 800mA load transient At the maximum input voltage Vin=5.5V, the converter has fast transient response and less overshoot, as the open loop crossover frequency is higher than that for the minimum input voltage Vin=3.5V.

CHAPTER 5 EXPERIMENT RESULTS

The 1.3MHZ, Current Mode Control boost converter shown in Figure 3.1 was built on ADP1614 Evaluation Board using the components listed in Table3.2 and tested with the simulation results of Chapter 4.

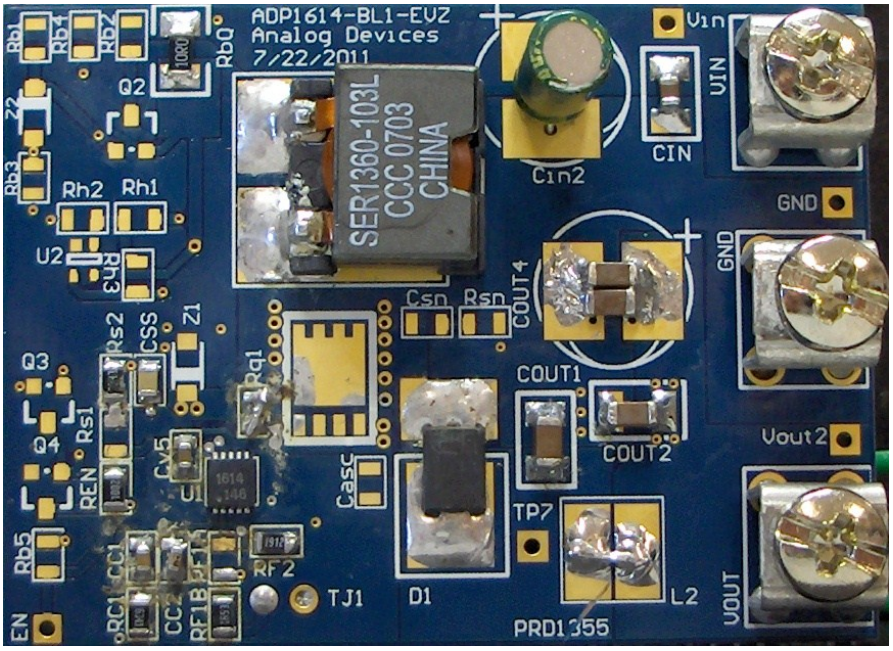


Figure 5.1 Prototype of 1.3MHZ CMC Boost converter

5.1 Bode plot test

The purpose for bode plot test is to evaluate the converter loop response for stability. The Frequency Response Analyzer is an instrument that injects a test signal and measures the response of a system to that frequency from the return signals. It enables the measurement of the open loop frequency response of the power supply loop in a closed loop configuration.

As show in Figure 5.2, there's a 10Ω resistor in the feedback path which serves as an AC signal injection point. The Frequency analyzer tracks the sine wave source that is applied across

the signal injection resistor and measure the response of this system. By increasing the frequency and measuring the response, and so on so forth throughout the entire interested frequency range in the analysis, the Frequency Response Analyzer makes a swept frequency response measurement that gives the magnitude and phase data plotted verses frequency. This injection topology can also be applied to other type of converters.

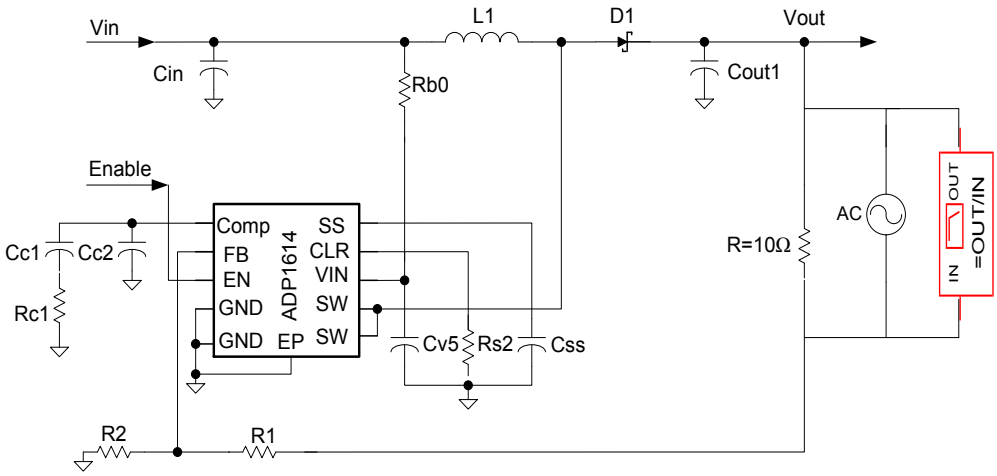


Figure 5.2 Boost converter connected with Frequency Response Analyzer

The bode plot was taken using Frequency Analyzer AP200 which can measure up to 15 MHz maximum. Usually 1 MHz is actually adequate for any of the loop responses of the applications. Higher frequency measurement makes it possible to evaluate the parasitic of inductors and the input and output capacitors by observing the high frequency resonance

The graphics below shows the test results for the Current Mode Control boost converter built in the laboratory. The green lines is the bode plot for Vin=3.5V with 6KHZ cross-over frequency, 64 degree phase margin, the blue line is for Vin=4.5V with 11 KHZ crossover frequency and 64.5 degree phase margin, and red line is for Vin=5.5V with 15 kHz cross-over frequency and 66 degrees phase margin. This represents an optimal loop design.

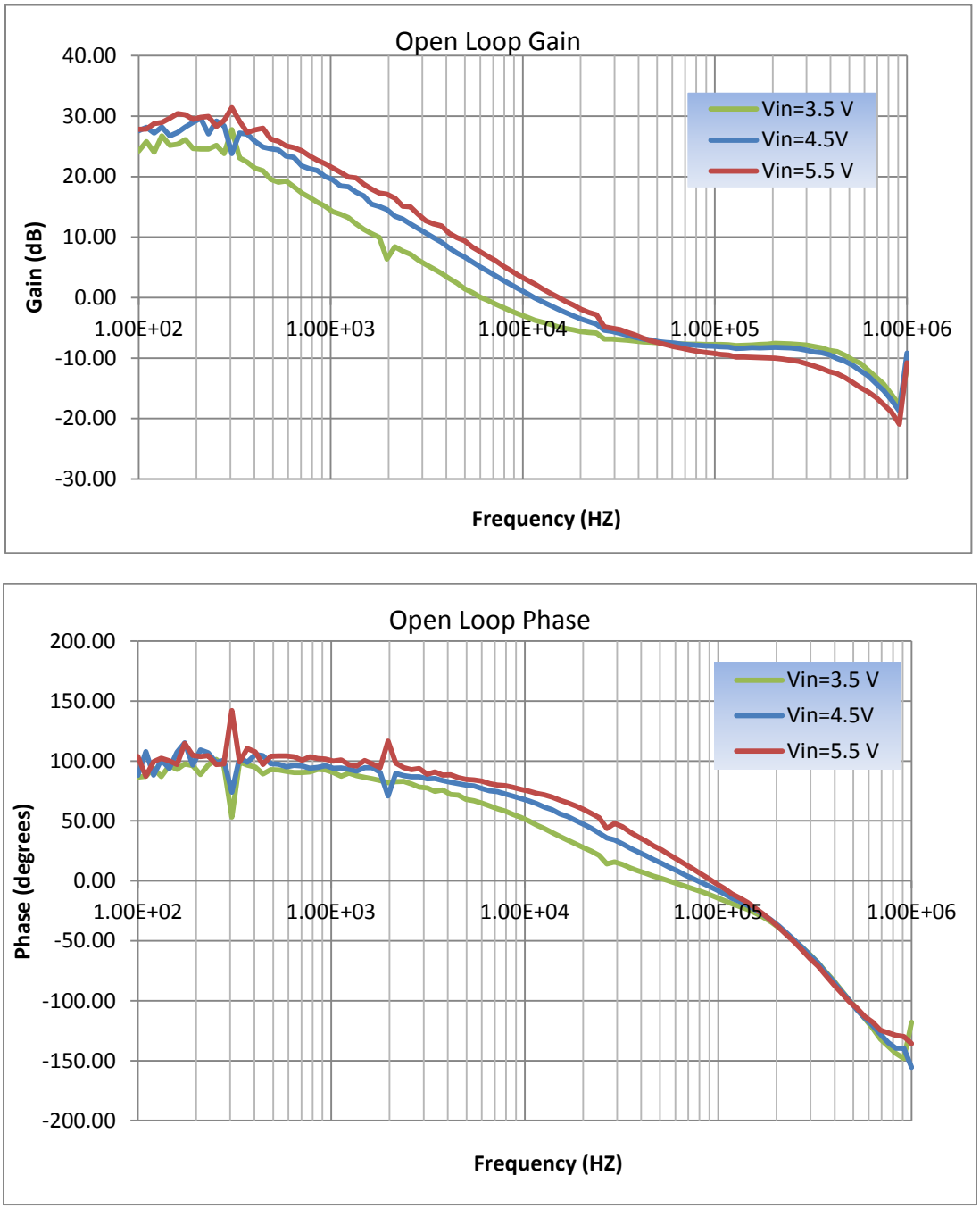


Figure 5.3 Open Loop bode plot lab test for V_{in}=3.5V, 4.5V and 5.5V

5.2 Inductor Current and Output voltage

Waveforms of inductor current I_L, switch node voltage V_{SW} and output voltage Vout at Vin=3.5V and 5.5V are shown in figure 5.4 and Figure 5.5 respectively. The converter is

operating in Continuous Conduction Mode with 71.5% duty cycle at Vin=3.5V and 55% duty cycle at Vin=5.5V. The stable waveforms can be observed in both cases with output voltage ripple less than 32mV.

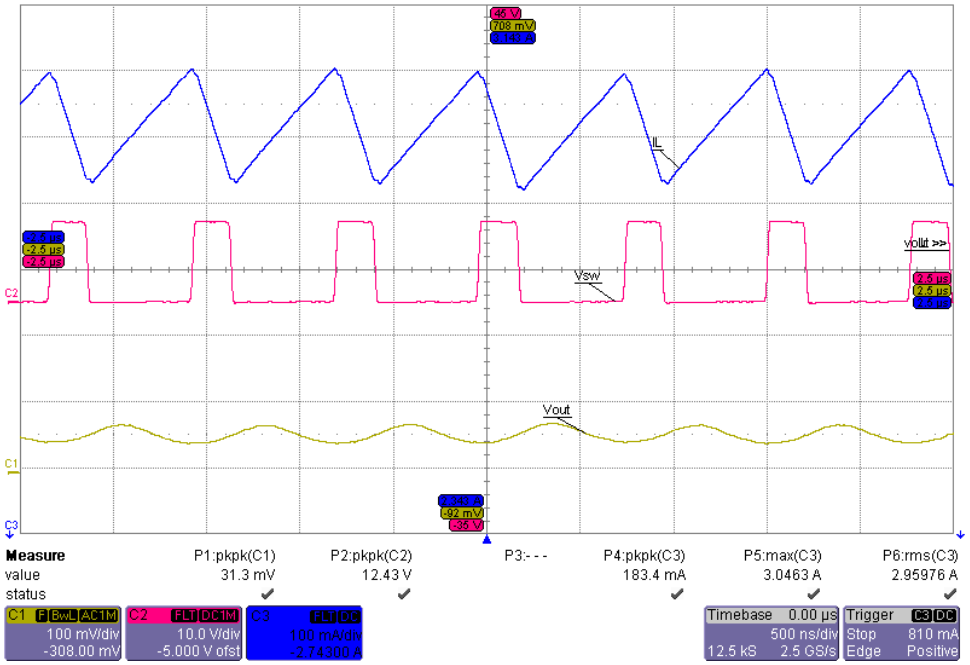


Figure 5.4 Waveforms of inductor current I_L, switch node voltage V_{SW} and output voltage V_{out} at Vin=3.5V

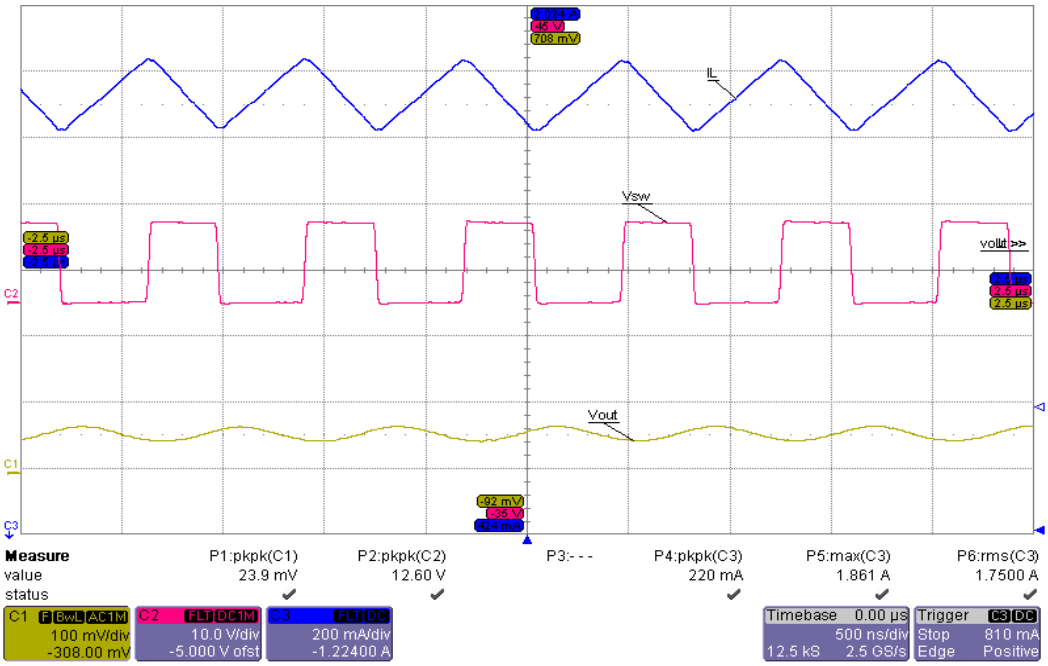


Figure 5.5 Waveforms of inductor current I_L, switch node voltage V_{SW} and output voltage V_{out} at V_{in}=3.5V

5.3 Transient Response

An under damped system is not stable, the poor phase margin leads to overshoot and ringing. While an over damped system with too much phase margin is stable, yet it does not give the best transient recovery performance. For waveforms shown in Figure 5.6 and 5.7, the output current step error is 30% for I_{OUT}=0.8A, the worst case of transient response is when Vin is the minimum input voltage 3.5V, the output voltage overshoot is 378mV and the under shoot is 370 mV, the totally Vout step error is 748mV which is less than 8% of the output voltage.

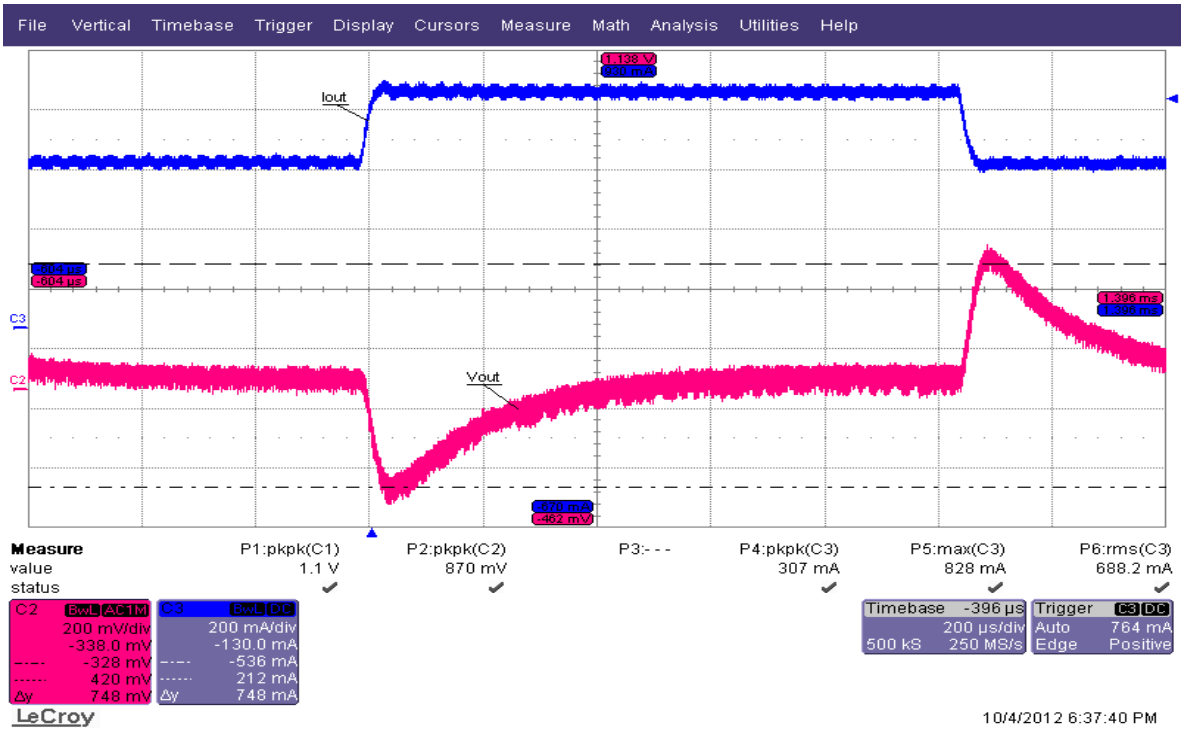


Figure 5.6 560mA to 800mA Load Transient response, V_{in}=3.5V V_{out}=12V

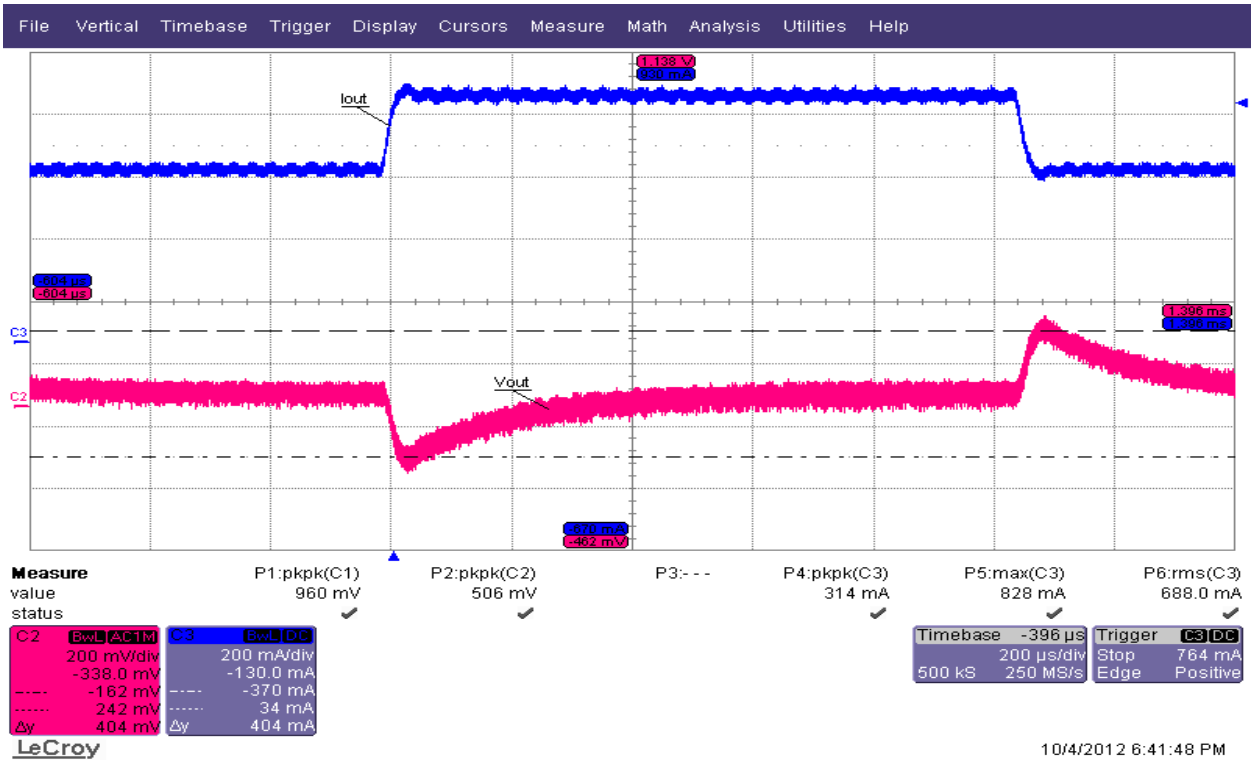
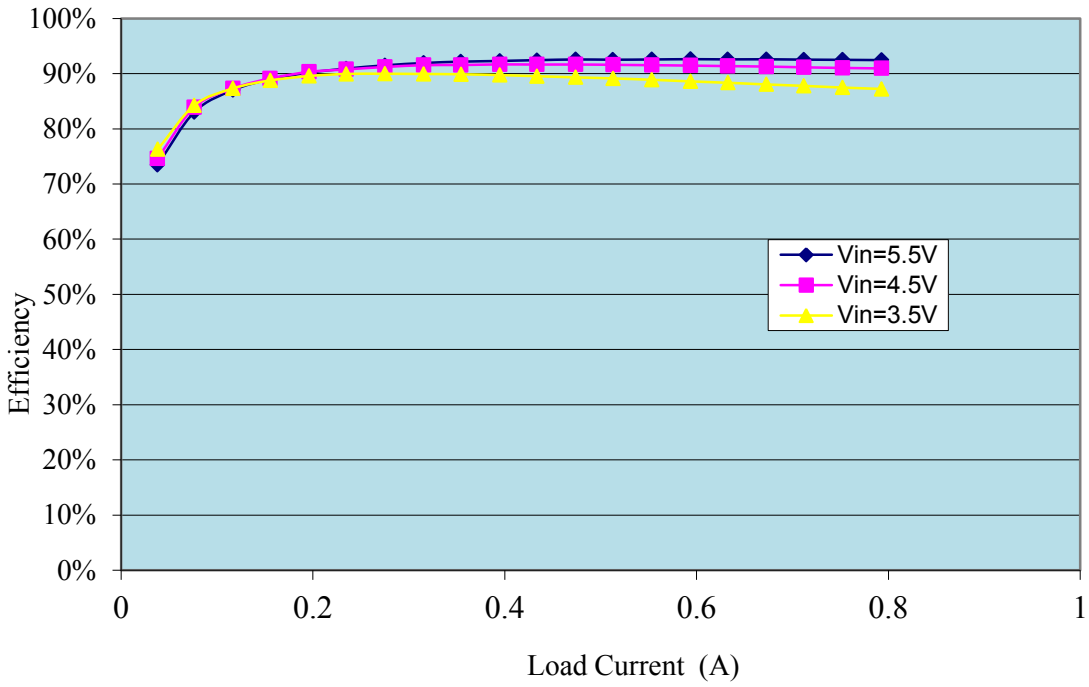


Figure 5.7 560mA to 800mA Load Transient response, V_{in}=5.5V V_{out}=12V

5.4 Efficiency Test

The efficiency test result is shown in figure 5.8. To reduce the power consumption in the rectifier diode, a Schottky diode with low forward voltage was used. Notice that as the input voltage decreases, the efficiency drops slightly. The lower input voltage causes higher inductor current which results in higher inductor core losses and copper loss.



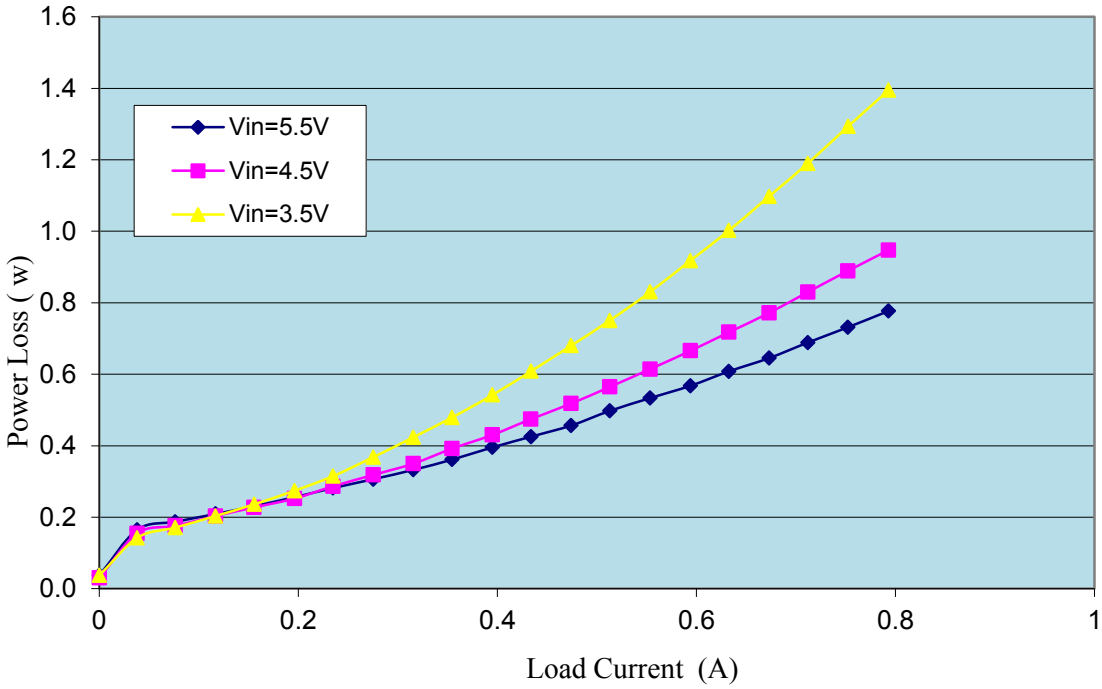


Figure 5.8 Efficiency test result for V_{in}=3.5V, 4.5V and 5.5V

CHAPTER 6 CONCLUSION AND FUTURE WORK

6.1 Conclusions

Usually, dc-dc converters are designed to operate in the Discontinuous Conduction Mode (DCM) when there is light load (small DC load current).Yet, in some cases, they are purposely designed to operate in DCM as there is no right half plane zero under these conditions, so that the converter in DCM can have higher loop crossover frequency allowing quicker transient response to load or input changes.

When the boost converter operates in Continuous Conduction Mode (CCM), the topologies have a RHPZ in their control to output transfer function. Using voltage Mode Control, the sharp phase drop after the filter resonant frequency requires a type three compensator. However, using Current Mode Control makes the compensation of the boost converter much easier as the power stage has a response of single-pole system at low frequency and using a type two compensator is adequate, which greatly simplifies the design process.

Current-mode control has subharmonic oscillation when the duty cycle of the converter approaches 50% due to the difference between the average inductor current and the value of current when the sample is taken. Subharmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node, like any other oscillation, will continue to ring and grow in amplitude which leads to the instability of the converter. Slope compensation is required to maintain stability of the current-mode regulator.

For IC controller that has internal slope-compensation, select the inductor value which makes Qp value keep in the range of 0.4 to 1 or so, or make sure the amplitude at the half switch frequency is below -10dB. This works for many applications. For general application, it is better

to have too much slope compensation when it is not needed rather than too little when it is needed to ensure a stabilized system. The performance drawback with too much slope compensation is lower crossover frequency.

6.2 Future Works

Current Mode Control of switching power converters has many advantages over the conventional Voltage Mode Control. Nevertheless, every choice has consequences we must be aware of. The problematic part of Current Mode Control is measuring the current accurately. One issue is the time delay, caused by the parasitic capacitor around the power switch from charging and discharging, affects the accuracy of current sensing. The other issue is that this parasitic capacitance along with the parasitic inductor associated with the current sensor resistor and the path cause other poles which need to be considered in the loop compensation.

Current Mode Control has inherent peak current limiting to protect on-switch peak current stress. ADP1614 has a pin-adjustable current limit that can be set be the current limit resistor R_{CL} shown in figure 3.2. However, changing the current limit also changes the gain of the error amplifier as seen from the experiment shown in Figure 7.1with the following parameters: 5.5V input and 12V/180mA output, 650KHZ switch frequency. One obvious effort in the future could be model the relationship of the error amplifier gain and the current limit resistor. This is the first step for loop compensation to optimize the open loop gain and the bandwidth of the converter and therefore the converter will have better transient response even with higher current limit resistor.

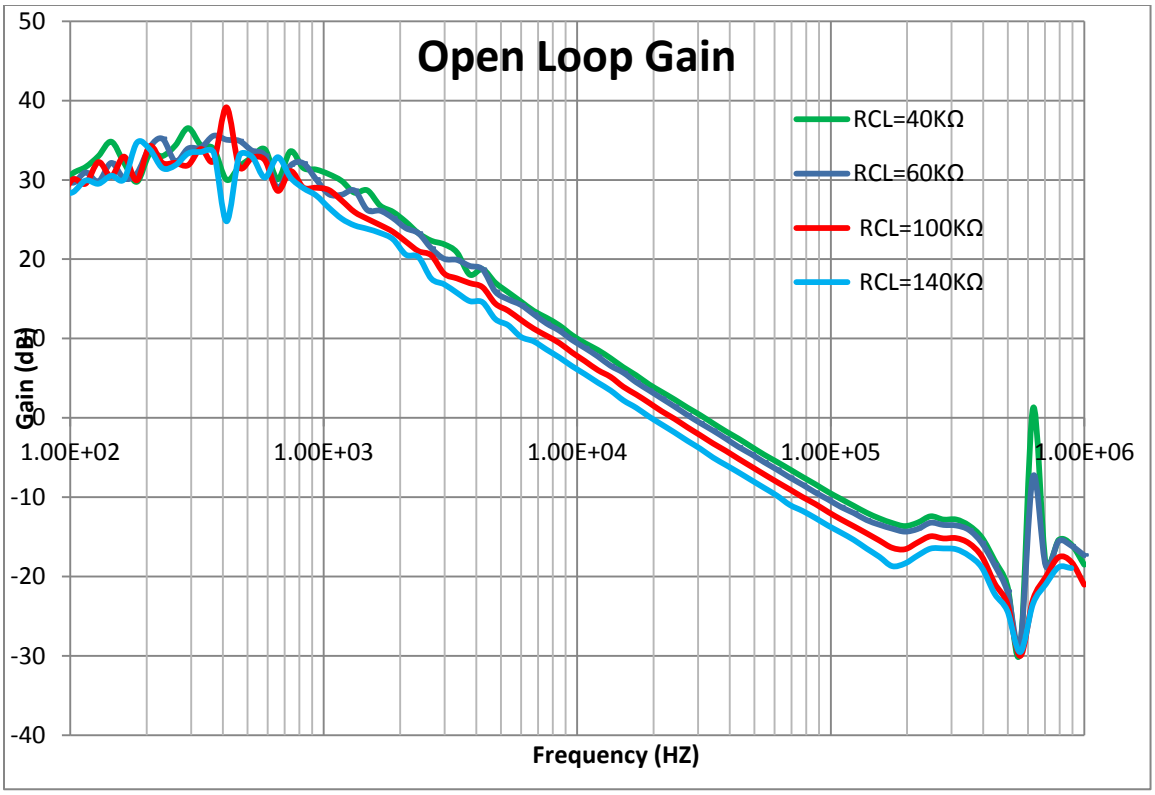


Figure 6.1 Open Loop gain varies with current limit resistor R_{CL}

The slope compensation is essential for the stability of converters with Current Mode Control. Determining the slope compensation voltage ramp is the first important for eliminating the subharmonic oscillation occurs in the current control loop. The voltage ramp of the ADP1614 varies with input and output voltage. Future effort to expand on this research could accurately model the voltage ramp of the current feedback loop from the lab experimental results.

REFERENCE

[1] Robert W. Erickson, Dragan Maksimovic, "Fundamentals of Power Electronics", Kluwer Academic Publishers, 2e, 2001

[2] George Collins, "ECE 562, Lecture notes on Power Electronics I, Colorado State Univ, ECE Dept" Fall 2011

[3] "The Right-Half-Plane. Zero -- A. Simplified. Explanation", available at http://www.ti.com/lit/ml/slup084/slup084.pdf

[4] Christophe Basso, "Understanding the Right-Half-Plane Zero Part 1", Apr1, 2009 http://powerelectronics.com/power_management/understanding_righthalfplane_zero_part_one_0409/

[5] Christophe Basso , "Understanding the Right-Half-Plane Zero part2", http://powerelectronics.com/power_management/power_understanding_righthalfplane_zero_0509/

[6] Christophe Basso, " Compensating the RHPZ in a CCM Boost Converter: the analytical way", available at: http://powerelectronics.com/power_management/compensating_rhpz_ccm_0609/index.html

[7] Wei-Chung Wu, R.M. Bass, J.R. Yeargan, " Elimination the effects of the Right-half Plane Zero in Fixed Frequency Boost Converters", *IEEE Annual Power Electronics Specialists Conference 06/1998,* 362 - 366 vol.1

[8] Christophe Basso, " the PWM switch operated in Borderline Condition, current mode", available at: http://cbasso.pagesperso-orange.fr/Spice.htm

[9] Christophe BASSO, "The Right−Half –Plane Zero, a Two-Way Control Path", http://cbasso.pagesperso-orange.fr/Spice.htm

[10] L. Dixon, "The right-half-plane zero – a simplified explanation", Unitrode seminars SEM-500

[11] R.B. Ridley, "A More Accurate Current-Mode Control Model", available http://www.ridleyengineering.com

[12] Robert Sheehan, " A New Way to Model Current-Mode Control ", May 1, 2007 , By, National Semiconductor, Santa Clara, Calif.

[13] R. Ridley, "Current Mode Control Modeling", *Switching Power Magazine*, 2006,

[14] R. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron*, vol. 6, no. 2, pp. 271–280, 1991.

[15] R.B. Ridley, "Boost converter with Current-Mode Control Model --- Power Supply Control Design Tools–Part 3", http://www.ridleyengineering.com

[16] R.B. Ridley, "Boost converter with Current-Mode Control Model --- Power Supply Control Design Tools–Part 4", http://www.ridleyengineering.com

[17] R. B. Ridley, "A New Small-Signal Model for Current-Mode Control." Ph.D dissertation, November 27, 1990.

[18] R. B. Ridley, " Current Mode or Voltage Mode", *Switching Power Magazine*, October 2000

[19] Robert Sheehan, "Understanding and Applying Current-Mode Control Theory", http://www.national.com/assets/en/other/UnderstandingandApplyingCurrent-ModeControlTheoryv1.pdf

[20] Robert Sheehan, "A New Way to Model Current-Mode Control, Part 1," *Power Electronics Technology Magazine*, May 2007.

[21] Robert Sheehan, "A New Way to Model Current-Mode Control, Part 2," *Power Electronics Technology Magazine*, June 2007.

[22] F.D. Tan, R.D. Middlebrook, "A Unified Model for Current-Programmed Converters," *IEEE Transactions on Power Electronics,* Volume 10, Issue 4, pp. 397–408, 1995.

[23] ADP1614 Datasheet, Available http://www.analog.com/ADP1614

[24] ADP1621 Datasheet, Available http://www.analog.com/ADP1621

[25] V. Vorperian, "Simplified Analysis of PWM Converters Using the Model of the PWM Switch: Parts I and II," *IEEE Transactions on Aerospace and ElectronicSystems,* Vol. AES-26, pp. 490-505, May 1990.

[26] E. Rogers, "Control Loop Modeling of Switching Power Supplies," *Proceedings of EETimes Analog and Mixed-Signal Applications Conference,* July 13-14, 1998, San Jose, CA.

[27] Lloyd Dixon, Average Current Mode Control of Switching Power Supplies, http://ecee.colorado.edu/~ecen5807/course_material/papers/cpm/Dixon_1990.pdf

[28] V. Vorpérian, "Analysis of Current-Mode Controlled PWM Converters Using the Model of the Current-Controlled PWM Switch." *Power Conversion and Intelligent Motion*, October 1990.

[29] K.G. Remya, Chikku Abraham, and Babita R. Jose, " A Slope Compensated Current Mode Controlled Boost Converter", *Communications in Computer and Information Science*, 2012, Volume 305, Part 3, 69-76

[30] Keith Billings, "Switchmode Power Supply Handbook", McGraw-Hill Inc, 1989

[31] Marty Brown, “Power Supply Cookbook”, *Elsevier Science*, 2e, 2001

[32] C. Basso, “Switch Mode Power Supplies: SPICE Simulations and Practical Designs”, McGraw-Hill

[33] Brian T.Lynch, Under the Hood of a DC/DC Boost Converter, available at http: // focus.ti.com/download/trng/docs/seminar/Topic_3_Lynch.pdf

[34] “SIMetrix/ Simplis---Circuit Simulation Software For Power Electronics Designers” http://www.simplistechnologies.com/

[35] “Measuring Frequency Response, Tips and Methods” http://www.ridleyengineering.com

[36] Venable Technical Paper #5, “Current Mode Control” http://www.venable.biz/tp-05.pdf